Tentative

IPS Alpha Technology, Ltd.

TECHNICAL DATA

AX080F068G

CONTENTS

RECORD OF REVISION

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DESCRIPTION

The following specifications are applied to the following TFT module.
Note : Inverter for back light unit is built in this module.

Product Name : 32FHD

General Specifications

Effective Display Area	: (H) 698.4 × (V) 392.85	(mm)
Number of Pixels	: (H)1,920×(V)1,080	(pixels)
Pixel Pitch	: (H) 0.3638 × (V) 0.3638	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Semi-Glare	
Number of Colors	: 1,073,741,824	(colors)
Viewing Angle Range	: Super wide version (Horizontal & Vertical : 170°at φ=0°,90°, 180°,270°, CR≧10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 8pcs. of CCFL	
External Dimensions	: (H)760.0 x (V)450.0 x (t)48.0Max	(mm)
Weight	:TBD	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1),5)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	TBD	m/s2	3)
Shock	-	29.4(3G)	-	TBD	m/s2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	

Note 1) Temperature and Humidity should be applied to the glass surface of a TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 70℃ on the condition of operating.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≦40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta＞40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
However, it does not affect the characteristics and reliability of the product.

1.2 Electrical Absolute Maximum Ratings

(1)TFT Module Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	0	13.2	V	
Input Voltage for logic	VI	-0.3	4.0	V	1)
Electrostatic Durability	VESD0	±100		V	2),3)
	VESD1	±20		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient：200pF-250Ω, Environmental：25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light Inverter Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Voltage	Vin	0	26.4	V	
ON/OFF Control Input Voltage	ON/OFF	0	6.0	V	
Brightness Control Voltage	PWM	0	3.3	V	

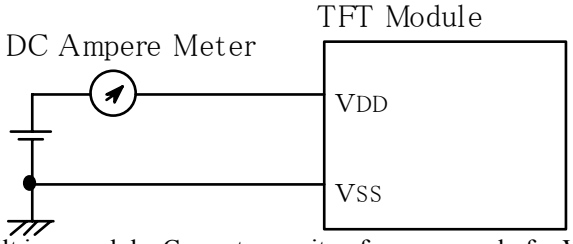
2. ELECTRICAL CHARACTERISTICS

2.1 TFT-LCD Module

Ta=25℃、Vss=0V

ITEM		SYSTEM	Min.	Typ	Max	単位	備考
Power supply Voltage		VDD	11.4	12.0	12.6	V	
Power supply Current		I DD	-	(0.8)	TBD	A	1),2)
Ripple voltage of power Supply		VDDR	-	-	350	mV	
LVDS select	High	LVDSSEL	2.2	3.1	3.6	V	
	Low		0	0	0.6	V	

Note 1)fV=60.0Hz, fCLK=82MHz, VDD=12.0V, and Display pattern is white.



2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of electrical circuit of module.

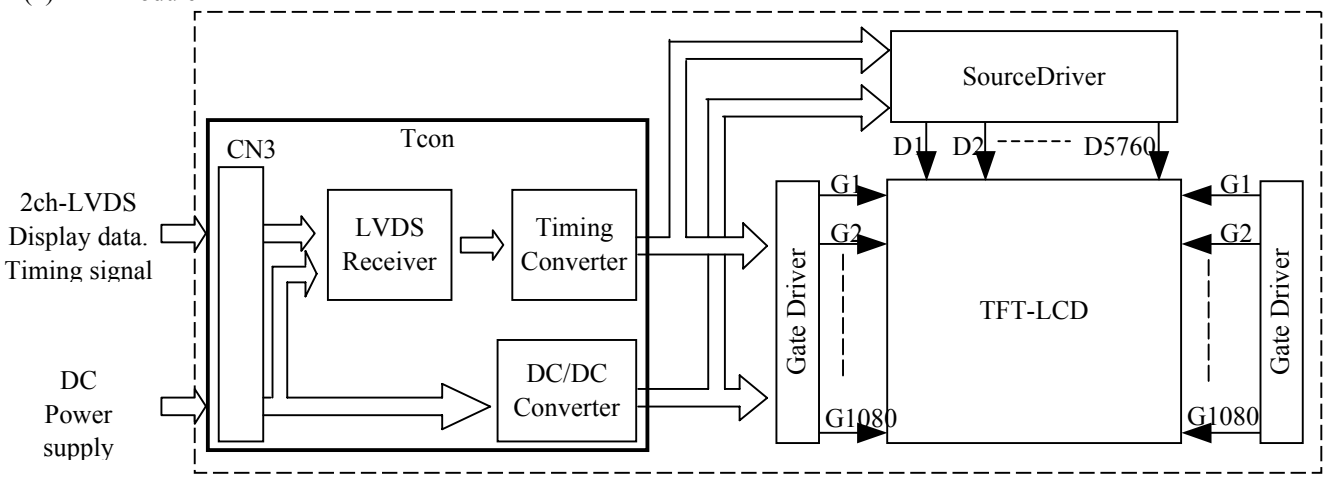
2.2 Back Light

ITEM		Symbol	Min.	Typ.	Max.	Unit	Notes
Input Voltage		VBL	21.6	24.0	26.4	V	
Input Current		IBL	-	3.2	-	A	VBL=24V, PWM on Duty100% 3)
ON/OFF Control Voltage	ON	ON/OFF	2.0	-	5.0	V	
	OFF		0	-	0.8	V	
Brigthness Control Input Voltage	Min. Brightness	PWM	-	0	-	V	
	Max. Brightness		-	-	3.3	V	
PWM Duty	Min. Brightness	on-Duty	-	(20)	-	%	
	Max. Brightness		-	-	100		

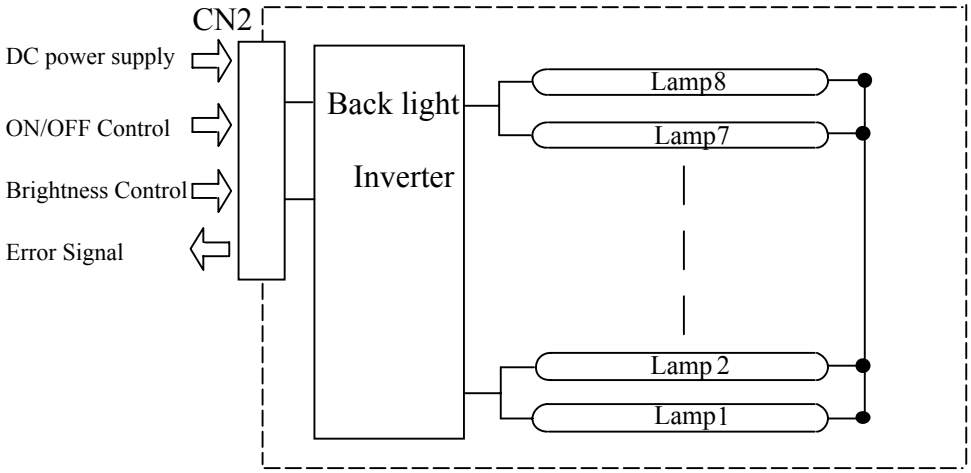
Note 3)This characteristics should be applied putting on the lamp about 60 minutes later with ambient temperature. (Ta=25℃±2℃)

3. BLOCK DIAGRAM

(1) TFT Module



(2) Back light unit



4. INTERFACE PIN ASSIGNMENT

4. 1 TFT-LCD module

CN3:JAE FI-R51S-HF

(Matching connector : JAE FI-R51-HL)

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	VSS	GND(0V)	2)
2	Test		4)
3	IC	Internally Connected, Keep Open	
4	IC		
5	IC		
6	IC		
7	LVDSSEL	Select LVDS Data Format	5)
8	IC	Internally Connected, Keep Open	
9	NC	No Connection	
10	NC		
11	VSS	GND(0V)	2)
12	RxA0-	ODD Pixel Data	3)
13	RxA0+		
14	RxA1-	ODD Pixel Data	3)
15	RxA1+		
16	RxA2-	ODD Pixel Data	3)
17	RxA2+		
18	VSS	GND(0V)	2)
19	CLKA-	ODD Pixel Clock	3)
20	CLKA+		
21	VSS	GND(0V)	2)
22	RxA3-	ODD Pixel Data	3)
23	RxA3+		
24	NC	No Connection	
25	NC		
26	VSS	GND(0V)	2)
27	VSS		

PIN No.	SYMBOL	DESCRIPTION	NOTE
28	RxB0-	EVEN Pixel Data	3)
29	RxB0+		
30	RxB1-	EVEN Pixel Data	3)
31	RxB1+		
32	RxB2-	EVEN Pixel Data	3)
33	RxB2+		
34	VSS	GND(0V)	2)
35	CLKB-	EVEN Pixel Clock	3)
36	CLKB+		
37	VSS	GND(0V)	2)
38	RxB3-	EVEN Pixel Data	3)
39	RxB3+		
40	NC	No Connection	
41	NC	No Connection	
42	VSS	GND(0V)	2)
43	VSS		
44	VSS		
45	VSS		
46	VSS		
47	NC	No Connection	
48	VDD	Power Supply (typ.+12V)	1)
49	VDD		
50	VDD		
51	VDD		

Note 1) All VDD pins shall be connected to +12.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) Rx n+ and Rx n- (n=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

4) Open : Normal mode. GND : Test mode.

5) See page 8-3/6 & 8-4/6

4. 2 Back light unit

Inverter pin assignment

JST S14B-PHA-SM-TB(LF)(SN)

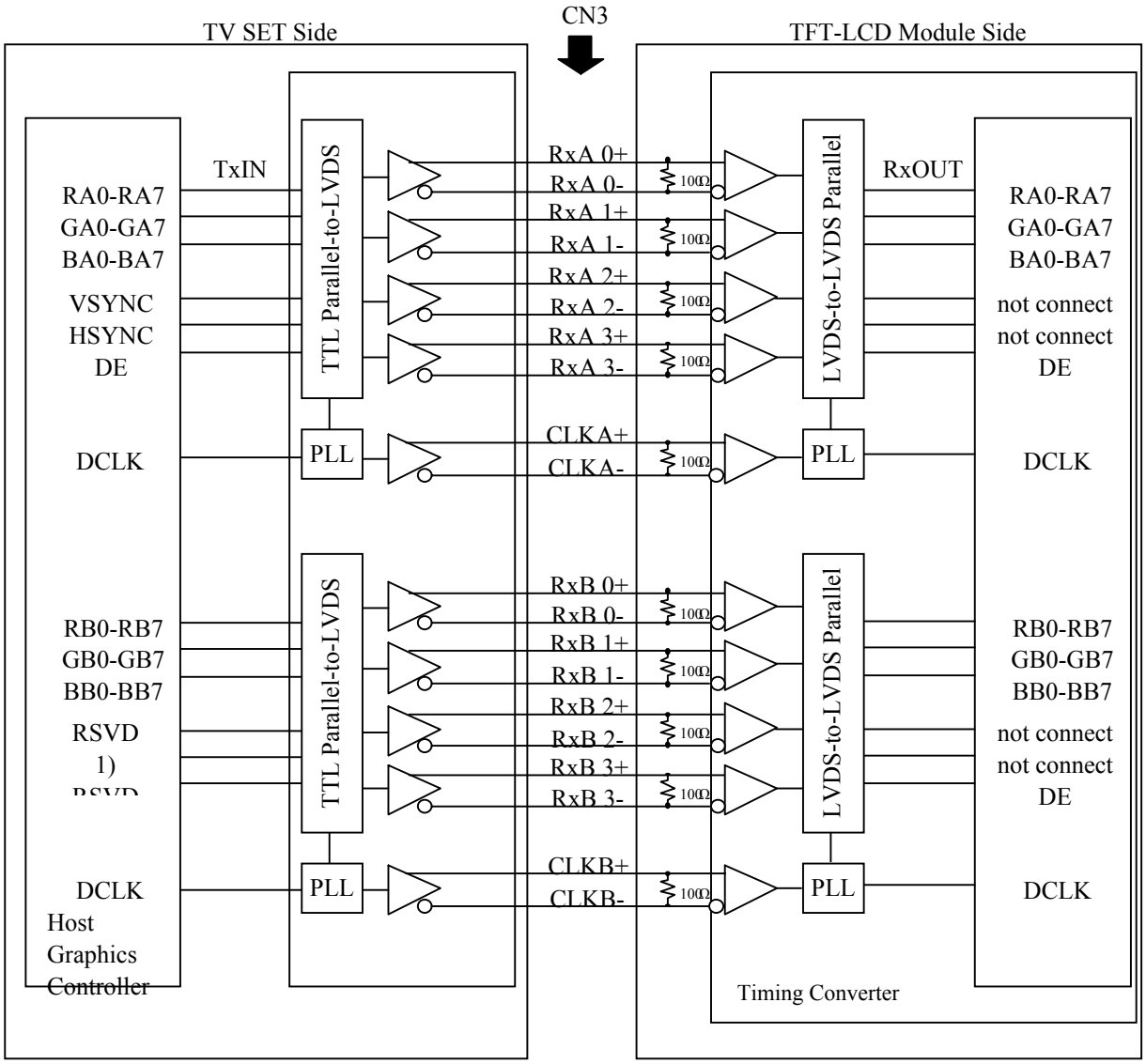
(Matching connector : JST PHR-14)

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	Vin	Power supply (Typ. +24.0V)	1)
2	Vin		
3	Vin		
4	Vin		
5	Vin		
6	Vss	GND (0V)	2)
7	Vss		
8	Vss		
9	Vss		
10	Vss		
11	FAIL	Status output (Normal:GND abnormal:open)	
12	ON/OFF	High : LAMP ON(3.3V) Low : LAMP OFF	
13	PWM	14pin low:0-3.3V pulse (120-240Hz ON duty 20-100%)	
14	SELECT	Low:external pwm dimming	

Note 1) All Vin pins shall be connected to +24.0V(Typ.).

2) All Vss pins shall be grounded. Metal bezel is internally connected to Vss.

4. 3 Block diagram of interface



RA0～RA7, RB0～RB7	: Pixel R Data	(7; MSB, 0; LSB)
GA0～GA7, GB0～GB7	: Pixel G Data	(7; MSB, 0; LSB)
BA0～BA7, BB0～BB7	: Pixel B Data	(7; MSB, 0; LSB)
DE	: Data Enable	

Note 1) The system must have the transmitter to drive the module.

2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

4. 4 LVDS interface

The LVDSSEL signal of CN3 pin No.7 specification is “L” or open.【LVDSSEL = L or open】

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		PIN	INPUT	TV Set	TFT-LCD	PIN	OUTPUT	INPUT
24bit	RA0/RB0	51	Tx IN0	TA OUT0+	RxA/B 0+	27	Rx OUT0	RA0/RB0
	RA1/RB1	52	Tx IN1			29	Rx OUT1	RA1/RB1
	RA2/RB2	54	Tx IN2			30	Rx OUT2	RA2/RB2
	RA3/RB3	55	Tx IN3			32	Rx OUT3	RA3/RB3
	RA4/RB4	56	Tx IN4			33	Rx OUT4	RA4/RB4
	RA5/RB5	3	Tx IN6	TA OUT0-	RxA/B 0-	35	Rx OUT6	RA5/RB5
	GA0/GB0	4	Tx IN7			37	Rx OUT7	GA0/GB0
	GA1/GB1	6	Tx IN8	TA OUT1+	RxA/B 1+	38	Rx OUT8	GA1/GB1
	GA2/GB2	7	Tx IN9			39	Rx OUT9	GA2/GB2
	GA3/GB3	11	Tx IN12			43	Rx OUT12	GA3/GB3
	GA4/GB4	12	Tx IN13			45	Rx OUT13	GA4/GB4
	GA5/GB5	14	Tx IN14			46	Rx OUT14	GA5/GB5
	BA0/BB0	15	Tx IN15	TA OUT1-	RxA/B 1-	47	Rx OUT15	BA0/BB0
	BA1/BB1	19	Tx IN18			51	Rx OUT18	BA1/BB1
	BA2/BB2	20	Tx IN19	TA OUT2+	RxA/B 2+	53	Rx OUT19	BA2/BB2
	BA3/BB3	22	Tx IN20			54	Rx OUT20	BA3/BB3
	BA4/BB4	23	Tx IN21			55	Rx OUT21	BA4/BB4
	BA5/BB5	24	Tx IN22			1	Rx OUT22	BA5/BB5
	HSYNC or RSVD1)	27	Tx IN24			3	Rx OUT24	HSYNC or RSVD1)
	VSYNC or RSVD1)	28	Tx IN25	TA OUT2-	RxA/B 2-	5	Rx OUT25	VSYNC or RSVD1)
	DE/DE	30	Tx IN26			6	Rx OUT26	DE/DE
	RA6/RB6	50	Tx IN27	TA OUT3+	RxA/B 3+	7	Rx OUT27	RA6/RB6
	RA7/RB7	2	Tx IN5			34	Rx OUT5	RA7/RB7
	GA6/GB6	8	Tx IN10			41	Rx OUT10	GA6/GB6
	GA7/GB7	10	Tx IN11			42	Rx OUT11	GA7/GB7
	BA6/BB6	16	Tx IN16			49	Rx OUT16	BA6/BB6
	BA7/BB7	18	Tx IN17	TA OUT3-	RxA/B 3-	50	Rx OUT17	BA7/BB7
	RSVD 1)	25	Tx IN23			2	Rx OUT23	RSVD 1)
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLKA/B IN+ RxCLKA/B IN-	26	RxCLK OUT	DCLK

RA0～RA7, RB0～RB7 : Pixel R Data (7; MSB, 0; LSB)
GA0～GA7, GB0～GB7 : Pixel G Data (7; MSB, 0; LSB)
BA0～BA7, BB0～BB7 : Pixel B Data (7; MSB, 0; LSB)
DE : Data Enable

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

The LVDSSEL signal of CN3 pin No.7 specification is “H”.【LVDSSEL = H】

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		PIN	INPUT	TV Set	TFT-LCD	PIN	OUTPUT	INPUT
24bit	RA2/RB2	51	Tx IN0	TA OUT0+	RxA/B 0+	27	Rx OUT0	RA2/RB2
	RA3/RB3	52	Tx IN1			29	Rx OUT1	RA3/RB3
	RA4/RB4	54	Tx IN2			30	Rx OUT2	RA4/RB4
	RA5/RB5	55	Tx IN3			32	Rx OUT3	RA5/RB5
	RA6/RB6	56	Tx IN4			33	Rx OUT4	RA6/RB6
	RA7/RB7	3	Tx IN6	TA OUT0-	RxA/B 0-	35	Rx OUT6	RA7/RB7
	GA2/GB2	4	Tx IN7			37	Rx OUT7	GA2/GB2
	GA3/GB3	6	Tx IN8	TA OUT1+	RxA/B 1+	38	Rx OUT8	GA3/GB3
	GA4/GB4	7	Tx IN9			39	Rx OUT9	GA4/GB4
	GA5/GB5	11	Tx IN12			43	Rx OUT12	GA5/GB5
	GA6/GB6	12	Tx IN13			45	Rx OUT13	GA6/GB6
	GA7/GB7	14	Tx IN14			46	Rx OUT14	GA7/GB7
	BA2/BB2	15	Tx IN15	TA OUT1-	RxA/B 1-	47	Rx OUT15	BA2/BB2
	BA3/BB3	19	Tx IN18			51	Rx OUT18	BA3/BB3
	BA4/BB4	20	Tx IN19	TA OUT2+	RxA/B 2+	53	Rx OUT19	BA4/BB4
	BA5/BB5	22	Tx IN20			54	Rx OUT20	BA5/BB5
	BA6/BB6	23	Tx IN21			55	Rx OUT21	BA6/BB6
	BA7/BB7	24	Tx IN22			1	Rx OUT22	BA7/BB7
	HSYNC or RSVD1)	27	Tx IN24			3	Rx OUT24	HSYNC or RSVD1)
	VSYNC or RSVD1)	28	Tx IN25	TA OUT2-	RxA/B 2-	5	Rx OUT25	VSYNC or RSVD1)
	DE/DE	30	Tx IN26			6	Rx OUT26	DE/DE
	RA0/RB0	50	Tx IN27	TA OUT3+	RxA/B 3+	7	Rx OUT27	RA0/RB0
	RA1/RB1	2	Tx IN5			34	Rx OUT5	RA1/RB1
	GA0/GB0	8	Tx IN10			41	Rx OUT10	GA0/GB0
	GA1/GB1	10	Tx IN11			42	Rx OUT11	GA1/GB1
	BA0/BB0	16	Tx IN16			49	Rx OUT16	BA0/BB0
	BA1/BB1	18	Tx IN17	TA OUT3-	RxA/B 3-	50	Rx OUT17	BA1/BB1
	RSVD 1)	25	Tx IN23			2	Rx OUT23	RSVD 1)
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLKA/B IN+ RxCLKA/B IN-	26	RxCLK OUT	DCLK

RA0～RA7, RB0～RB7 : Pixel R Data (7; MSB, 0; LSB)
GA0～GA7, GB0～GB7 : Pixel G Data (7; MSB, 0; LSB)
BA0～BA7, BB0～BB7 : Pixel B Data (7; MSB, 0; LSB)
DE : Data Enable

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

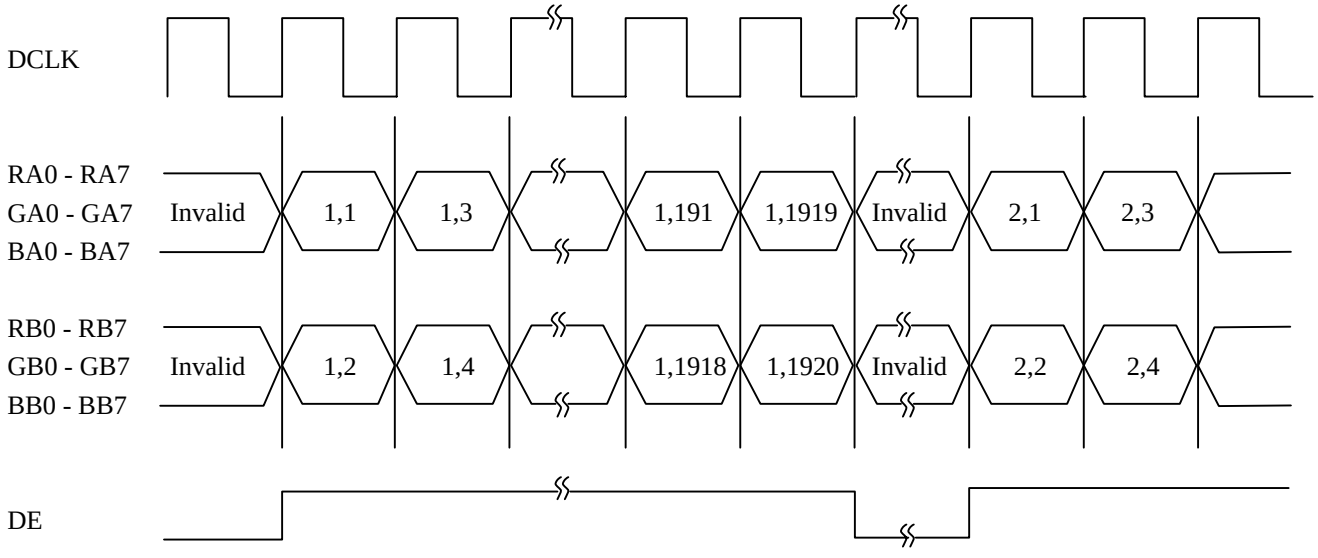
4. 5 Correspondence between input data and display image

Display data of adjacent one pixel is latched during one cycle of DCLK.

RA	(1,1) GA	BA	RB	(1,2) GB	BB

ODD pixel : RA0 - RA7 : R data
GA0 - GA7 : G data
BA0 - BA7 : B data
EVEN pixel RB0 - RB7 : R data
GB0 - GB7 : G data
BB0 - BB7 : B data

1 , 1	1 , 2	1 , 3	- -	1 , 1920
2 , 1	2 , 2	2 , 3	- -	2 , 1920
3 , 1	3 , 2	3 , 3	- -	3 , 1920
7080 , 1	1080 , 2	1080 , 3		1080 ,1920



4. 6 Relationship between display colors and input signals

Color		Input	Red Data										Green Data										Blue Data									
			R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
			MSB									LSB	MSB									LSB	MSB									LSB
Basic Color		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
		Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
		Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
		Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
		White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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		Red(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
		Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
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		Green(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
		Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Blue		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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		Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
		Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note 1) Definition of gray scale :

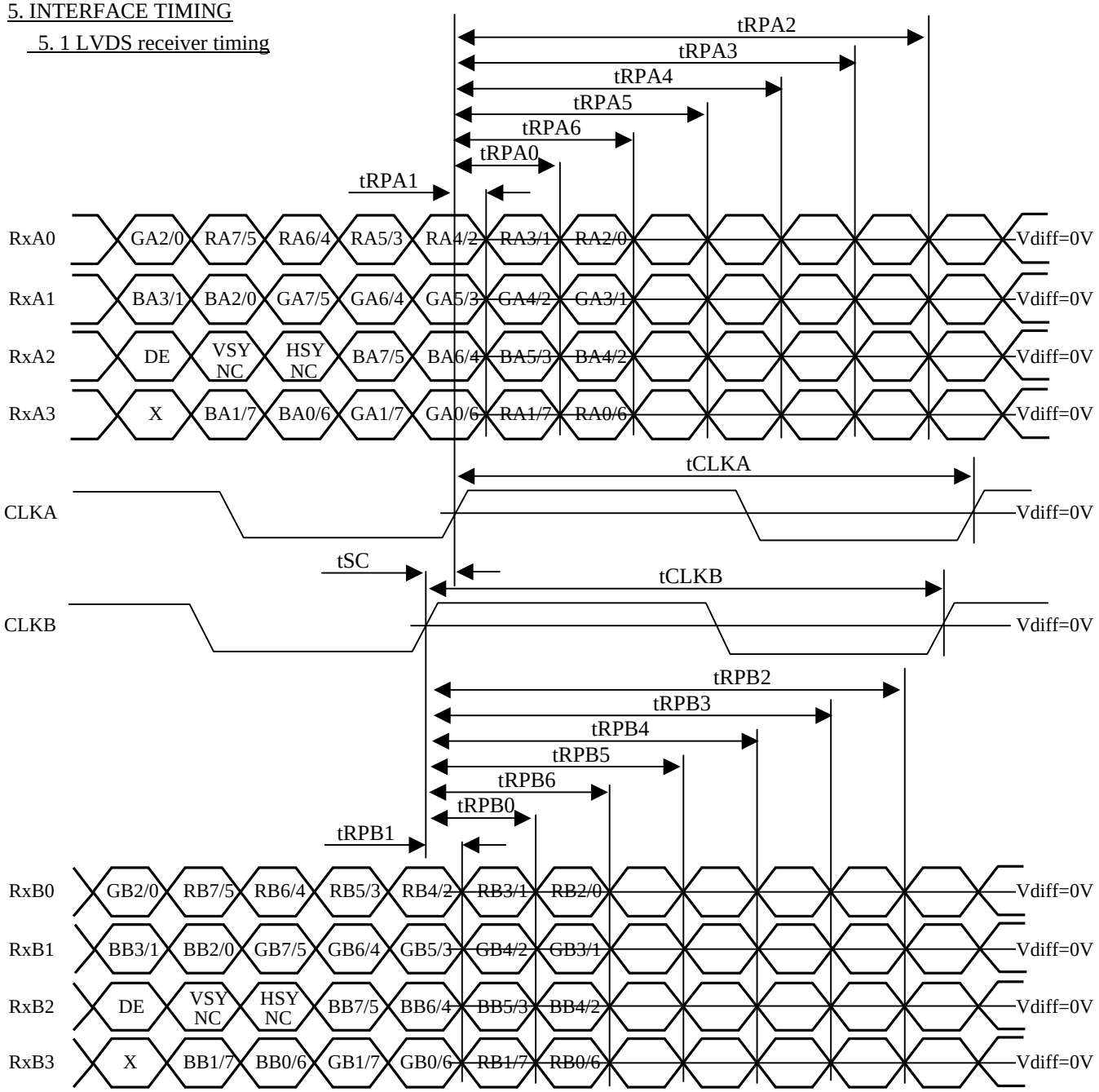
Color(n) · · · ·Number in parenthesis indicates gray scale level.

Larger n correspondsto brighter level.

2) Data : 1 : High, 0 : Low

5. INTERFACE TIMING

5. 1 LVDS receiver timing



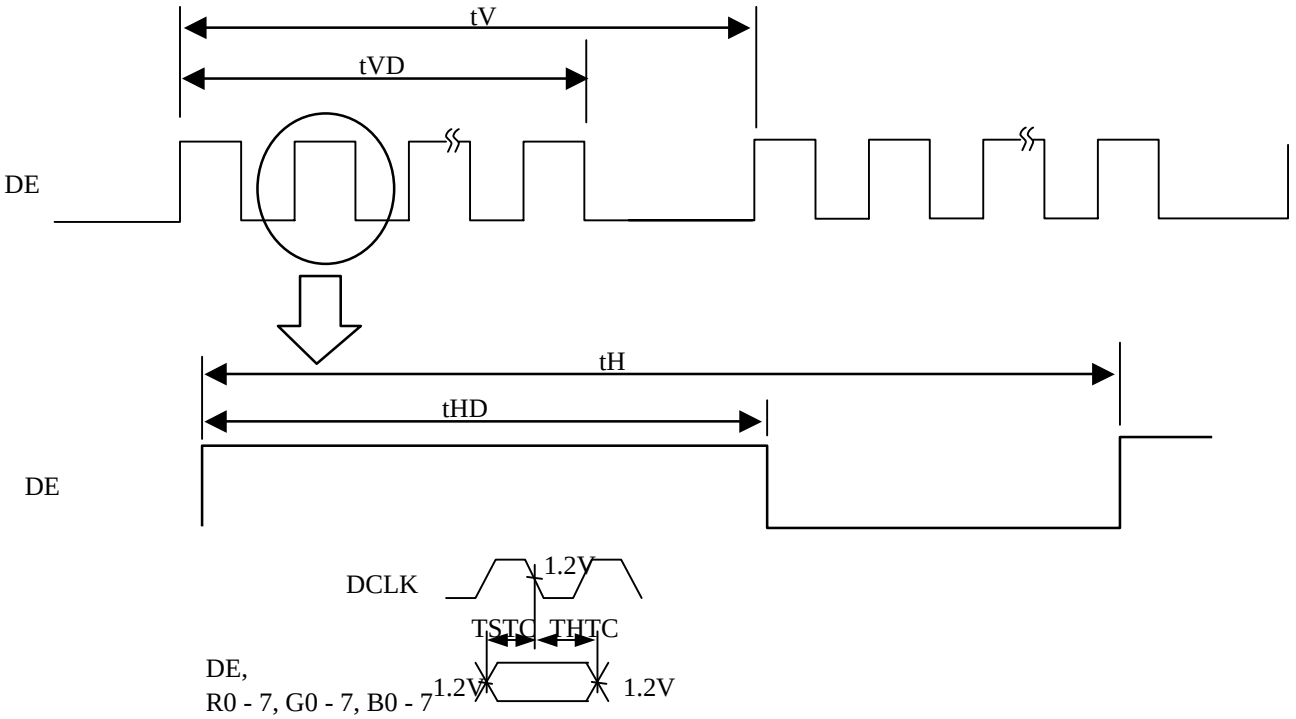
Rx*0=(Rx*0+)-(Rx*0-) Rx*3=(Rx*3+)-(Rx*3-)

Rx*1=(Rx*1+)-(Rx*1-) CLK=(CLK+)-(CLK-)

Rx*2=(Rx*2+)-(Rx*2-)

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
CLK	Frequency	DCLK	64.0	67.5	72.5	MHz	=1/tclk
	CLK Skew	tSC	- 4.0	0	+ 4.0	ns	
Rx*0 Rx*1 Rx*2 Rx*3	0 data position	tRP0	1/7tCLK - 0.4	1/7tCLK	1/7tCLK + 0.4	ns	
	1st data position	tRP1	- 0.4	0	+ 0.4		
	2nd data position	tRP2	6/7tCLK - 0.4	6/7tCLK	6/7tCLK + 0.4		
	3rd data position	tRP3	5/7tCLK - 0.4	5/7tCLK	5/7tCLK + 0.4		
	4th data position	tRP4	4/7tCLK - 0.4	4/7tCLK	4/7tCLK + 0.4		
	5th data position	tRP5	3/7tCLK - 0.4	3/7tCLK	3/7tCLK + 0.4		
	6th data position	tRP6	2/7tCLK - 0.4	2/7tCLK	2/7tCLK + 0.4		

5. 2 Syncronization signal timing



Note 1) Reference level for each timing signal is 1.2 V unless it is stated on the chart, high level voltage(VIH) and low level voltage(VIL) are defined as follows:

VIH ≧ 2.0 V VIL ≦ 0.8 V

2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.

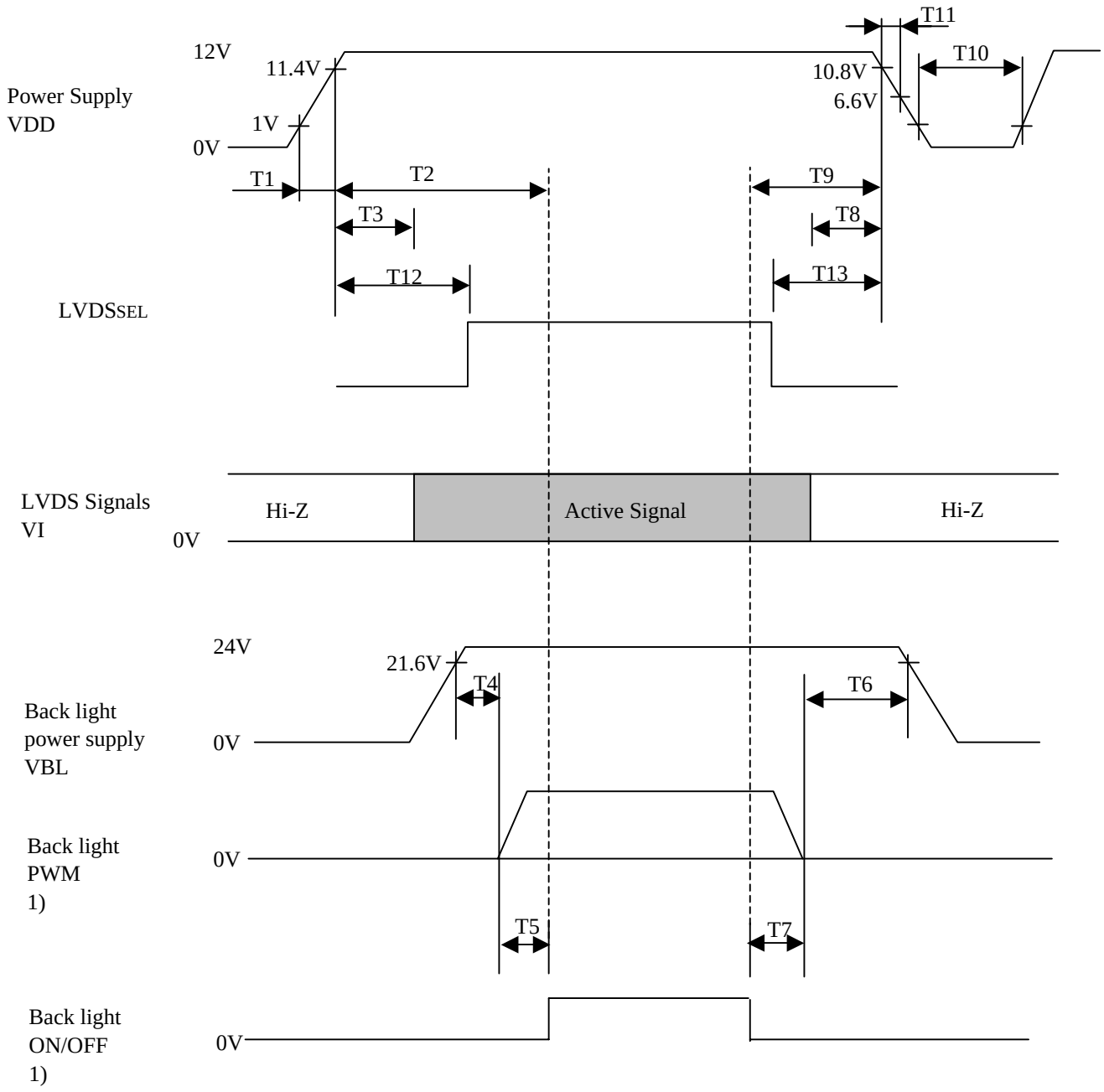
I)50Hz 2pxl/clk

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
DE	Vertical Frequency	fV	46	50	52	Hz	
	Vertical Period	tV	1265	1338	1435	tH	
	Vertical Valid	tVD		1080		tH	
	Horizontal Frequency	fH	65.1	66	69	kHz	
	Horizontal Period	tH	990	1009	1035	tCLK	
	Horizontal Valid	tHD		960		tCLK	

II)60Hz 2pxl/clk

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
DE	Vertical Frequency	fV	58	60	62	Hz	
	Vertical Period	tV	1090	1116	1150	tH	
	Vertical Valid	tVD		1080		tH	
	Horizontal Frequency	fH	65.1	66	69	kHz	
	Horizontal Period	tH	990	1009	1035	tCLK	
	Horizontal Valid	tHD		960		tCLK	

5.3 TIMING BETWEEN INTERFACE SIGNALS POWER SUPPLY



0.5	≦ T1 ≦	10	0	≦ T8	
350	≦ T2		0	≦ T9	
10	≦ T3		350	≦ T10	
200	≦ T4		10	< T11	
200	≦ T5		10	≦ T12	≦ T2-150
0	≦ T6		10	≦ T13	
0	≦ T7				

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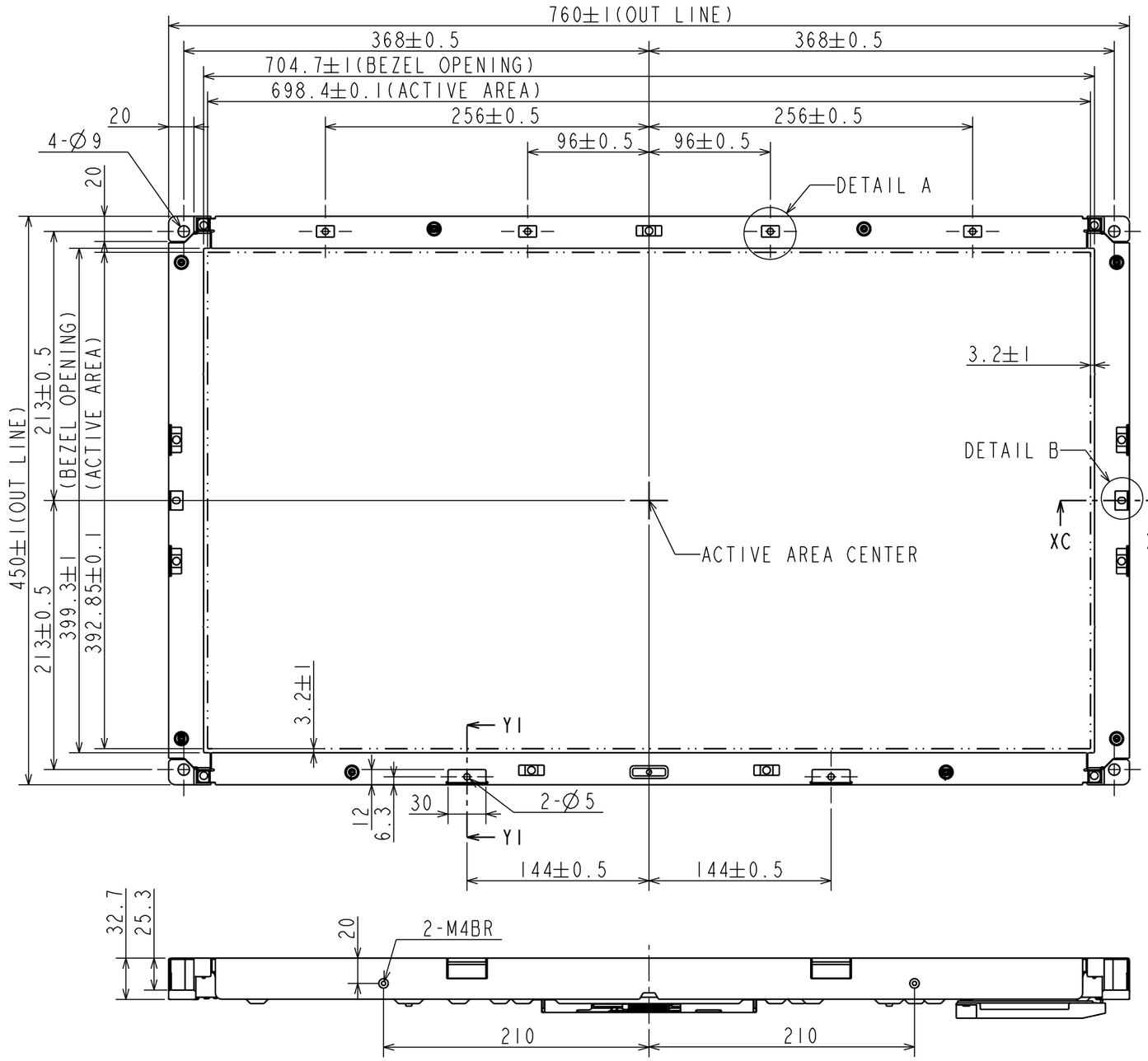
Unit : ms

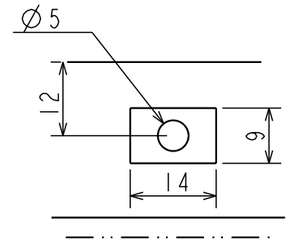
Note 1) In all periods, the backlight ON/OFF signal voltage and the PWM signal voltage should be lower than the backlight power supply voltage.

6. DIMENSIONAL OUT LINE

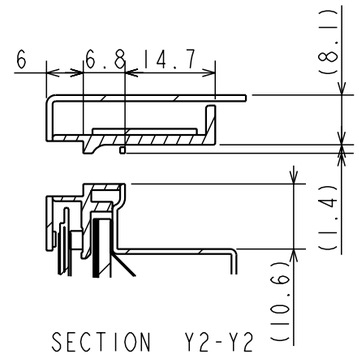
(1)FRONT VIEW

TENTATIVE

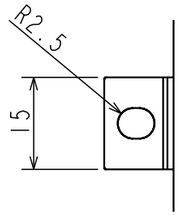




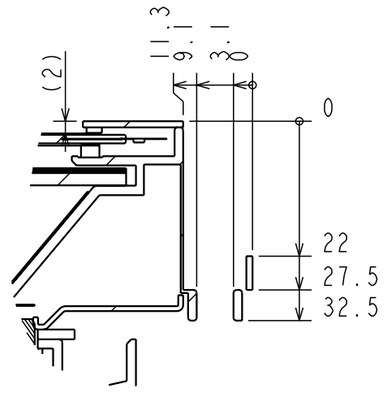
DETAIL A
(1:1)



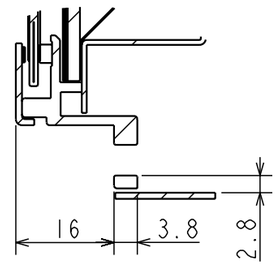
SECTION Y2-Y2



DETAIL B
(1:1)



SECTION XC-XC



SECTION YI-YI

Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ±0.8

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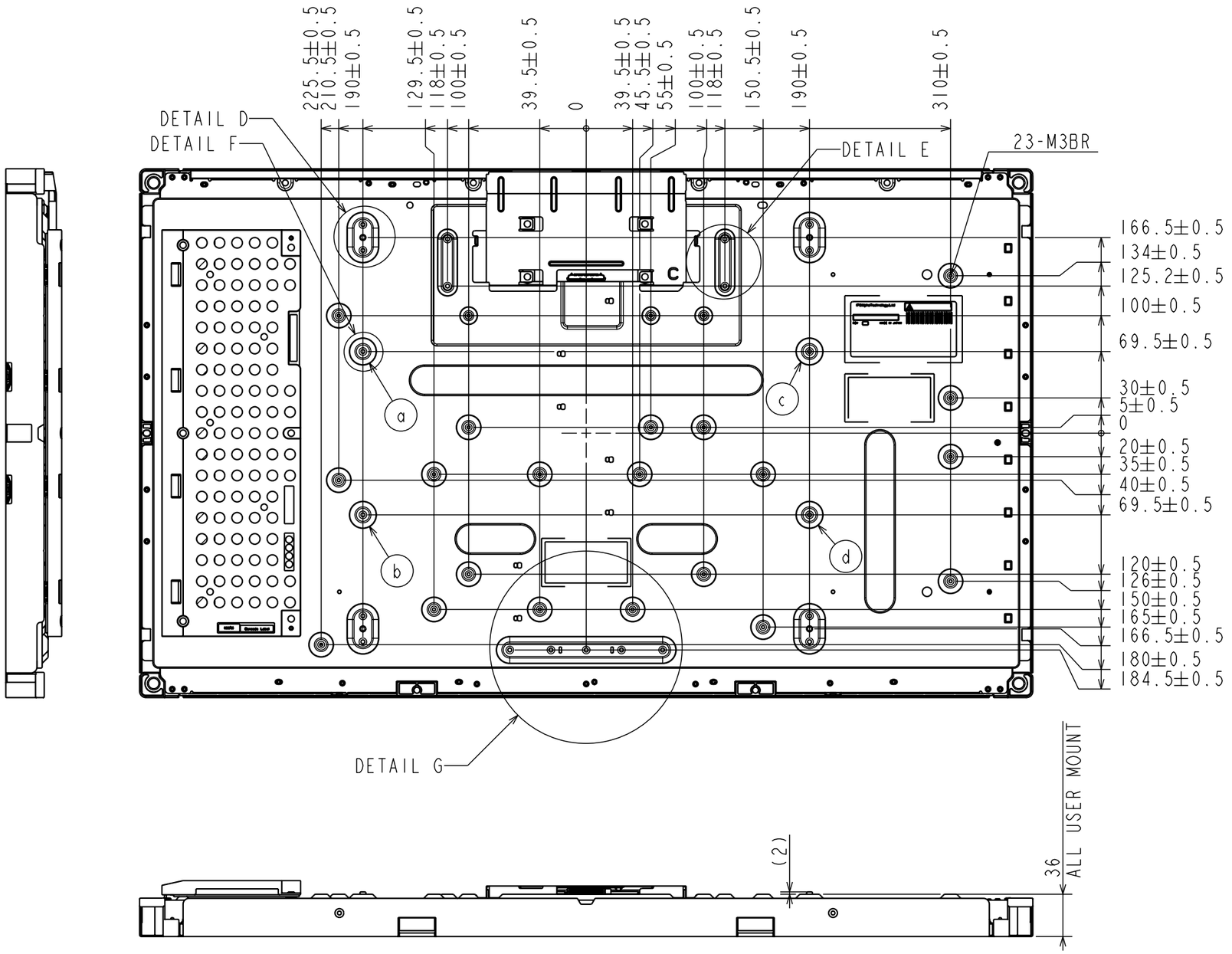
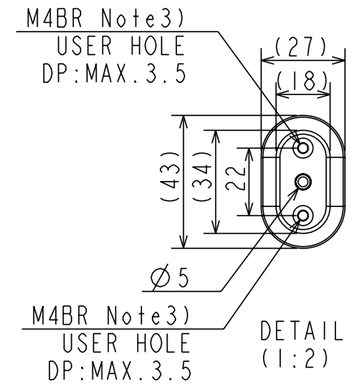
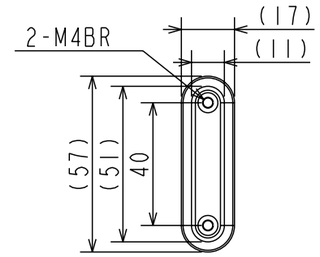
(2)BACK VIEW I

TENTATIVE

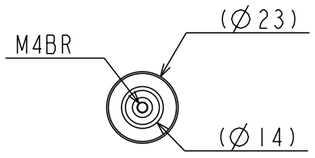




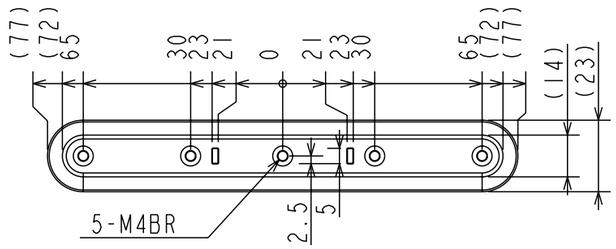
DETAIL D
(1:2)



DETAIL E
(1:2)



DETAIL F
(1:2)
(a,b,c,d)



DETAIL G
(1:2)

Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ±0.8
3) Torque MAX. 1.47N·m(15kgf·cm)

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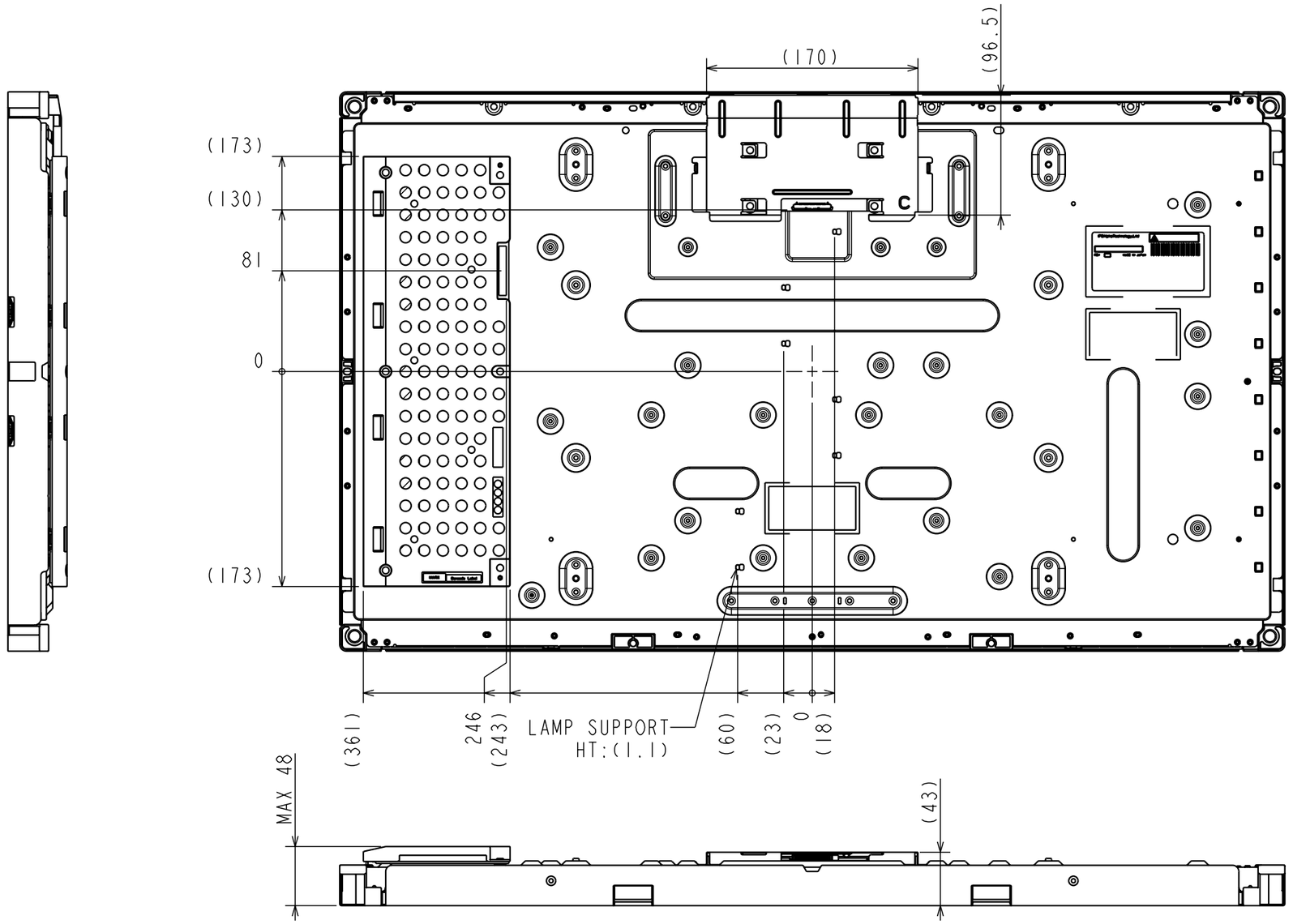
(3)BACK VIEW 2

TENTATIVE



Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ±0.8

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