Date:Mar. 29, 2007

STD-2700-1

TECHNICAL DATA

AX094F002F

CONTENTS

RECORD OF REVISION

Date	The upper section : Before revision The lower section : After revision		Summary
	Sheet No.	Page	

IPS Alpha Technology,Ltd.	Date	Mar. 29, 2007	Sheet No.	STD2700-1	Page	2-1/1

DESCRIPTION

The following specifications are applied to the following IPS-Pro module.
Note : Inverter for back light unit is built in this module.

Product Name : **AX094F002F**

General Specifications

Effective Display Area	: (H)819.36(V)460.89	(mm)
Number of Pixels	: (H)1,920×(V)1,080	(pixels)
Pixel Pitch	: (H)0.42675×(V)0.42675	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 178°, CR≧10)	
Input Signal	: 2-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 20 pcs. of EEFL	
External Dimensions	: (H)877 x (V)516.8 x (t)55.5	(mm)
Weight	: Typ 9,500	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1),5)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	14.7(1.5G)	m/s^2	3)
Shock	-	29.4(3G)	-	294(30G)	m/s^2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	1x	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 70℃ on the condition of operating.
The brightness of a EEFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≦40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta＞40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
However, it does not affect the characteristics and reliability of the product.

1.2 Electrical Absolute Maximum Ratings

(1)TFT Module Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	0	13.2	V	
Input Voltage for logic	V1	-0.3	3.6	V	1)
Electrostatic Durability	VESD0	±100		V	2),3)
	VESD1	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient：200pF-250Ω, Environmental：25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light Inverter Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Voltage	Vin	0	28.0	V	
ON/OFF Control Input Voltage	ON/OFF	-0.3	5.5	V	
Brightness Control Voltage	BRT	-0.3	5.5	V	
Error Signal Control	ERR	-0.3	5.5	V	

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

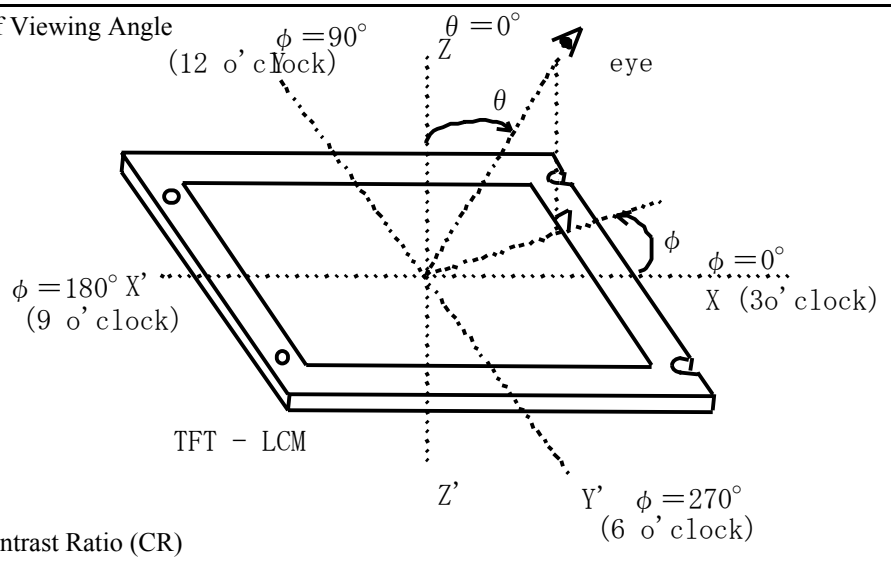
Measuring equipment：CS-1000A, or equivalent

Ambient Temperature =25℃、VDD=12.0V、f V=60Hz、

Vin=24V、 BRT=3.3V

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR	θ＝0° 1)	600	(900)	-	-	2)
Response Time	Rise	ton		-	8	20	ms	3)
	Fall	toff		-	6	20	ms	3)
Brightness of white		Bwh		350	(500)	-	cd/m^2	
Brightness uniformity		Buni		-	-	30	%	4)
Color Chromaticity (CIE)	Red	χ		0.62	0.65	0.68	-	【Gray scale =255】
		y		0.30	0.33	0.36		
	Green	χ		0.27	0.30	0.33		
		y		0.59	0.62	0.65		
	Blue	χ		0.12	0.15	0.18		
		y		0.04	0.065	0.10		
	White	χ		0.243	0.273	0.303		
		y		0.245	0.275	0.305		
Variation of Color Position (CIE)	Red	Δχ	θ＝+50° φ＝0°、90° 180°、270° 1)	-	-	0.04	-	5) 【Gray scale =255】
		Δ y		-	-	0.04		
	Green	Δχ		-	-	0.04		
		Δ y		-	-	0.04		
	Blue	Δχ		-	-	0.04		
		Δ y		-	-	0.04		
	White	Δχ		-	-	0.04		
		Δ y		-	-	0.04		
Contrast Ratio at 89°		CR89		10	-	-	-	Estimated value

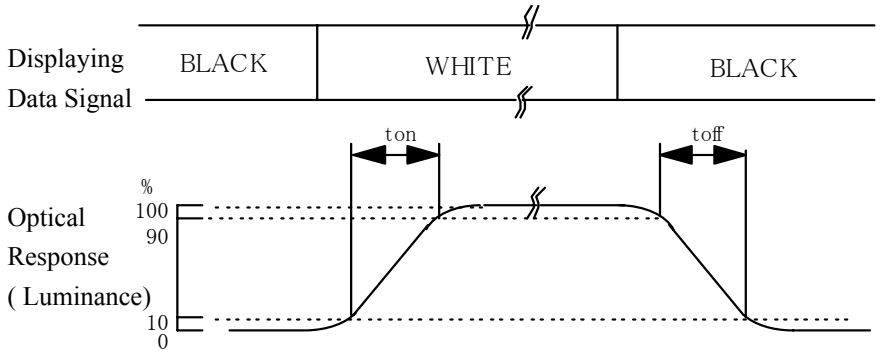
Note 1) Definition of Viewing Angle



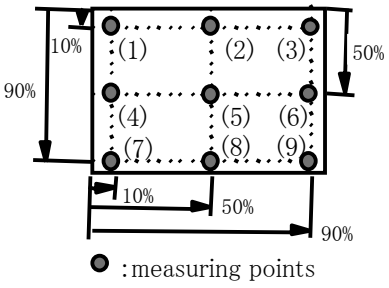
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformit Display pattern is white (255 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.



$$Buni = \frac{\left| \text{Bmax or Bmin - Bave} \right|}{\text{Bave}} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at θ =0°and at θ =50°& ϕ =0°90°180°270°.

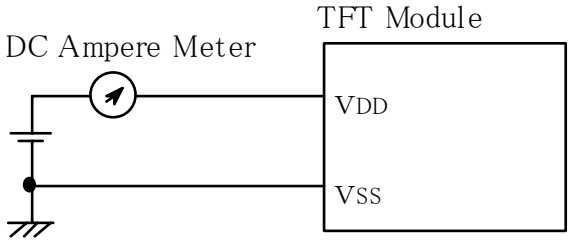
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD Module

Ta=25℃、Vss=0V

ITEM		SYSTEM	Min.	Typ	Max	単位	備考
Power supply Voltage		VDD	11.4	12.0	12.6	V	
Power supply Current		I DD	-	0.9	1.25	A	1),2)
Ripple voltage of power Supply		VDDR	-	-	150	mV	
LVDS select	High	LVDSSEL	2.2	2.5	3.6	V	
	Low		0	0	0.6	V	

Note 1)fV=60.0Hz, fCLK=66MHz, VDD=12.0V, and Display pattern is white.



2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of electrical circuit of module.

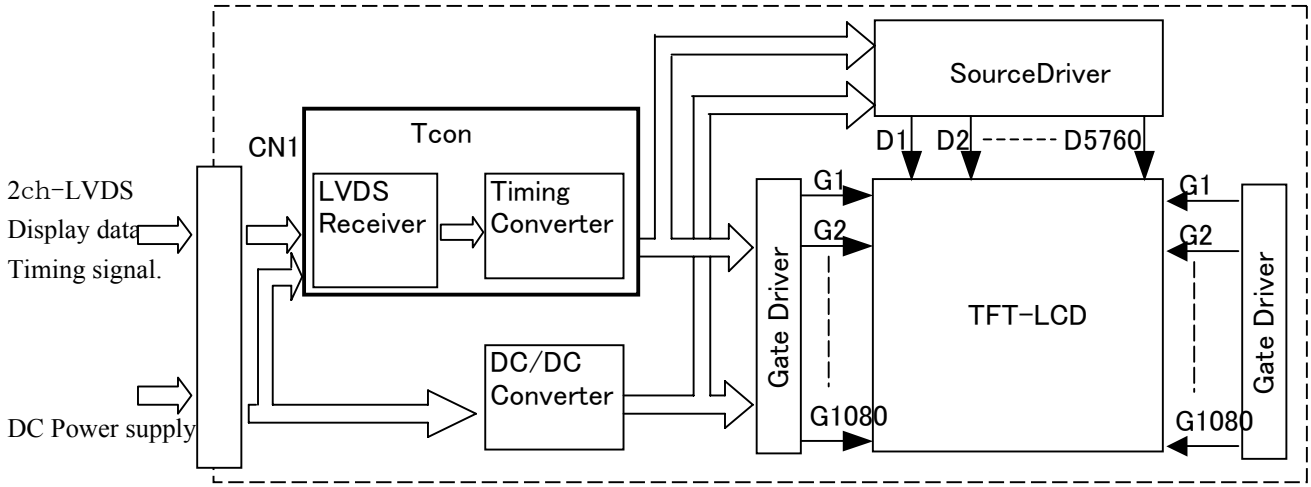
3.2 Back Light

ITEM		Symbol	Min.	Typ.	Max.	Unit	Notes
Input Voltage		VBL	21.6	24.0	26.4	V	
Input Current		IBL	-	(5.2)	6.5	A	VBL=24V, BRT=3.3V,3)
ON/OFF Control Voltage	ON	ON/OFF	2.2	-	5.5	V	
	OFF		-0.3	-	0.8	V	
Brigthness Control Input Voltage	Min. Brightness	BRT	-	0	-	V	
	Max. Brightness		3.0	-	3.3	V	
Output frequency		f	54.5	57.0	59.5	kHz	
Error Signal Control	Normal	ERR	-	0	0.8	V	
	Abnormal		Open Collector			V	

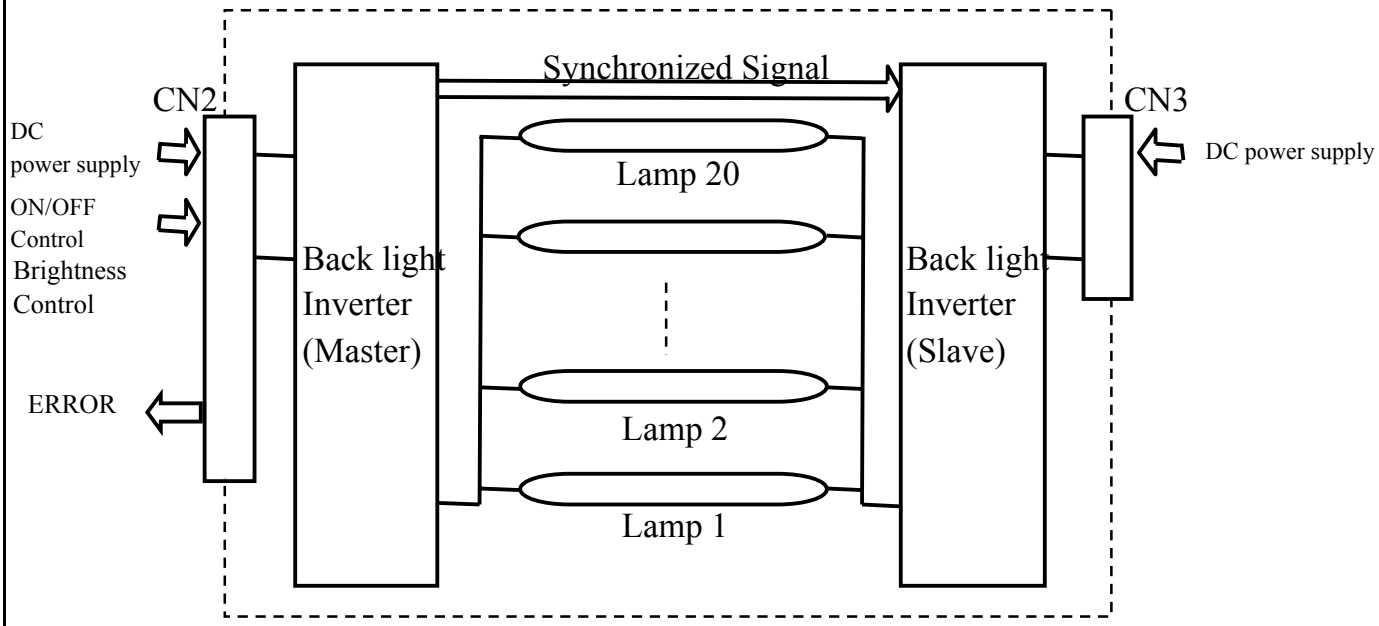
Note 3)This characteristics should be applied putting on the lamp about 60 minutes later with ambient temperature. (Ta=25℃±2℃)

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD MODULE

CN1:JAE FI-R51S-HF

(Matching connector : JAE FI-R51-HL)

PIN No.	SYMBOL	Description	Note
1	VSS	GND(0V)	2)
2	IC	Internally Connected , Keep Open	
3	IC		
4	IC		
5	IC		
6	IC		
7	LVDSSEL	Select LVDS Data Format	
8	IC	Internally Connected, Keep Open	
9	IC		
10	IC		
11	VSS	GND(0V)	2)
12	RxA0-	ODD Pixel Data	3)
13	RxA0+		
14	RxA1-	ODD Pixel Data	3)
15	RxA1+		
16	RxA2-	ODD Pixel Data	3)
17	RxA2+		
18	VSS	GND(0V)	2)
19	CLKA-	ODD Pixel Clock	3)
20	CLKA+		
21	VSS	GND(0V)	2)
22	RxA3-	ODD Pixel Data	3)
23	RxA3+		
24	IC	Internally Connected, Keep Open	
25	IC		
26	VSS	GND(0V)	2)
27	VSS		

PIN No.	SYMBOL	Description	Note
28	RxB0-	EVEN Pixel Data	3)
29	RxB0+		
30	RxB1-	EVEN Pixel Data	3)
31	RxB1+		
32	RxB2-	EVEN Pixel Data	3)
33	RxB2+		
34	VSS	GND(0V)	2)
35	CLKB-	EVEN Pixel Clock	3)
36	CLKB+		
37	VSS	GND(0V)	2)
38	RxB3-	EVEN Pixel Data	3)
39	RxB3+		
40	IC	Internally Connected, Keep Open	
41	IC		
42	VSS	GND(0V)	2)
43	VSS		
44	VSS		
45	VSS		
46	VSS		
47	NC	No Connection	
48	VDD	Power Supply (typ.+12V)	1)
49	VDD		
50	VDD		
51	VDD		

Notes 1) All VDD pins shall be connected to +12.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) Rx n+ and Rx n- (n=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

5. 2 BACK-LIGHT UNIT

CN2:JST S14B-PH-SM3-TF(LF)

(Matching connecor : JST PHR-14)

Pin No.	SYMBOL	Description	Note
1	VIN	Power Supply (typ.+24.0V)	1)
2	VIN		
3	VIN		
4	VIN		
5	VIN		
6	VSS	GND(0V)	2)
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	ERR	Error Signal Control	
12	ON/OFF	High:Lamp ON, Low:Lamp OFF	
13	BRT	Brightness Control	
14	IC	Internally Connected, Keep Open	

Notes 1) All VIN pins shall be connected to +24.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

CN3:JST S12B-PH-SM3-TF(LF)

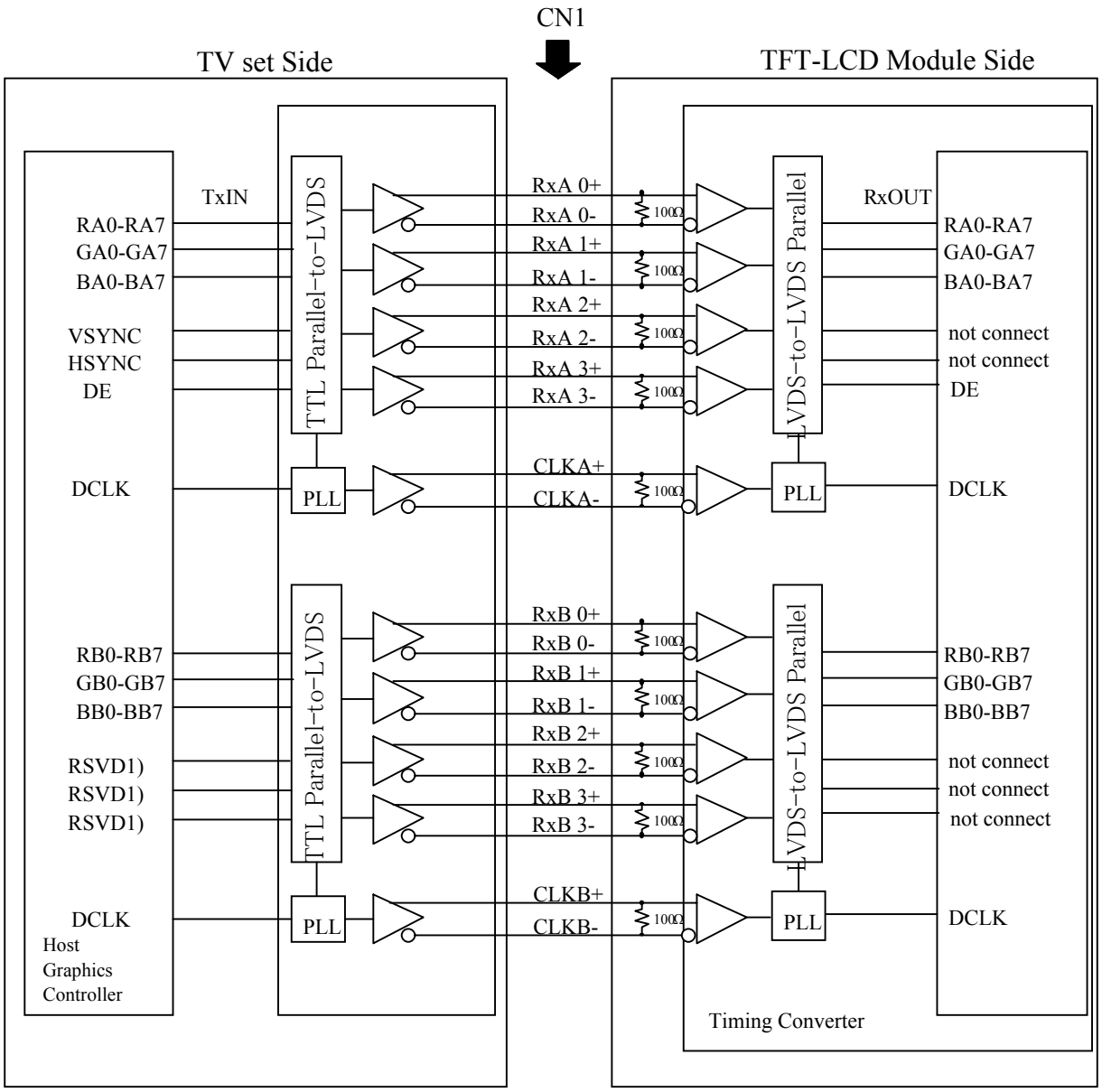
(Matching connecor : JST PHR-12)

Pin No.	SYMBOL	Description	Note
1	VIN	Power Supply (typ.+24.0V)	1)
2	VIN		
3	VIN		
4	VIN		
5	VIN		
6	VSS	GND(0V)	2)
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	NC	NC	
12	NC	NC	

Notes 1) All VIN pins shall be connected to +24.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

5.3 BLOCK DIAGRAM OF INTERFACE



RA0～RA7, RB0～RB7 : Pixel R Data (7; MSB, 0; LSB)
GA0～GA7, RB0～RB7 : Pixel G Data (7; MSB, 0; LSB)
BA0～BA7, BB0～BB7 : Pixel B Data (7; MSB, 0; LSB)
DE : Data Enable

Notes 1) The system must have the transmitter to drive the module.
2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

The 7st LVDSSEL signal of the connector pin specification is “L”. 【LVDSSEL = L】

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		PIN	INPUT	TV Set	TFT-LCD	PIN	OUTPUT	INPUT
24bit	RA0/RB0	51	Tx IN0	TA OUT0+	Rx 0+	27	Rx OUT0	RA0/RB0
	RA1/RB1	52	Tx IN1			29	Rx OUT1	RA1/RB1
	RA2/RB2	54	Tx IN2			30	Rx OUT2	RA2/RB2
	RA3/RB3	55	Tx IN3			32	Rx OUT3	RA3/RB3
	RA4/RB4	56	Tx IN4			33	Rx OUT4	RA4/RB4
	RA5/RB5	3	Tx IN6	TA OUT0-	Rx 0-	35	Rx OUT6	RA5/RB5
	GA0/GB0	4	Tx IN7			37	Rx OUT7	GA0/GB0
	GA1/GB1	6	Tx IN8	TA OUT1+	Rx 1+	38	Rx OUT8	GA1/GB1
	GA2/GB2	7	Tx IN9			39	Rx OUT9	GA2/GB2
	GA3/GB3	11	Tx IN12			43	Rx OUT12	RA3/RB3
	GA4/GB4	12	Tx IN13			45	Rx OUT13	RA4/RB4
	GA5/GB5	14	Tx IN14			46	Rx OUT14	RA5/RB5
	BA0/BB0	15	Tx IN15	TA OUT1-	Rx 1-	47	Rx OUT15	RA0/RB0
	BA1/BB1	19	Tx IN18			51	Rx OUT18	RA1/RB1
	BA2/BB2	20	Tx IN19	TA OUT2+	Rx 2+	53	Rx OUT19	RA2/RB2
	BA3/BB3	22	Tx IN20			54	Rx OUT20	RA3/RB3
	BA4/BB4	23	Tx IN21			55	Rx OUT21	RA4/RB4
	BA5/BB5	24	Tx IN22			1	Rx OUT22	RA5/RB5
	HSYNC/RSVD1)	27	Tx IN24			3	Rx OUT24	not connect
	VSYNC/RSVD1)	28	Tx IN25	TA OUT2-	Rx 2-	5	Rx OUT25	not connect
	DE/RSVD1)	30	Tx IN26			6	Rx OUT26	DE/not connect
	RA6/RB6	50	Tx IN27	TA OUT3+	Rx 3+	7	Rx OUT27	RA6/RB6
	RA7/RB7	2	Tx IN5			34	Rx OUT5	RA7/RB7
	GA6/GB6	8	Tx IN10			41	Rx OUT10	GA6/GB6
	GA7/GB7	10	Tx IN11			42	Rx OUT11	GA7/GB7
	BA6/BB6	16	Tx IN16			49	Rx OUT16	BA6/BB6
	BA7/BB7	18	Tx IN17	TA OUT3-	Rx 3-	50	Rx OUT17	BA7/BB7
	RSVD 1)	25	Tx IN23			2	Rx OUT23	RSVD 1)
	DCLK	31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK
				TxCLK OUT-	RxCLK IN-			

RA0～RA7, RB0～RB7 :Pixel R Data (7;MSB, 0;LSB)
GA0～GA7, GB0～GB7 :Pixel G Data (7;MSB, 0;LSB)
BA0～BA7, BB0～BB7 :Pixel B Data (7;MSB, 0;LSB)
DE :Data Enable

Notes 1)RSVD(reserved)pins on the transmitter shall be tied to"H"or"L".

5.4 LVDS INTERFACE

The 7st LVDSSEL signal of the connector pin specification is “H”. 【LVDSSEL = H】

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		PIN	INPUT	TV Set	TFT-LCD	PIN	OUTPUT	INPUT
24bit	RA2/RB2	51	Tx IN0	TA OUT0+	RxA/B 0+	27	Rx OUT0	RA2/RB2
	RA3/RB3	52	Tx IN1			29	Rx OUT1	RA3/RB3
	RA4/RB4	54	Tx IN2			30	Rx OUT2	RA4/RB4
	RA5/RB5	55	Tx IN3			32	Rx OUT3	RA5/RB5
	RA6/RB6	56	Tx IN4			33	Rx OUT4	RA6/RB6
	RA7/RB7	3	Tx IN6	TA OUT0-	RxA/B 0-	35	Rx OUT6	RA7/RB7
	GA2/GB2	4	Tx IN7			37	Rx OUT7	GA2/GB2
	GA3/GB3	6	Tx IN8	TA OUT1+	Rx A/B1+	38	Rx OUT8	GA3/GB3
	GA4/GB4	7	Tx IN9			39	Rx OUT9	GA4/GB4
	GA5/GB5	11	Tx IN12			43	Rx OUT12	GA5/GB5
	GA6/GB6	12	Tx IN13			45	Rx OUT13	GA6/GB6
	GA7/GB7	14	Tx IN14			46	Rx OUT14	GA7/GB7
	BA2/BB2	15	Tx IN15	TA OUT1-	RxA/B 1-	47	Rx OUT15	BA2/BB2
	BA3/BB3	19	Tx IN18			51	Rx OUT18	BA3/BB3
	BA4/BB4	20	Tx IN19	TA OUT2+	Rx A/B2+	53	Rx OUT19	BA4/BB4
	BA5/BB5	22	Tx IN20			54	Rx OUT20	BA5/BB5
	BA6/BB6	23	Tx IN21			55	Rx OUT21	BA6/BB6
	BA7/BB7	24	Tx IN22			1	Rx OUT22	BA7/BB7
	HSYNC/RSVD1)	27	Tx IN24	TA OUT2-	Rx A/B2-	3	Rx OUT24	HSYNC/RSVD1)
	VSYNC/RSVD1)	28	Tx IN25			5	Rx OUT25	VSYNC/RSVD1)
	DE/RSVD1)	30	Tx IN26			6	Rx OUT26	DE/RSVD1)
	RA0/RB0	50	Tx IN27	TA OUT3+	RxA/B 3+	7	Rx OUT27	RA0/RB0
	RA1/RB1	2	Tx IN5			34	Rx OUT5	RA1/RB1
	GA0/GB0	8	Tx IN10			41	Rx OUT10	GA0/GB0
	GA1/GB1	10	Tx IN11			42	Rx OUT11	GA1/GB1
	BA0/BB0	16	Tx IN16			49	Rx OUT16	BA0/BB0
	BA1/BB1	18	Tx IN17	TA OUT3-	Rx A/B3-	50	Rx OUT17	BA1/BB1
	RSVD 1)	25	Tx IN23			2	Rx OUT23	RSVD 1)
	DCLK	31	TxCLK IN	TxCLK OUT+	RxCLKA/B IN+	26	RxCLK OUT	DCLK
				TxCLK OUT-	RxCLKA/B IN-			

RA0～RA7, RB0～RB7 :Pixel R Data (7;MSB, 0;LSB)
GA0～GA7, GB0～GB7 :Pixel G Data (7;MSB, 0;LSB)
BA0～BA7, BB0～BB7 :Pixel B Data (7;MSB, 0;LSB)
DE :Data Enable

Notes 1)RSVD(reserved)pins on the transmitter shall be tied to"H"or"L".

5.5 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

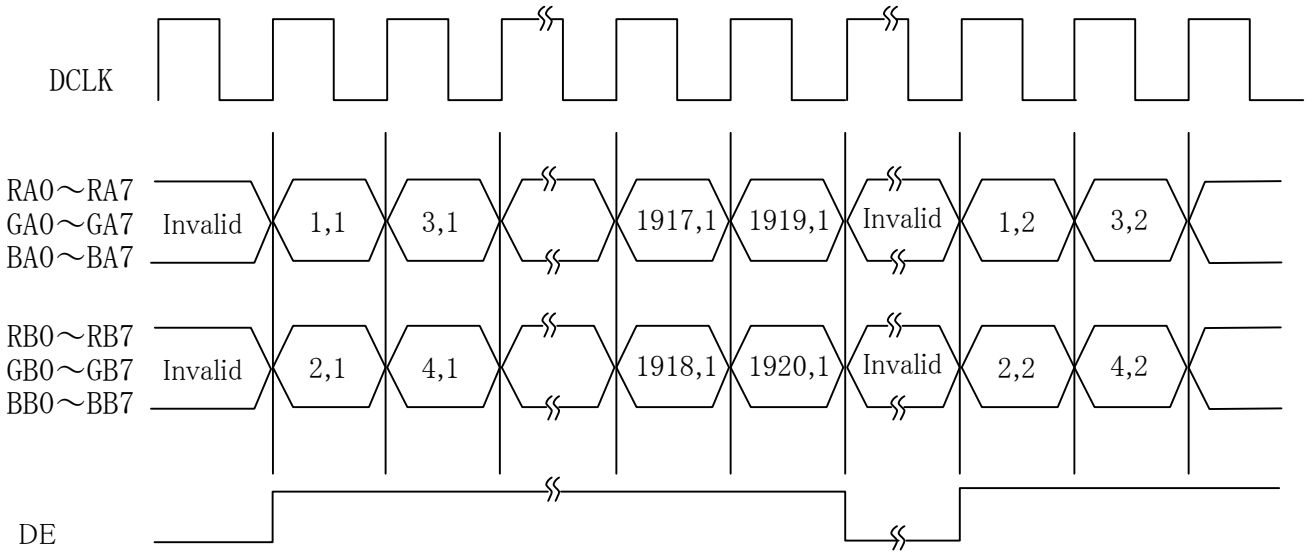
Display data of adjacent one pixel is latched during one cycle of DCLK.

	(1,1)			(1,2)	
RA	GA	BA	RB	GB	BB

odd pixel : RA0～RA7 :R data
GA0～GA7 :G data
BA0～BA7 :B data

Even pixel: RB0～RB7 :R data
GB0～GB7 :G data
BB0～BB7 :B data

1, 1	1, 2	1, 3	----------	1, 1920
2, 1	2, 2	2, 3	----------	2, 1920
3, 1	3, 2	3, 3	----------	3, 1920
⋮	⋮	⋮		⋮
1080, 1	1080, 2	1080, 3	----------	1080, 1920



5.6 RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input	Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

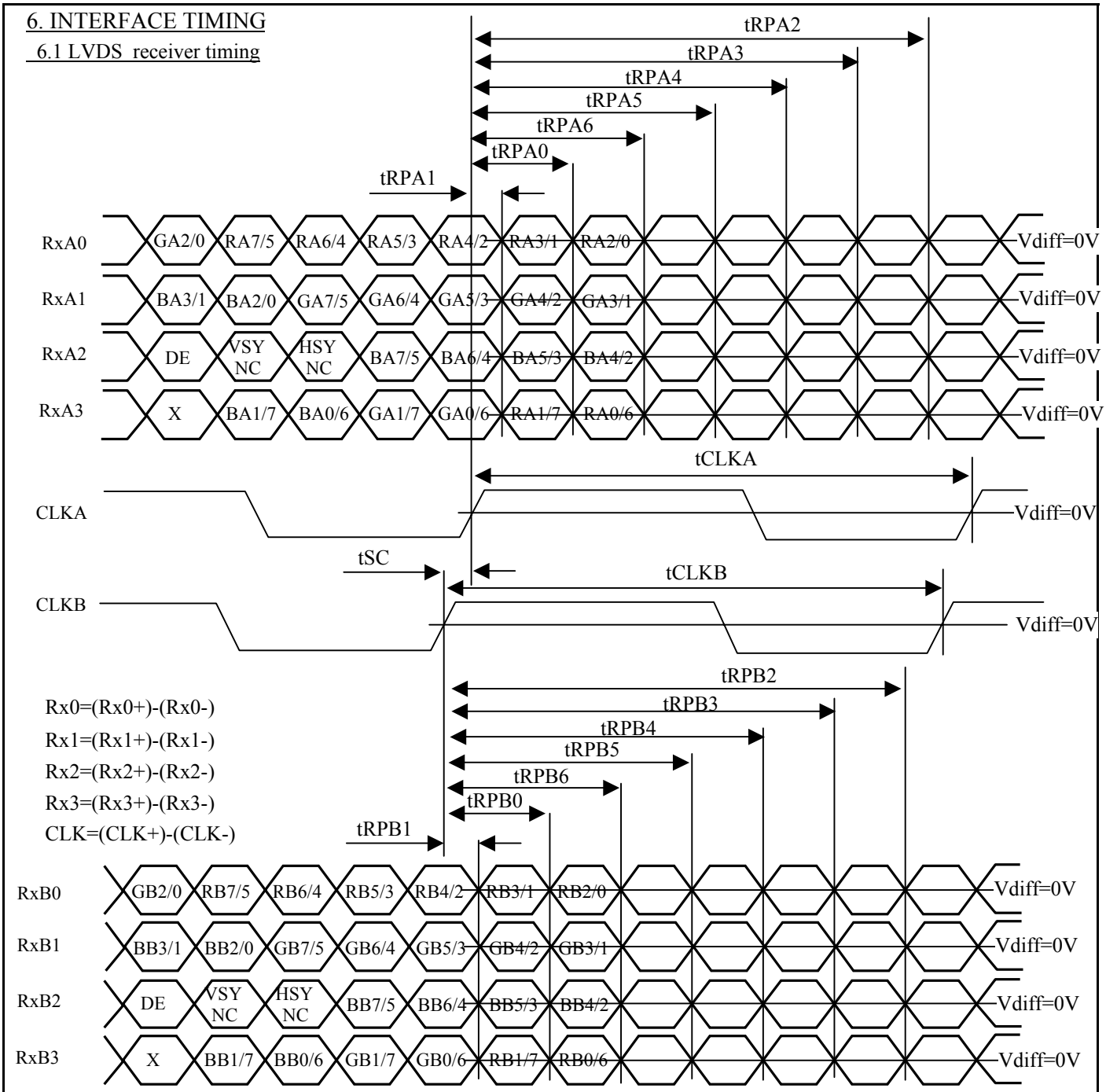
Notes 1) Definition of gray scale:

Color(n) ・・・・Number in parenthesis indicates gray scale level. Larger n corresponds to brighter level.

2) Data: 1:High, 0:Low

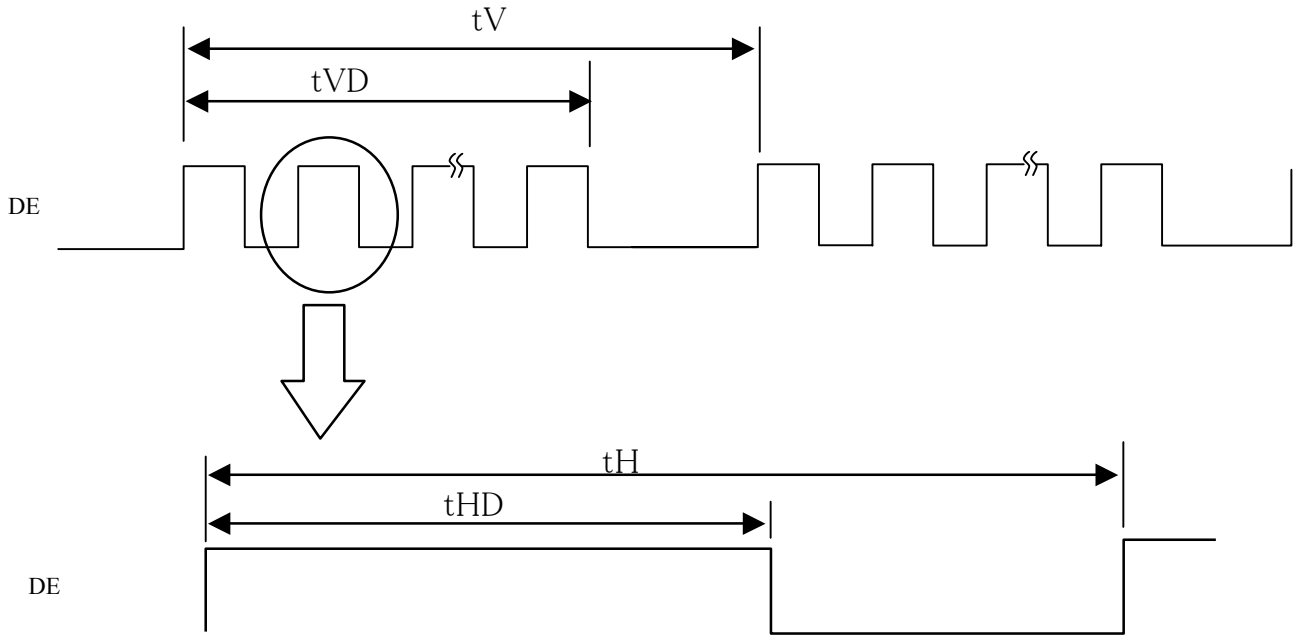
6. INTERFACE TIMING

6.1 LVDS receiver timing



Item		Symbol	Min	Typ	Max	Unit	Note
CLK	Frequency	DCLK	65	66	67.5	MHz	=1/tclk
	CLK Skew	tSC	-4.0	0	4.0	ns	
	0 data position	tRP0	1/7tCLK - 0.4	1/7tCLK	1/7tCLK +0.4	ns	
	1st data position	tRP1	-0.4	0	+0.4		
Rx*0	2nd data position	tRP2	2/7tCLK -0.4	2/7tCLK	2/7tCLK +0.4		
Rx*1	3rd data position	tRP3	3/7tCLK -0.4	3/7tCLK	3/7tCLK + 0.4		
Rx*2	4th data position	tRP4	4/7tCLK - 0.4	4/7tCLK	4/7tCLK +0.4		
Rx*3	5th data position	tRP5	5/7tCLK - 0.4	5/7tCLK	5/7tCLK + 0.4		
	6th data position	tRP6	6/7tCLK - 0.4	6/7tCLK	6/7tCLK + 0.4		

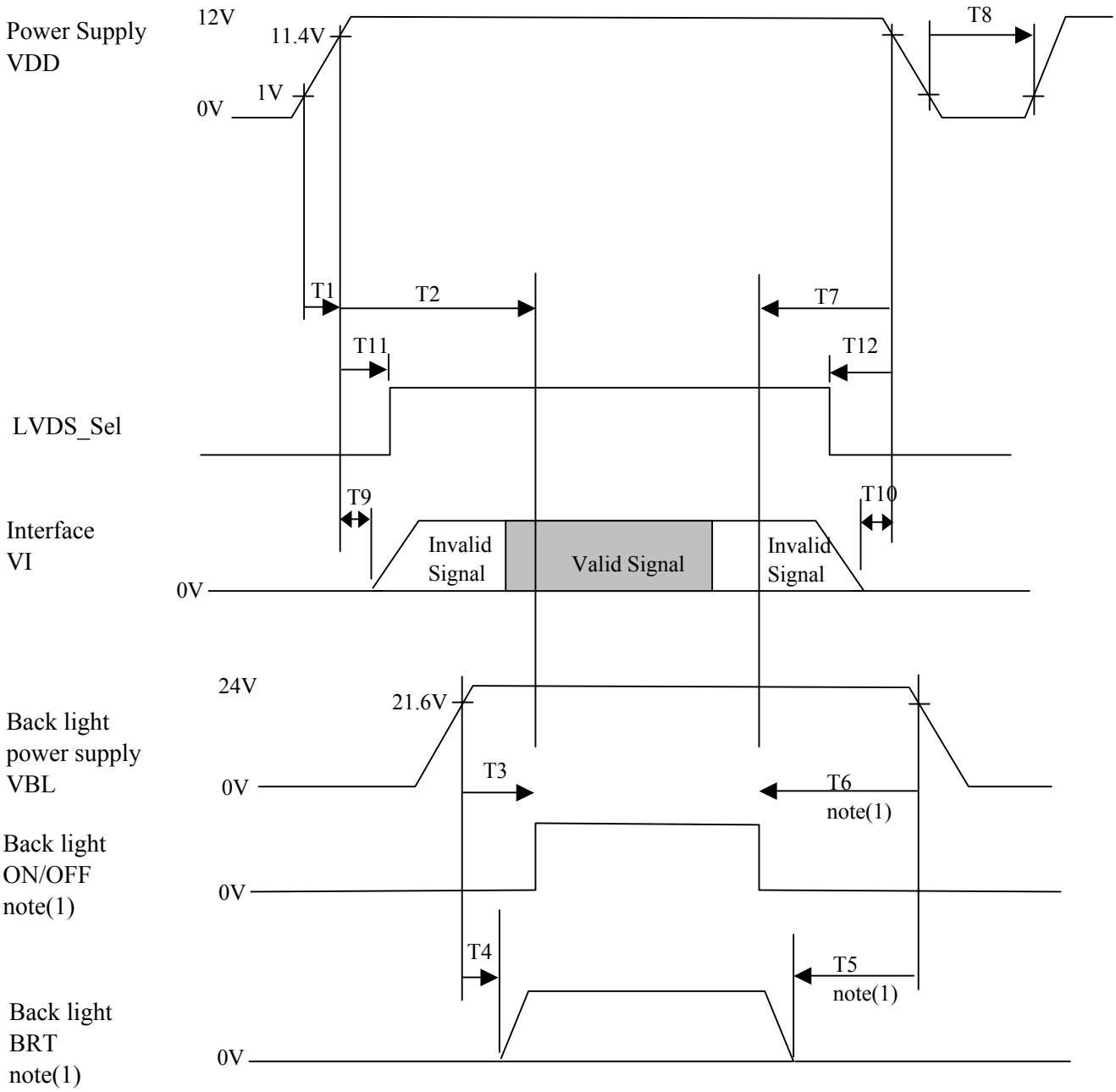
6.2 SYNCRONIZATION SIGNAL TIMING



2pxl/clk

Item		Symbol	Min	Typ	Max	Unit	Note
DE	Horizontal Frequency	fH	63	66	68	kHz	
	Horizontal Period	tH	990	1000	1035	tCLK	
	Horizontal Valid	tHD		960		tCLK	
	Vertical Frequency	fV	48	60	62	Hz	
	Vertical Period	tV	1090	1100	1350	tH	
	Vertical Valid	tVD		1080		tH	

6.3 TIMING BETWEEN INTERFACE SIGNALS POWER SUPPLY



0 ≦ T1 ≦ 10	-100 ≦ T5	10 ≦ T9	10 ≦ T11 ≦T2-150
350 ≦ T2	-100 ≦ T6	0 ≦ T10	0 ≦ T12
0 ≦ T3	0 ≦ T7		
1 ≦ T4	350 ≦ T8		

Unit : ms

Note 1) In all periods, the backlight ON/OFF signal voltage and the BRT signal voltage should be lower than the backlight power supply voltage.