2A Sink/Source Bus Termination Regulator

❖ GENERAL DESCRIPTION

The AX1250ES is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage cab be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

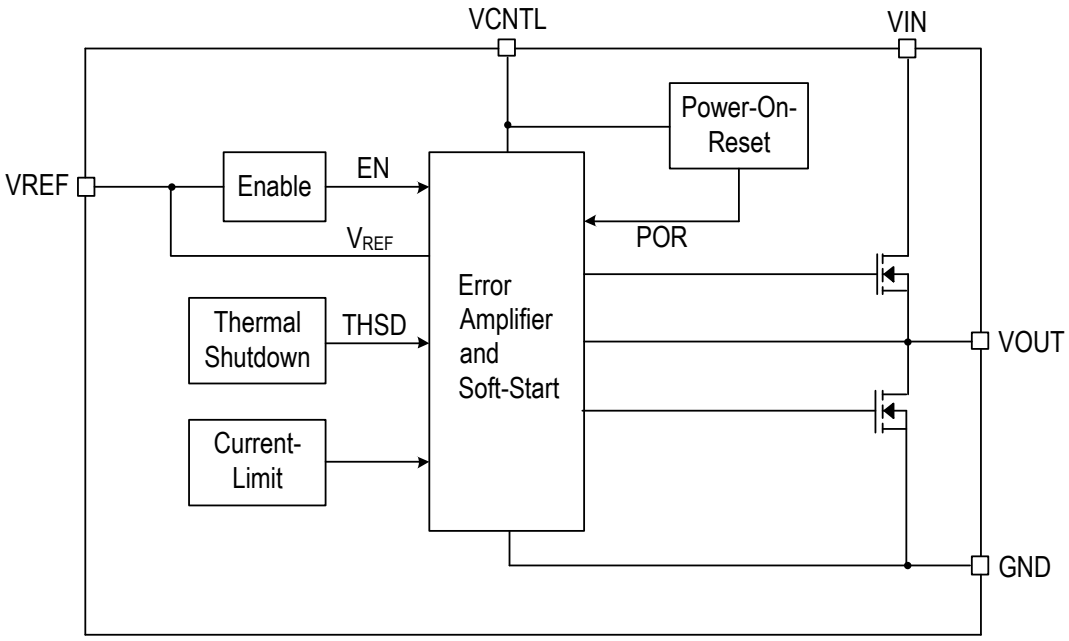
The AX1250ES also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The AX1250ES are available in the SOP-8L-EP (Exposed Pad) surface mount packages.

❖ FEATURES

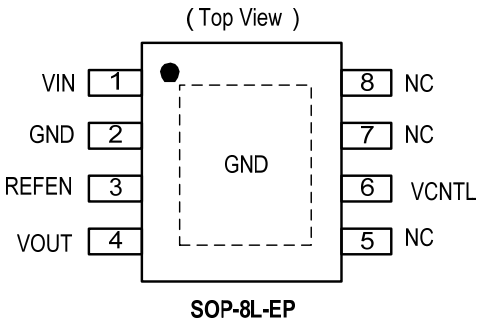
- Ideal for DDR-I, DDR-II and DDR-III VTT Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Voltage traces REFEN Pin Voltage.
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- Thermal Shutdown Protection
- SOP-8L with exposed pad Pb-Free Package.

❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The package of AX1250ES is SOP-8L-EP; the pin assignment is given by:



Name	Description
VIN	Input Voltage pin
GND	Ground pin
REFEN	Reference voltage input and chip enable pin
VOUT	Output Voltage pin
VCNTL	Supply Input and Gate drive voltage pin
NC	No connect pin

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX1250 XX X Package Type ES: SOP-8L-EP Packing Blank: Tube A : Taping	Logo ← AX1250 → Part number YYWWX → ID code: internal WW: 01 ~ 52 Year: 10=2010 11=2011

❖ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristics	Symbol	Rating	Unit
VIN Supply Voltage	V_{IN}	6	V
Control Voltage	V_{CNTL}	6	V
Power Dissipation	PD	Internally Limited	W
Storage Temperature Range	T_{ST}	-65 to +150	°C
Thermal Resistance from Junction to case	θ_{JC}	15	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	40	°C/W

Note: θ_{JA} is measured with the PCB copper area (need connect to Exposed pad) of approximately 1.5 in^2 (Multi-layer).

❖ OPERATING RATTING

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	1.3 to V_{CNTL}	V
Control Voltage	V_{CNTL}	5 or 3.3	V
Ambient Temperature	T_A	-40 to +85	°C
Junction Temperature	T_J	-40 to +125	°C

Note: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

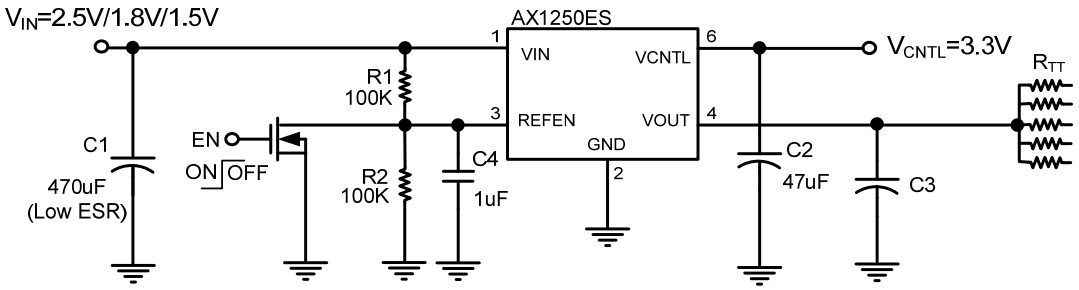
❖ ELECTRICAL CHARACTERISTICS

V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REFEN}=1.25V, C_{OUT}=10µF (Ceramic), T_A=25ºC, unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Gate Drive Voltage Range	V_{CNTL}		-	3.3	5.5	V
POR Threshold	$V_{CNTLRTH}$		-	2.5	-	V
POR Hysteresis	V_{CNTL}		-	0.1	-	V
Input Voltage	V_{IN}		1.3	-	V_{CNTL}	V
Quiescent Current	I_{CNTL}	I_{OUT}=0A	-	1	3	mA
Standby Current	I_{STBY}	I_{OUT}=0A, V_{REFEN}=0V	-	1	10	µA
Output Offset Voltage **(Note1)**	V_{OS}	I_{OUT}=0A	-20	-	+20	mV
Load Regulation **(Note2)**	ΔV_{LOAD}	I_{OUT}=±2.0A	-	0.5	±2	%
Shutdown Threshold	V_{IH}	Enable, REFEN Rising	0.7	-	-	V
	V_{IL}	Shutdown, REFEN Falling	-	-	0.2	V
Current Limit	$I_{CL-Source}$	Sourcing	2.2	-	-	A
	$I_{CL-Sink}$	Sinking	2.2	-	-	A
Soft-Start Period	T_{SS}	V_{OUT}=1.25V	-	1.5	-	mS
Thermal Shutdown	T_{SD}		-	160	-	°C
Thermal Shutdown Hysterisis	T_{SDH}		-	30	-	°C

Note 1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.
Note 2: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

❖ APPLICATION CIRCUIT



R_{TT}=50Ω/33Ω/25Ω

C3=10uF(Ceramic) + 1000uF under the worst case testing condition

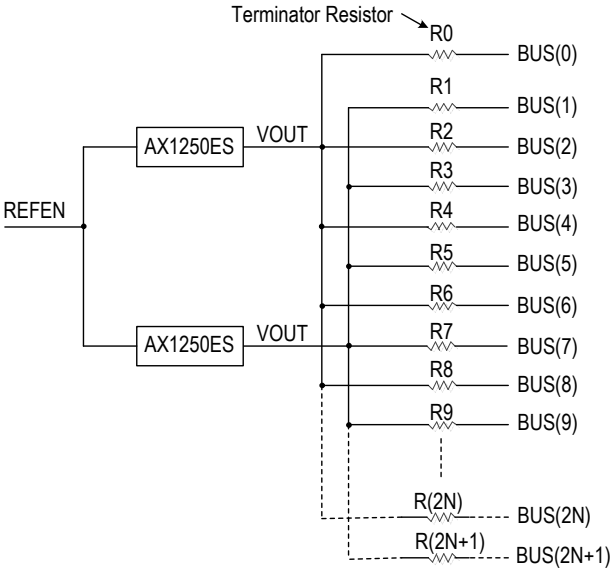
❖ APPLICATION INFORMATION

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AX1250ES. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AX1250ES and the preceding power converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the low pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Considerations

The AX1250ES series can deliver a current of up to 2A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$PD\ (MAX) = (T_{J\ (MAX)} - T_A) / \theta_{JA}$$

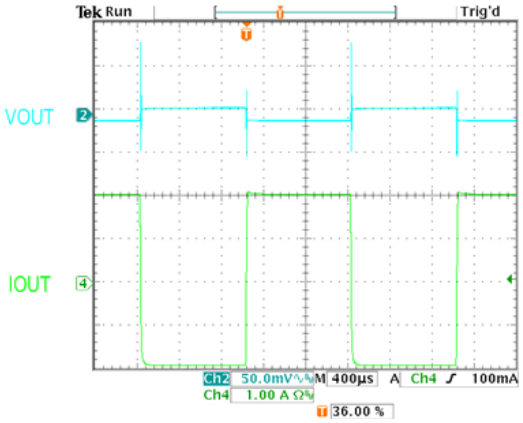
Where $T_{J\ (MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) for SOP-8L-EP (Exposed pad) package at recommended minimum footprint is 40°C/W on 1.5 in^2 and Multi-layer PCB layout. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$$PD\ (MAX) = (125°C - 25°C) / 40°C/W = 2.5W$$

The thermal resistance θ_{JA} of SOP-8L-EP (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of SOP-8L-EP package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

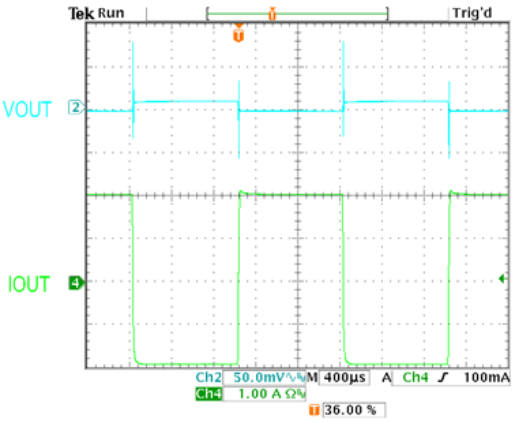
❖ TYPICAL CHARACTERISTICS

Transient Test



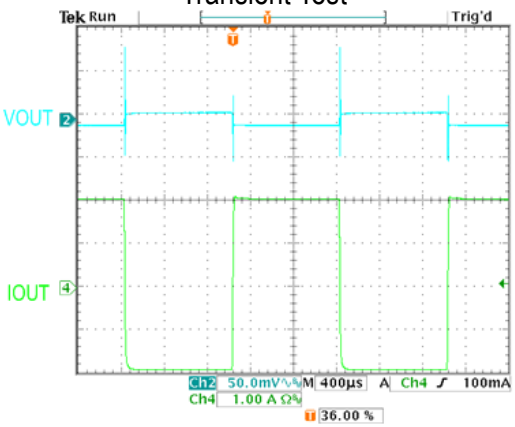
V_{IN}=2.5V, V_{OUT}=1.25V,
V_{CNTL}=3.3V, I_{OUT}=-1.5A~1.5A

Transient Test



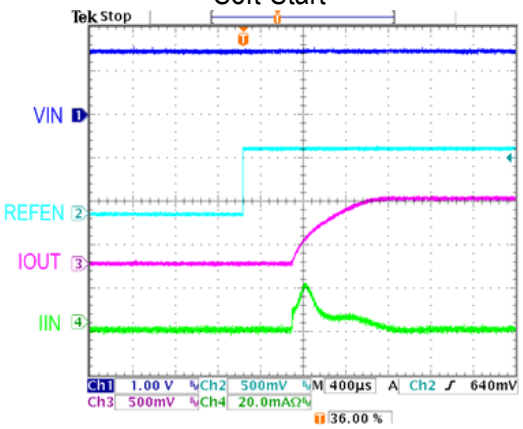
V_{IN}=1.8V, V_{OUT}=0.9V,
V_{CNTL}=3.3V, I_{OUT}=-1.5A~1.5A

Transient Test



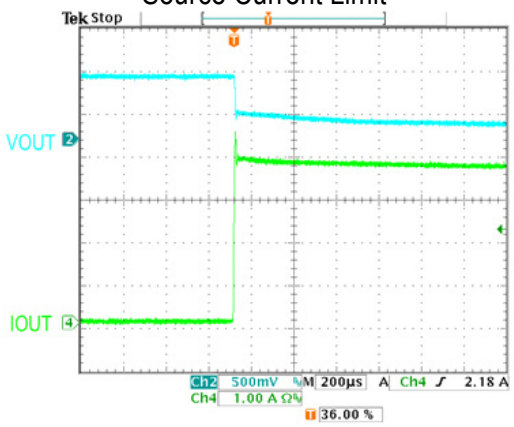
V_{IN}=1.5V, V_{OUT}=0.75V,
V_{CNTL}=3.3V, I_{OUT}=-1.5A~1.5A

Soft-Start



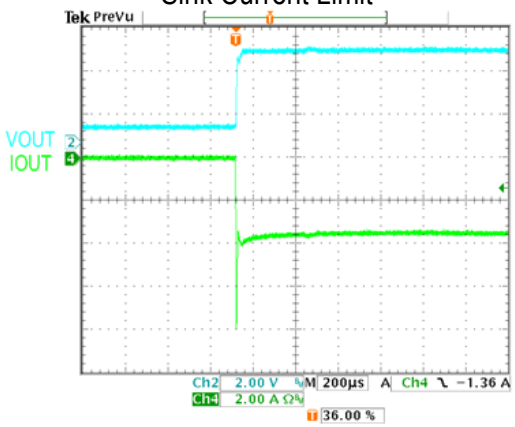
V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNTL}=3.3V

Source Current Limit



V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNTL}=3.3V

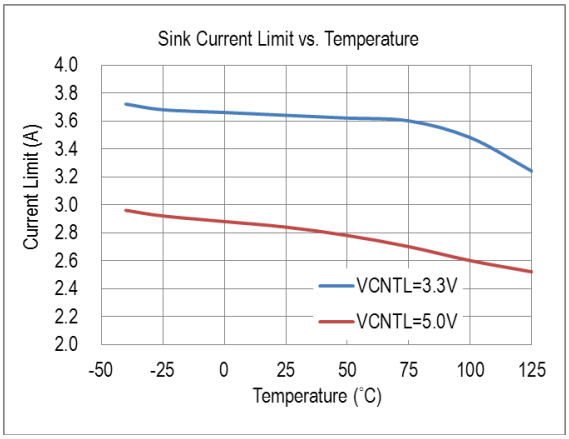
Sink Current Limit



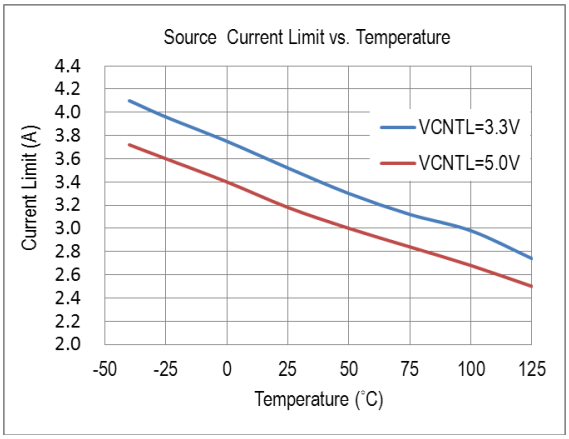
V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNTL}=3.3V

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

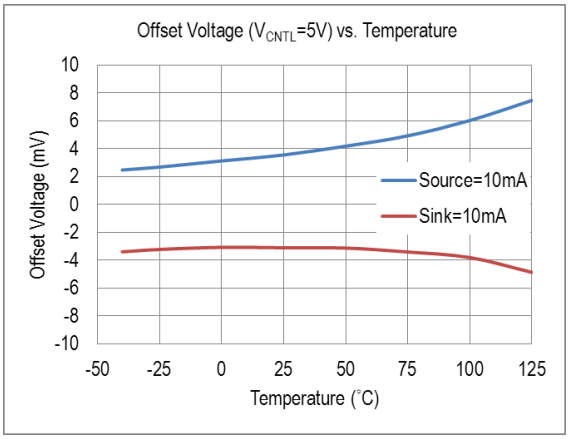
DDR-II



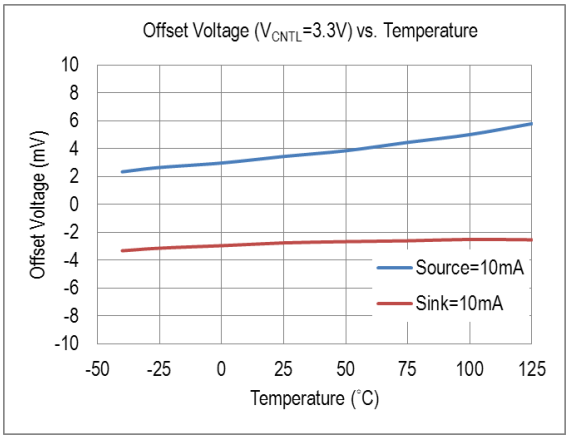
DDR-II



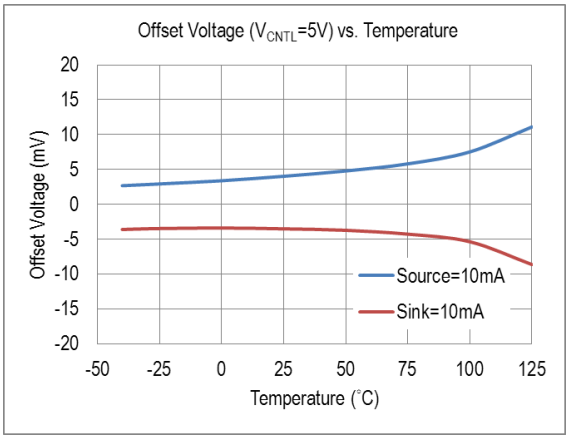
DDR-I



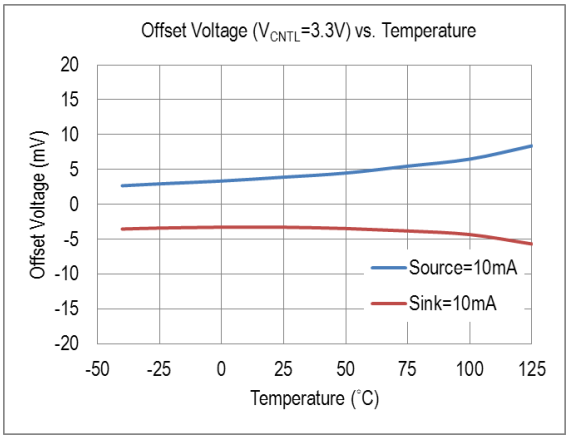
DDR-I



DDR-II

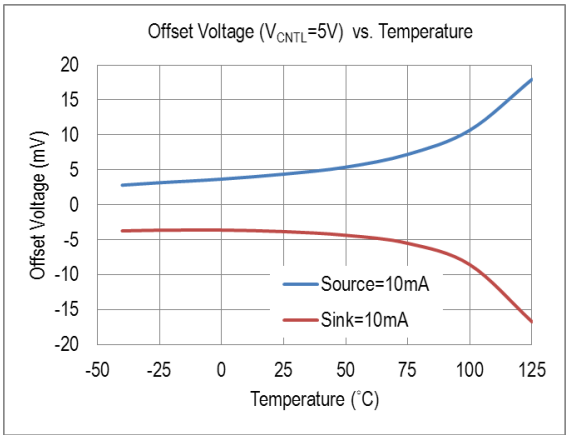


DDR-II

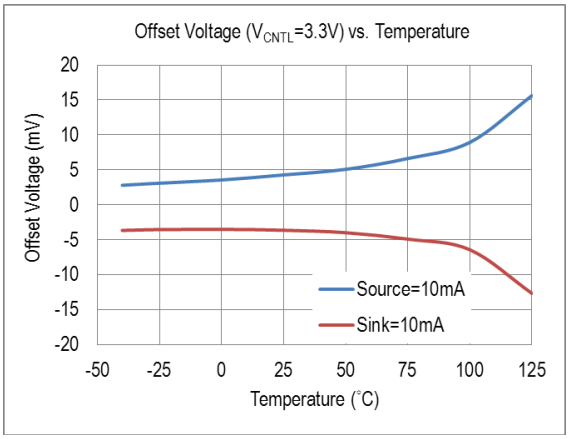


❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

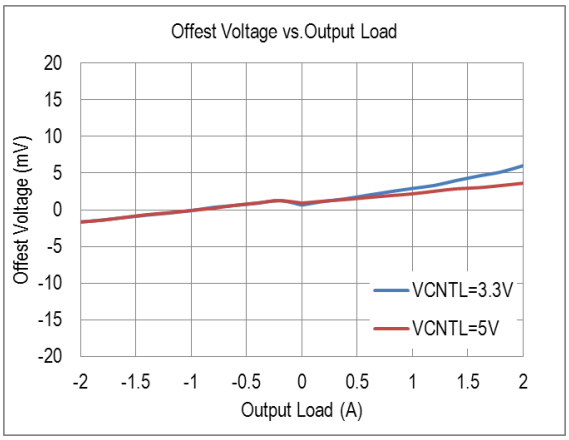
DDR-III



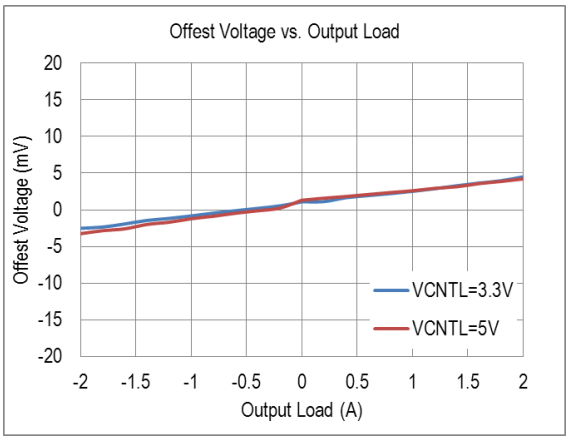
DDR-III



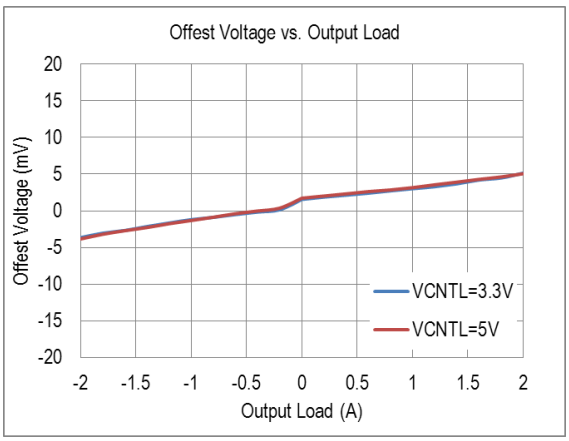
DDR-I



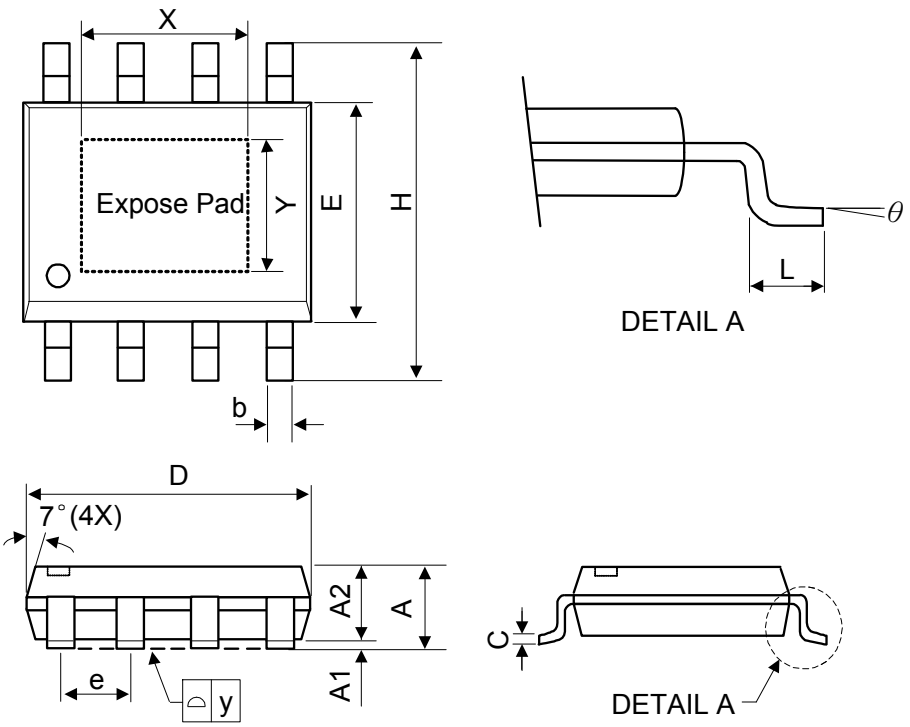
DDR-II



DDR-III



❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0	-	0.15	0	-	0.06
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
X	-	2.34	-	-	0.092	-
Y	-	2.34	-	-	0.092	-
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side

JEDEC outline: MS-012 BA