

## **1.5A Sink/Source Bus Termination Regulator**

### **❖ GENERAL DESCRIPTION**

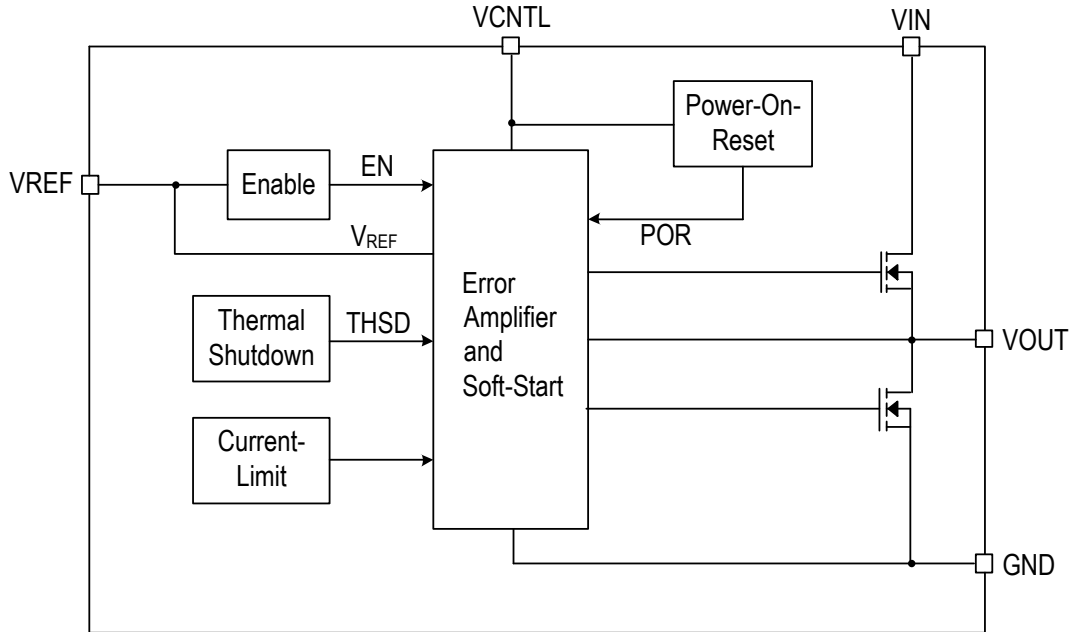
AX1250S is a linear regulator designed as a cost-effective solution for active termination of DDR SDRAM. The converting voltage range is from 1.3V to 5.5V into a desired output voltage, which is adjusted by two external resistors. The current sourcing and sinking capability of the regulator is up to 1.5A while the output voltage within 2%.

This device provides on-chip thermal shutdown and current limit functions for circuit tolerance of the output fault conditions. SOP-8L package is available for all commercial and industrial surface mount applications.

### **❖ FEATURES**

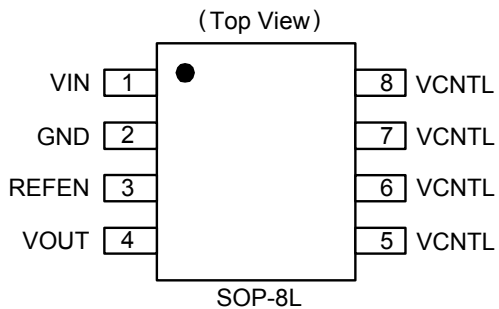
- Ideal for DDR-I, DDR-II and DDR-III applications
- Capable of sourcing and sinking current 1.5A
- Integrated power MOSFETs
- Current limiting protection
- Thermal shutdown protection
- High accuracy output voltage at full load
- Output Voltage Traces REFEN Pin Voltage
- Low external component count
- Shutdown for standby or suspend mode operation with high-Impedance output
- SOP-8L Pb-Free Package.

❖ **BLOCK DIAGRAM**



❖ **PIN ASSIGNMENT**

The package of AX1250S is SOP-8L; the pin assignment is given by:



Name	Description
<b>VIN</b>	Input Voltage pin
<b>GND</b>	Ground pin
<b>REFEN</b>	Reference voltage input and chip enable pin
<b>VOUT</b>	Output Voltage pin
<b>VCNTL</b>	Supply Input and Gate drive voltage pin

❖ **ORDER/MARKING INFORMATION**

Order Information	Top Marking
<p><b>AX1250 X X</b></p> <p>Package Type S: SOP-8L</p> <p>Packing Blank: Tube A: Taping</p>	<p>Logo ← <b>AX</b> 1250 → Part number</p> <p>YYWWX → ID code: internal</p> <p>WW: 01 ~ 52</p> <p>Year: 10=2010 11=2011</p>

**❖ ABSOLUTE MAXIMUM RATINGS** ( $T_A=25^{\circ}\text{C}$ )

Characteristics	Symbol	Rating	Unit
$V_{IN}$ Supply Voltage	$V_{IN}$	6	V
Control Voltage	$V_{CNTL}$	6	V
Power Dissipation	PD	Internally Limited	W
Storage Temperature Range	$T_{ST}$	-65 to +150	$^{\circ}\text{C}$
Thermal Resistance from Junction to case	$\theta_{JC}$	20	$^{\circ}\text{C/W}$
Thermal Resistance from Junction to ambient	$\theta_{JA}$	60	$^{\circ}\text{C/W}$

Note:  $\theta_{JA}$  is measured with the PCB copper area (need connect to all  $V_{CNTL}$  pins) of approximately 1.5 in<sup>2</sup>

(Multi-layer).

**❖ OPERATING RATTING**

Parameter	Symbol	Value	Unit
Input Voltage	$V_{IN}$	1.3 to $V_{CNTL}$	V
Control Voltage	$V_{CNTL}$	5 or 3.3	V
Ambient Temperature	$T_A$	-40 to +85	$^{\circ}\text{C}$
Junction Temperature	$T_J$	-40 to +125	$^{\circ}\text{C}$

Note:  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .

**❖ ELECTRICAL CHARACTERISTICS**

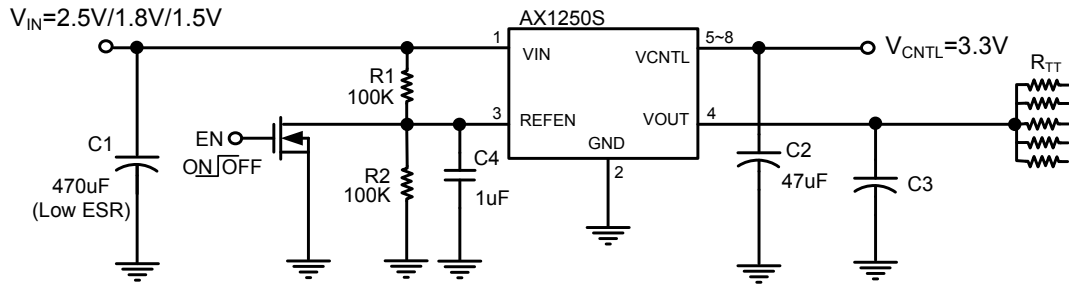
$V_{IN}=2.5\text{V}$ ,  $V_{CNTL}=3.3\text{V}$ ,  $V_{REFEN}=1.25\text{V}$ ,  $C_{OUT}=10\mu\text{F}$  (Ceramic),  $T_A=25^{\circ}\text{C}$ , unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Gate Drive Voltage Range	$V_{CNTL}$		-	3.3	5.5	V
POR Threshold	$V_{CNTLRTH}$		-	2.5	-	V
POR Hysteresis	$V_{CNTL}$		-	0.1	-	V
Input Voltage	$V_{IN}$		1.3	-	$V_{CNTL}$	V
Quiescent Current	$I_{CNTL}$	$I_{OUT}=0\text{A}$	-	1	3	mA
Standby Current	$I_{STBY}$	$I_{OUT}=0\text{A}$ , $V_{REFEN}=0\text{V}$	-	1	10	$\mu\text{A}$
Output Offset Voltage (Note1)	$V_{OS}$	$I_{OUT}=0\text{A}$	-20	-	+20	mV
Load Regulation (Note2)	$\Delta V_{LOAD}$	$I_{OUT}=\pm 1.5\text{A}$	-	0.5	$\pm 2$	%
Shutdown Threshold	$V_{IH}$	Enable, REFEN Rising	0.7	-	-	V
	$V_{IL}$	Shutdown, REFEN Falling	-	-	0.2	V
Current Limit	$I_{CL-Source}$	Sourcing	2	-	-	A
	$I_{CL-Sink}$	Sinking	2	-	-	A
Soft-Start Period	$T_{SS}$	$V_{OUT}=1.25\text{V}$	-	1.5	-	mS
Thermal Shutdown	$T_{SD}$		-	160	-	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	$T_{SDH}$		-	30	-	$^{\circ}\text{C}$

**Note 1:**  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .

**Note 2:** Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 1.5A.

❖ APPLICATION CIRCUIT



$$R_{TT}=50\Omega/33\Omega/25\Omega$$

C3=10uF(Ceramic) + 1000uF under the worst case testing condition

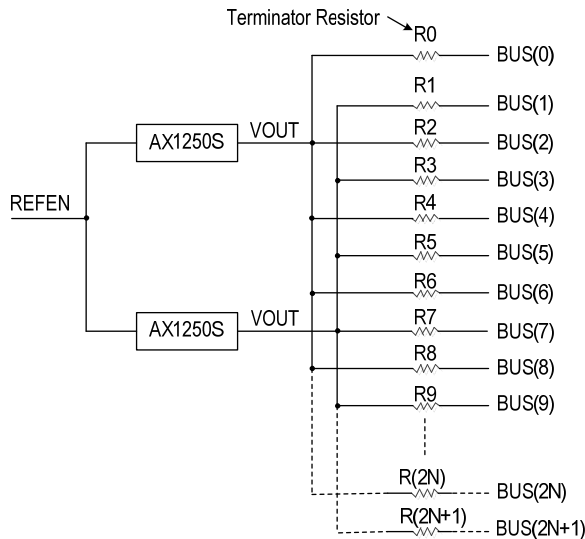
❖ APPLICATION INFORMATION

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AX1250S. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AX1250S and the preceding power converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V<sub>REFEN</sub> is below 0.2V. In addition, the capacitor and voltage divider form the low pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



## Thermal Considerations

The AX1250S series can deliver a current of up to 1.5A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

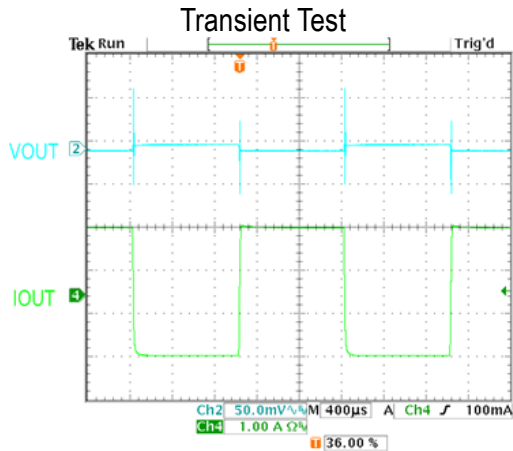
$$PD (MAX) = (T_{J (MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J (MAX)}$  is the maximum junction temperature of the die (125°C) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$ ) for SOP-8L package at recommended minimum footprint is 60°C/W on 1.5 in<sup>2</sup> and Multi-layer PCB layout. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

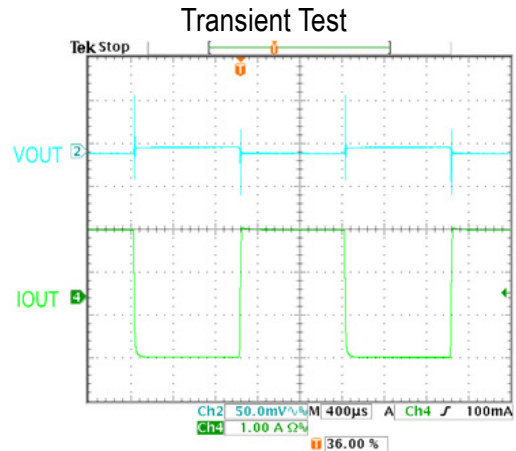
$$PD (MAX) = (125^\circ\text{C} - 25^\circ\text{C}) / 60^\circ\text{C} / \text{W} = 1.67\text{W}$$

The thermal resistance  $\theta_{JA}$  of SOP-8L is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding wide copper to  $V_{CNTL}$  pins. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

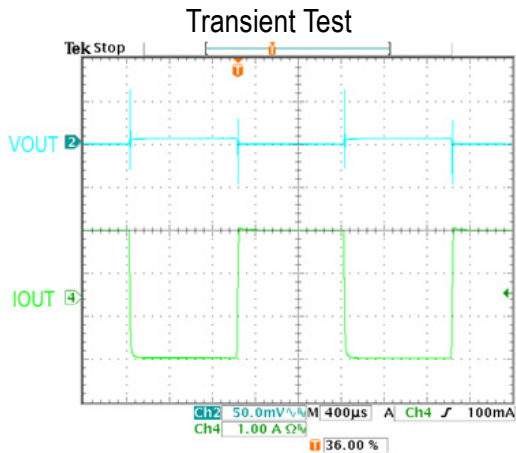
❖ TYPICAL CHARACTERISTICS



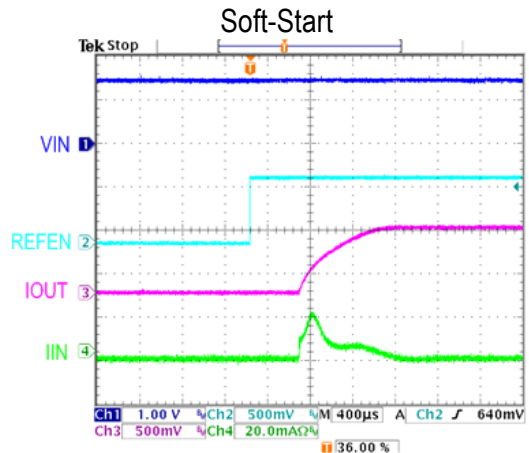
$V_{IN}=2.5V, V_{OUT}=1.25V,$   
 $V_{CNL}=3.3V, I_{OUT}=-1.5A\sim 1.5A$



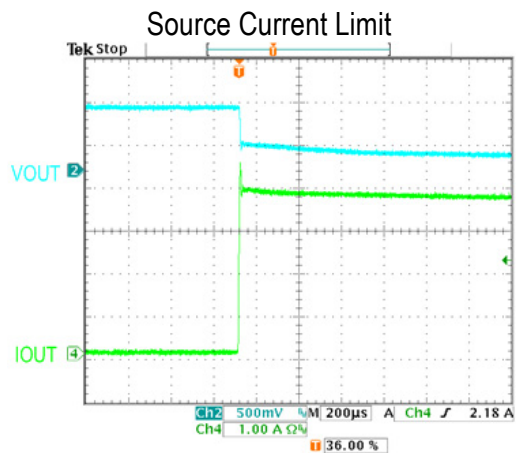
$V_{IN}=1.8V, V_{OUT}=0.9V,$   
 $V_{CNL}=3.3V, I_{OUT}=-1.5A\sim 1.5A$



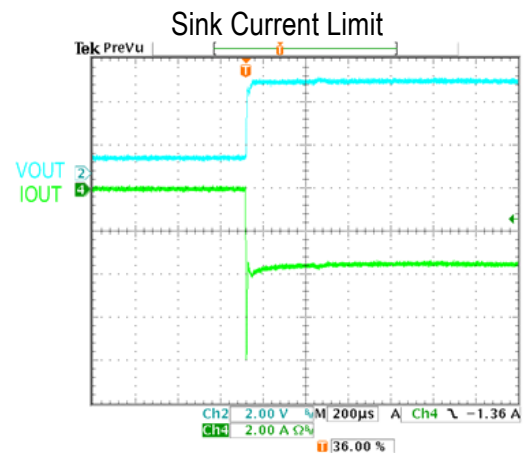
$V_{IN}=1.5V, V_{OUT}=0.75V,$   
 $V_{CNL}=3.3V, I_{OUT}=-1.5A\sim 1.5A$



$V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNL}=3.3V$



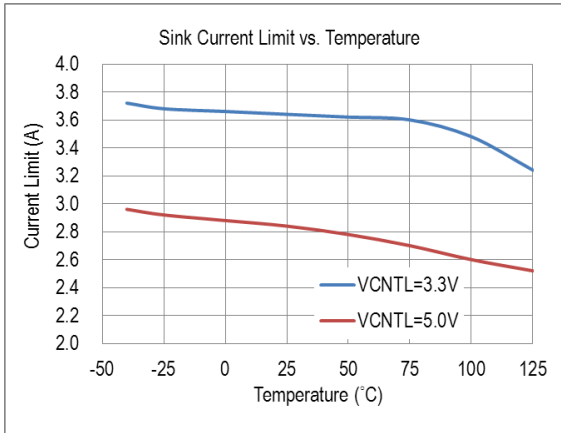
$V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNL}=3.3V$



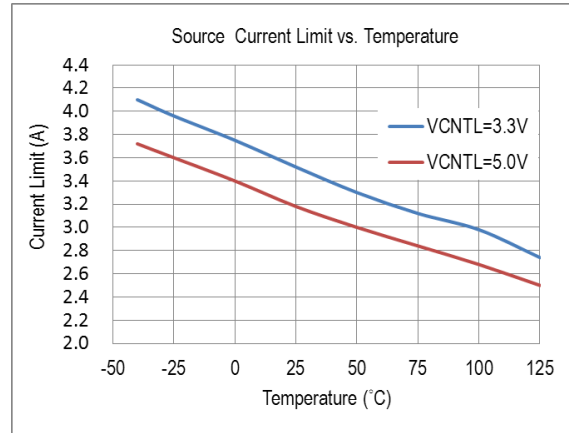
$V_{IN}=1.5V, V_{OUT}=0.75V, V_{CNL}=3.3V$

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

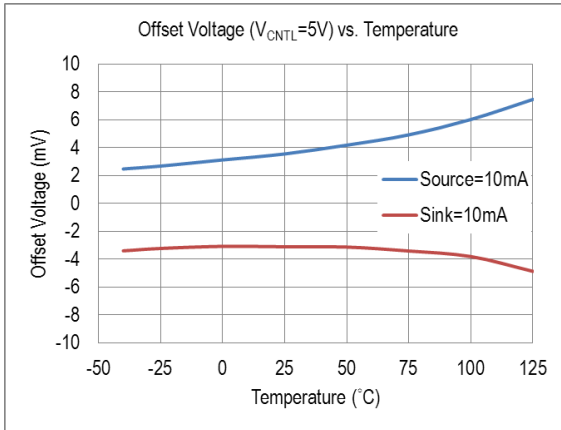
DDR-II



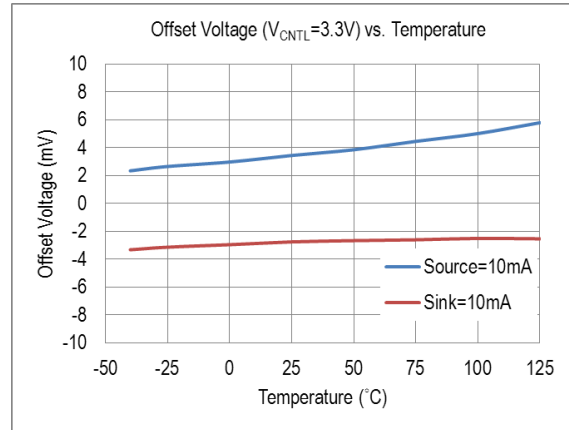
DDR-II



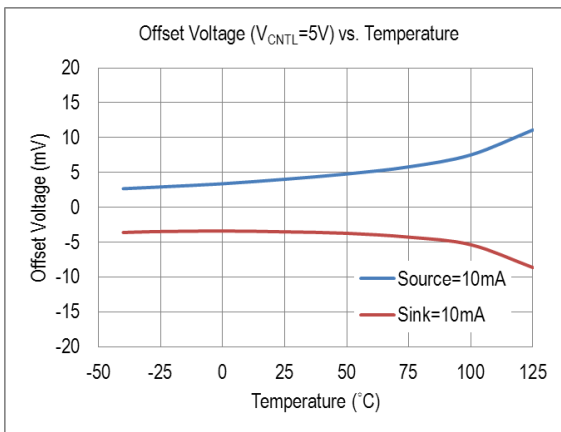
DDR-I



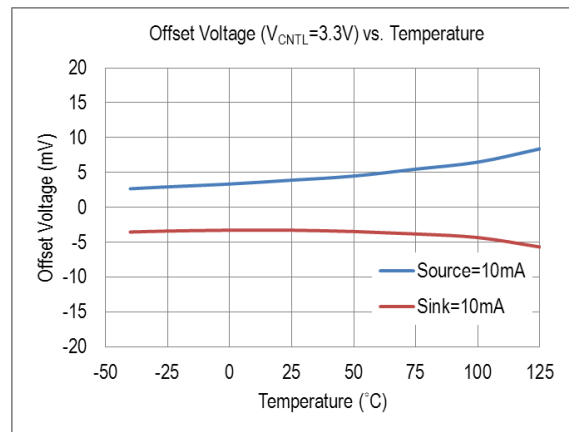
DDR-I



DDR-II

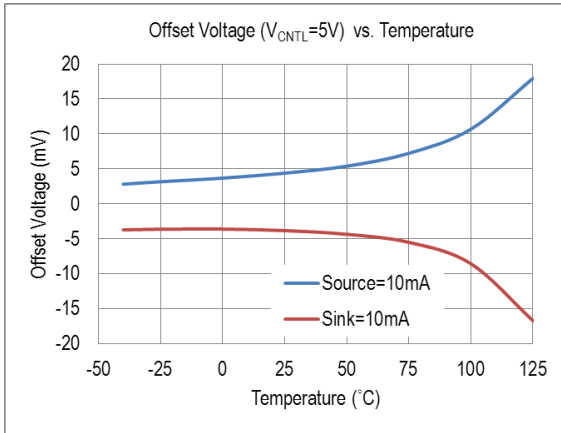


DDR-II

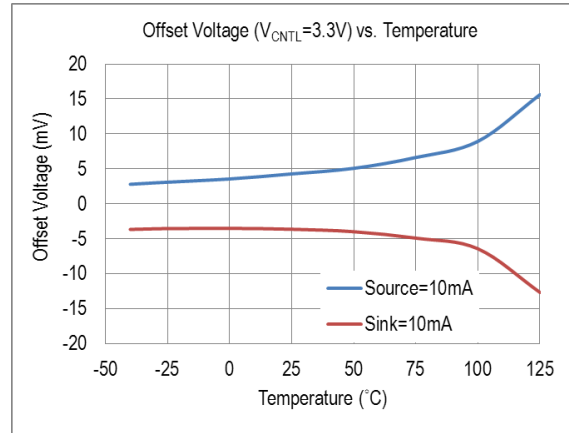


❖ **TYPICAL CHARACTERISTICS (COUNTINOUS)**

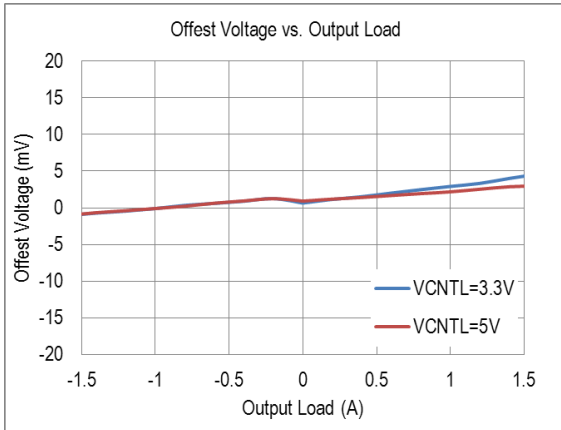
**DDR-III**



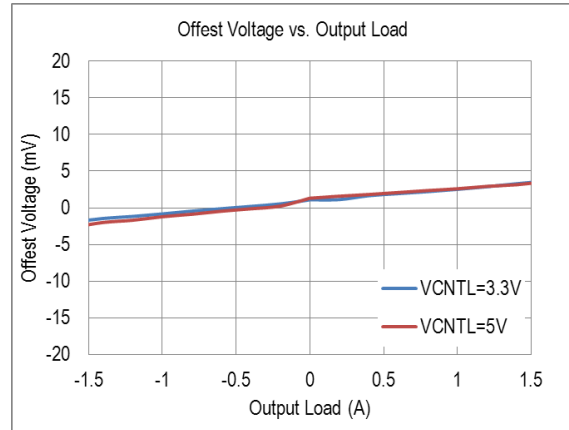
**DDR-III**



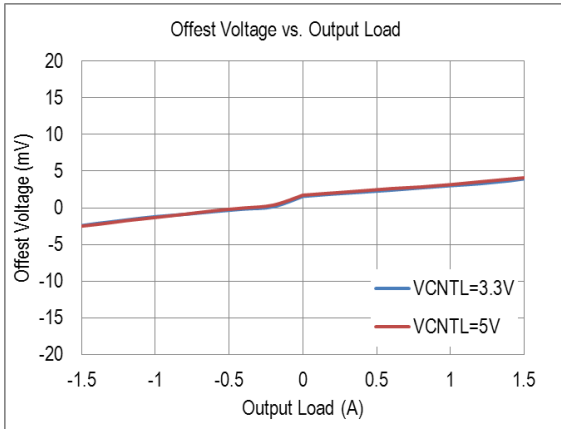
**DDR-I**



**DDR-II**

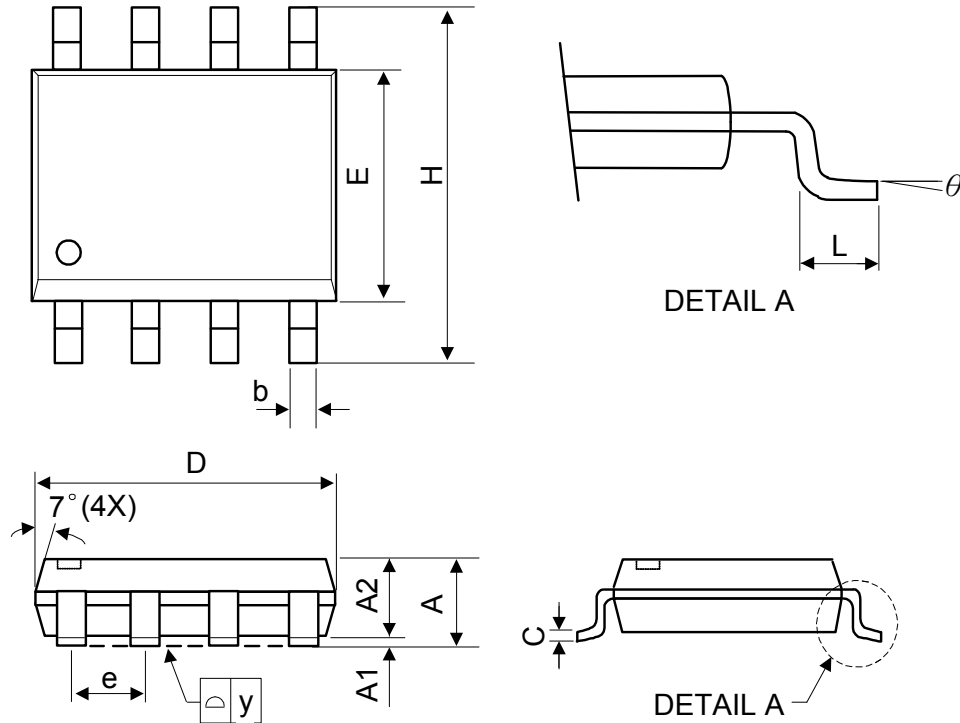


**DDR-III**





❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
$\theta$	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side

JEDEC outline: MS-012 AA