DATASHEET

AX5051-510

470-510 MHz ASK/FSK/PSK Transceiver

Datasheet extension for AX5051

Version 1.13-510

Document	Type	Datasheet
Document	Status	
Document	Version	Version 1.13-510
Product		AX5051-510

Table of Contents

1. Overview

This datasheet explains the parameters of AX5051 in the Chinese ISM bands between 470-510 MHz. The specification between 400-470 MHz and 800-940 MHz stays unchanged.

1.1. Features

- **Configurable for usage between 470 and 510 MHz**

1.2. Applications

Operation in the Chinese ISM bands between 470 MHz and 510 MHz.

- Telemetry
- Sensor readout, thermostats
- AMR
- Toys
- Wireless audio
- Wireless networks
- Wireless M-Bus
- Access control
- Remote keyless entry
- Remote controls
- Active RFID

2. Block Diagram

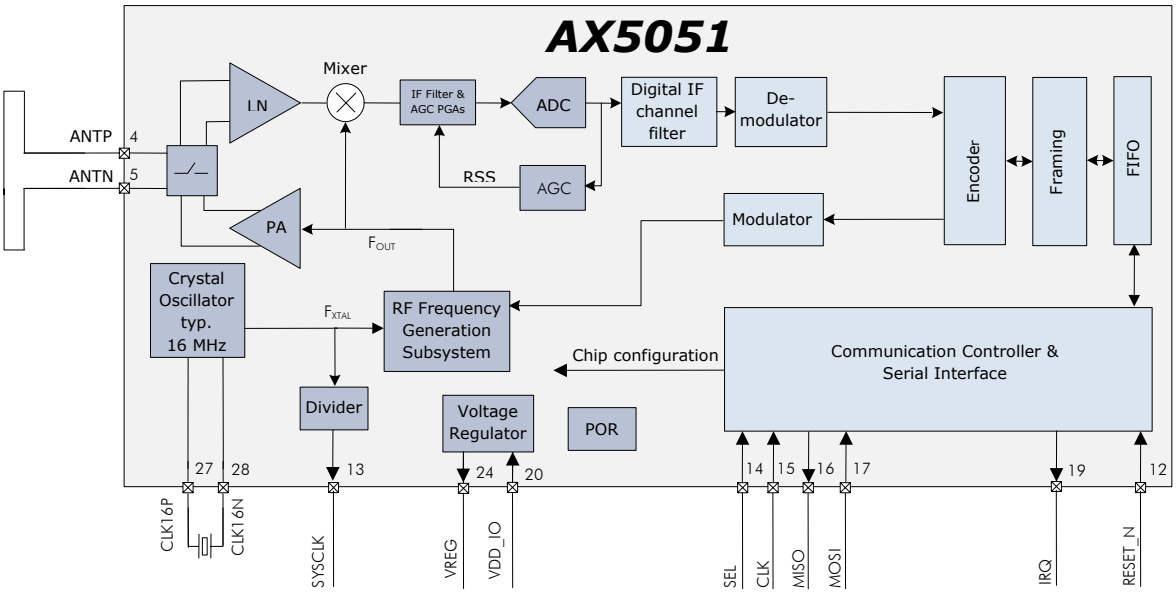

Figure 1 Functional block diagram of the AX5051

3. Pin Function Descriptions

Symbol	Pin(s)	Type	Description
NC	1	N	Not to be connected
VDD	2	P	Power supply, must be supplied with regulated voltage VREG
GND	3	P	Ground
ANTP	4	A	Antenna input/output
ANTN	5	A	Antenna input/output
GND	6	P	Ground
VDD	7	P	Power supply, must be supplied with regulated voltage VREG
NC	8	N	Not to be connected
TST1	9	I	Must be connected to GND
TST2	10	I	Must be connected to GND
GND	11	P	Ground
RESET_N	12	I	Optional reset pin If this pin is not used it must be connected to VDD_IO
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
TST3	18	I	Must be connected to GND
IRQ	19	I/O	Default functionality: Transmit and receive interrupt Can be programmed to be used as a general purpose I/O pin
VDD_IO	20	P	Unregulated power supply
NC	21	N	Not connected
GND	22	P	Ground
NC	23	N	Not to be connected
VREG	24	P	Regulated output voltage VDD pins must be connected to this supply voltage A 1µF low ESR capacitor to GND must be connected to this pin
NC	25	N	Not to be connected
NC	26	N	Not to be connected
CLK16P	27	A	Crystal oscillator input/output
CLK16N	28	A	Crystal oscillator input/output

A = analog signal
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs; digital input and output levels are LVCMOS/LVTTL compatible and 5V tolerant.

The center pad of the QFN28 package should be connected to GND.

3.1. Pin-out Drawing

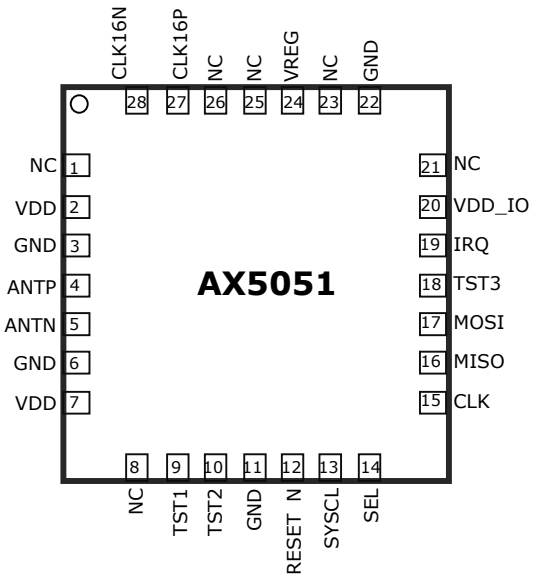

Figure 2: Pin-out drawing (Top view)

4. Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
VDD_IO	Supply voltage		-0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		-10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		-100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		-0.5	5.5	V
	Input voltage digital pins		-0.5	5.5	V
V_{es}	Electrostatic handling	HBM	-2000	2000	V
T_{amb}	Operating temperature		-40	85	°C
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction Temperature			150	°C

4.2. DC Characteristics

Supplies

SYMBOL	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
T_{AMB}	Operational ambient temperature		-40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage	RX operation or TX operation up to 4 dBm output power	2.4	3.0	3.6	V
		TX operation up to 12 dBm output power	2.5	3.0	3.6	V
VREG	Internally regulated supply voltage	Power-down mode PWRMODE=0x00		1.7		V
		All other power modes	2.1	2.5	2.8	V
$VREG_{droptyp}$	Regulator voltage drop	RX operation or TX operation up to 4 dBm output power			50	mV
$VREG_{dropmax}$	Regulator voltage drop at maximum internal current consumption	TX mode with 12 dBm output power			300	mV
I_{PDOWN}	Power-down current	PWRMODE=0x00		0.5		µA
I_{RX-HS}	Current consumption RX High sensitivity mode: VCO_I=001; REF_I=011	Bit rate 10 kbit/s		19		mA
I_{RX-LP}	Current consumption RX Low power mode: VCO_I=001; REF_I=101	Bit rate 10 kbit/s		17		mA
I_{TX}	Current consumption TX VCO_I=001; REF_I=011; LOCURST=1	470 MHz, 10 dBm		28		mA
		470 MHz, 0 dBm		19		
		470 MHz, 15 dBm		45		
		470 MHz, min power		11		

Logic

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUTS						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		-10		10	µA
DIGITAL OUTPUTS						
I_{OH}	Output Current, high	V_{OH}= 2.4V	4			mA
I_{OL}	Output Current, low	V_{OL}= 0.4V	4			mA
I_{OZ}	Tri-state output leakage current		-10		10	µA

4.3. AC Characteristics

Crystal Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{XTAL}	Crystal frequency	Note 1, 3	15.5	16	25	MHz
gm_{osc}	Transconductance oscillator	XTALOSCGM=0000		1		mS
		XTALOSCGM=0001		2		
		XTALOSCGM =0010 default		3		
		XTALOSCGM =0011		4		
		XTALOSCGM =0100		5		
		XTALOSCGM =0101		6		
		XTALOSCGM =0110		6.5		
		XTALOSCGM =0111		7		
		XTALOSCGM =1000		7.5		
		XTALOSCGM =1001		8		
		XTALOSCGM =1010		8.5		
		XTALOSCGM =1011		9		
		XTALOSCGM =1100		9.5		
		XTALOSCGM =1101		10		
		XTALOSCGM =1110		10.5		
		XTALOSCGM =1111		11		
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 000000 default		2		pF
		XTALCAP = 111111		33		pF
$C_{osc\text{-}lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP			0.5		pF
f_{ext}	External clock input	Note 2, 3	15.5	16	25	MHz
RIN_{osc}	Input DC impedance		10			kΩ

Notes

1. Tolerances and start-up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ
2. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and XTALCAP=000000
3. Lower frequencies than 15.5 MHz or higher frequencies than 25 MHz can be used. However not all typical RF frequencies can than be generated

RF Frequency Generation Subsystem (Synthesizer)

SYMBOL	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
f_{REF}	Reference frequency	Note 1		16 24		MHz
f_{range_hi}	Frequency range	BANDSEL=0				MHz
f_{range_low}		BANDSEL=1	470		510	
f_{RESO}	Frequency resolution		1			Hz
BW_1	Synthesizer loop bandwidth VCO current: VCOI=001	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		100		kHz
BW_2		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
BW_3		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		200		
BW_4		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		500		
T_{set1}	Synthesizer settling time for 1MHz step as typically required for RX/TX switching VCO current: VCO_I=001	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		15		µs
T_{set2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		30		
T_{set3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		7		
T_{set4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		3		
T_{start1}	Synthesizer start-up time if crystal oscillator and reference are running VCO current: VCO_I=001	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		25		µs
T_{start2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
T_{start3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		12		
T_{start4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		5		
PN_{470}	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010 VCO current: VCO_I=001	470 MHz, 50 kHz from carrier		-90		dBc/Hz
		470 MHz, 100 kHz from carrier		-95		
		470 MHz, 300 kHz from carrier		-105		
		470 MHz, 2 MHz from carrier		-115		

Notes
1. ASK, PSK and 0.1-200 kbps FSK with 16 MHz crystal, 200-350 kbps FSK with 24 MHz crystal

Transmitter

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK	1		350	
PTX_{470}	Transmitter power @ 470 MHz	TXRNG=1111 LOCURST=1		15		dBm

Notes

Note 1. 1-200 kbps with a 16 MHz crystal, 200-350 kbps with a 24 MHz crystal

Receiver

Datarate	Input sensitivity TYP. on SMA connector for BER=10^{-3}					
kbps	ASK	FSK h=1	FSK h=4	FSK h=8	FSK h=16	PSK
1.2				-115	-116	
2				-115	-115	
10	-103			-109		-110
100	-97	-103	-98			-104
200	-94	-100				-100
600	-90					-98

Condition: 470 MHz

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK	1		350	
		802.15.4 (ZigBee)		-100		
IL	Maximum input level				-20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		-35		dBm
IIP3	Input referred IP3			-25		
RSSIR	RSSI control range			85		dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AGCCOUNTER, TRKAMPL		0.1		dB
SEL_{470}	Adjacent channel suppression	FSK 50 kbps, notes 1 & 2		18		dB
	Alternate channel suppression			19		
	Adjacent channel suppression	FSK 100 kbps, notes 1 & 3		16		dB
	Alternate channel suppression			30		
	Adjacent channel suppression	PSK 200 kbps, notes 1 & 4		17		dB
	Alternate channel suppression			28		
BLK_{470}	Blocking at +/- 1MHz offset	FSK 100 kbps, note 5		38		dB
	Blocking at - 2MHz offset			40		
	Blocking at +/- 10MHz offset			60		
	Blocking at +/- 100MHz offset			82		
$IMRR_{470}$	Image rejection			30		

Notes

1. Interferer/Channel @ BER = 10^{-3}, channel level is +10dB above the typical sensitivity, the interfering signal is a random data signal (except PSK200); both channel and interferer are modulated without shaping
2. FSK 50 kbps: 470 MHz, 200 kHz channel spacing, 25 kHz deviation, programming as recommended in Programming Manual
3. FSK 100 kbps: 470 MHz, 400kHz channel spacing, 50 kHz deviation , programming as recommended in Programming Manual
4. PSK 200 kbps: 470 MHz, 400kHz channel spacing, programming as recommended in Programming Manual, interfering signal is a constant wave
5. Channel/Blocker @ BER = 10^{-3}, channel level is +10dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated without shaping, the image frequency lies 2 MHz above the wanted signal

SPI Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high-Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	Note 1	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

Notes

1. For SPI access during power-down mode the period should be relaxed to 100ns.

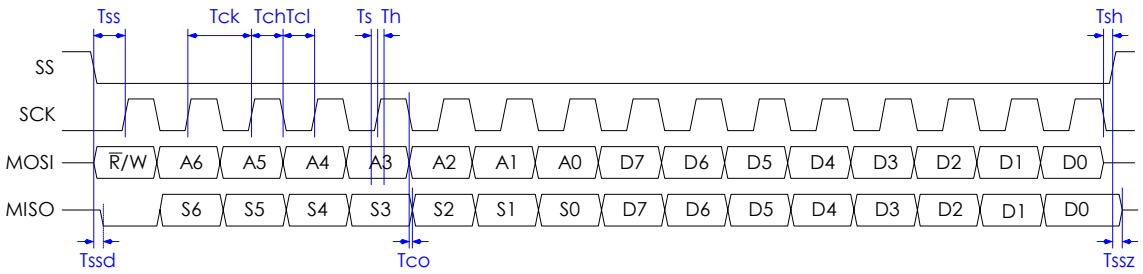

Figure 3 Serial peripheral interface timing

5. Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. AXSEM customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify AXSEM for any damages resulting from such improper use or sale.

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