Current Mode PWM Power Switch

❖ GENERAL DESCRIPTION

AX6224 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications in under 8W range.

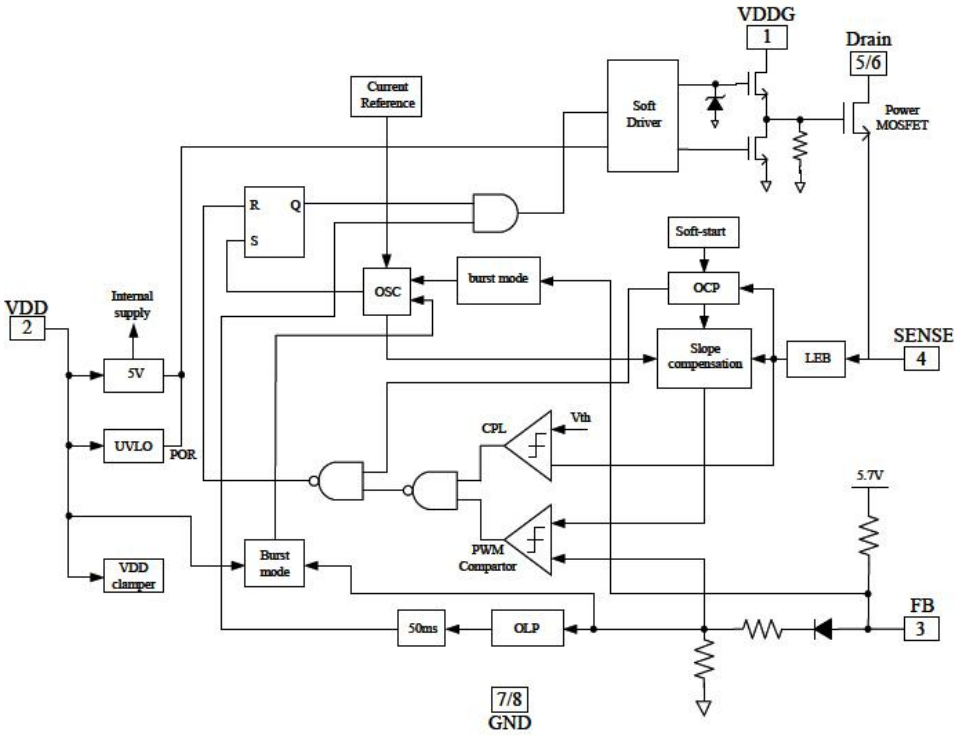
AX6224 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHz is minimized in the design and audio noise is eliminated during operation. AX6224 is offered in SOP-8L package.

❖ FEATURES

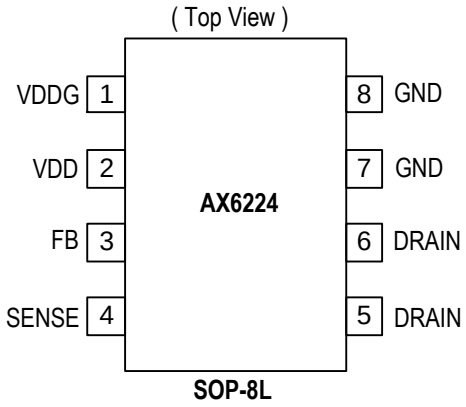
- Power on Soft Start Reducing MOSFET V_{DS} Stress
- Frequency Shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 50KHz Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- Good Protection Coverage With Auto Self-Recovery
  - ◆ VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
  - ◆ Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting for Constant Output Power Limiting Over Universal Input Voltage Range
  - ◆ Overload Protection (OLP)
  - ◆ Over Voltage Protection (OVP)
- Compatible with OB2353/OB2354/CR6224
- Pb-Free SOP-8L

❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The package of AX6224 is SOP-8L; the pin assignment is given by:



Name	Pin No.	I/O	Description
VDDG	1	P	Internal Gate Driver Power Supply
VDD	2	P	IC DC Power Supply Input
FB	3	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
SENSE	4	I	Current sense input
DRAIN	5,6	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
GND	7,8	P	Ground

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX6224 X X Package: S: SOP-8L Packing: Blank : Tube	Logo ← AX 6 2 2 4 → Part number Y Y WW X → ID code:internal WW:01~52 Year: 11=2011, 12=2012

❖ ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristics	Symbol	Rating	Unit
Drain Voltage (off state)		-0.3 to 600	V
VDD Voltage		-0.3 to 30	V
VDDG Input Voltage		-0.3 to 30	V
VDD Clamp Continuous Current		10	mA
FB Input Voltage		-0.3 to 7	V
Sense Input Voltage		-0.3 to 7	V
Min/Max Operating Junction Temperature	T_J	-20 to 150	°C
Min/Max Storage Temperature	T_{STG}	-55 to 160	°C
Lead Temperature (Soldering, 10secs)		260	°C
Thermal Resistance from Junction to case	θ_{JC}	25	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	70	°C/W

Note: θ_{JA} is measured with the PCB copper area (need connect to OUT pin) of approximately 1.5 in^2 (Multi-layer).

❖ ELECTRICAL CHARACTERISTICS

(T_A=25°C, V_{DD}=V_{DDG}=16V, unless otherwise specified)

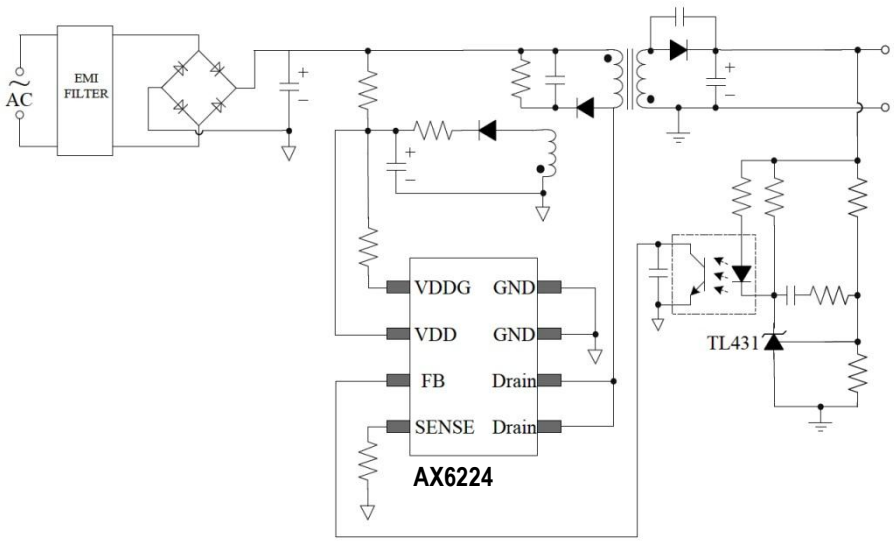
Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage (VDD)						
VDD Start-up Current	I_{ST}	V_{DD}=14.5V, measure leakage current into VDD	-	6	20	uA
Operation Current	I_V_{DD} _Operation	V_{FB}=3V	-	2.1	-	mA
VDD Under Voltage Lockout Enter	$U_{VLO(ON)}$		8.7	9.3	10.7	V
VDD Under Voltage Lockout Exit (Recovery)	$U_{VLO(OFF)}$		14.8	15.3	16.0	V
Over Voltage Protection	$O_{VP(ON)}$	FB=3V ramp up VDD until gate clock is off	27.0	28.8	30.0	V
VDD Zener Clamp Voltage	I_{DD}_Clamp	IDD=10mA	-	30	-	V
Feedback Input Section (FB Pin)						
V_{FB} Open Loop Voltage	V_{FB}_Open		5.4	5.6	6.0	V
FB Pin Short Circuit Current	I_{FB}_Short	Short FB pin to GND and measure current	-	1.45	-	mA
Zero Duty Cycle FB Threshold Voltage	V_{TH_0D}		-	1.23	-	V
Power Limiting FB Threshold Voltage	V_{TH}_PL		-	4.2	-	V
Power Limiting De-bounce Time	T_D_PL		-	50	-	ms
Input Impedance	Z_{FB}_IN		-	4	-	KΩ
Current Sense Input (Sense Pin)						
Soft start time			-	4	-	ms
Leading Edge Blanking Time	T_blanking		-	270	-	ns
Input Impedance	Z_{SENSE}_IN		-	40	-	KΩ
Over Current Detection and Control Delay	T_D_OC	From over current occurs till the Gatedriver output start to turn off	-	120	-	ns
Internal Current Limiting Threshold Voltage	V_{TH}_OC	FB=3.3V	0.78	0.83	0.88	V

❖ ELECTRICAL CHARACTERISTICS (CONTINUOUS)

(T_A=25°C, V_{DD}=V_{DDG}=16V, unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Oscillator						
Normal Oscillation Frequency	F_{OSC}		43	48	53	KHz
Frequency Temperature Stability	Δf_Temp		-	5	-	%
Frequency Voltage Stability	Δf_VDD		-	5	-	%
Maximum Duty Cycle	D_max	FB=3.3V, CS=0V	70	80	90	%
Burst Mode Base Frequency	F_Burst		-	22	-	KHz
Power MOSFET Section						
MOSFET Drain Source Breakdown Voltage	BVdss		600	-	-	V
Static Drain to Source On Resistance	$R_{DS(ON)}$		7	9	11	Ω
Frequency						
Frequency Modulation Range/Base Frequency	Δ_VDD		-4	-	4	%

❖ APPLICATION CIRCUIT



❖ FUNCTION DESCRIPTIONS

The AX6224 is a low power off-line SMPS Switcher optimized for off-line flyback converter applications in under 8W power range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of AX6224 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 2MΩ, 0.125W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of AX6224 is low at 2mA. Good efficiency is achieved with AX6224 low operating current together with the 'Extended burst mode' control features.

Soft Start

AX6224 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO (OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.83V. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency Shuffling (switching frequency modulation) is implemented in AX6224. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition.

The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters burst mode control. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency of AX6224 is internally fixed at 50KHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in AX6224 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Drive

The internal power MOSFET in AX6224 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

Operation Description

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

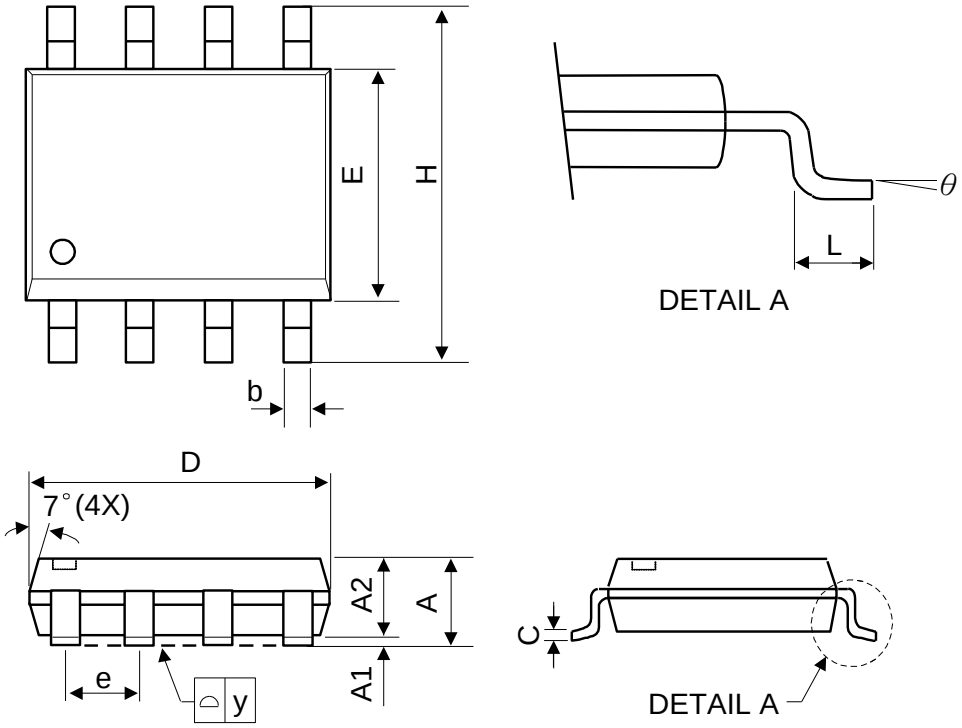
In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle Current Limiting (OCP), Overload Protection (OLP) and Over Voltage Clamp, Under Voltage Lockout on VDD (UVLO). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than 30V. The output of AX6224 is shut down when VDD drops below UVLO_ON limit and Switcher enters power on start-up sequence.

❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side

JEDEC outline: MS-012 AA