Ultra Low Output Voltage Linear N-FET Controller

❖ GENERAL DESCRIPTION

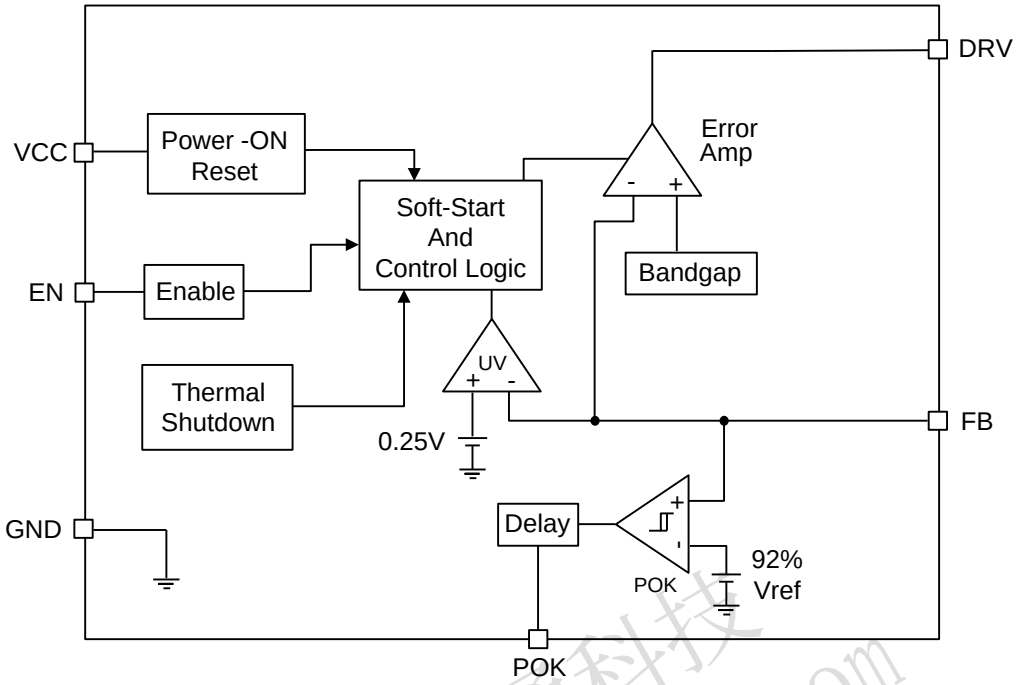
The AX6302 is an ultra low output voltage linear N-FET controller. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The AX6302 integrates many functions. A Power-On-Reset (POR) circuit monitors supply voltages to prevent wrong operations. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The AX6302 can be enabled by other power system.

A 0.5V reference voltage with 2% accuracy provide tight regulation of the output voltage, enable control, open drain power good signal, under-voltage protection and soft start.

❖ FEATURES

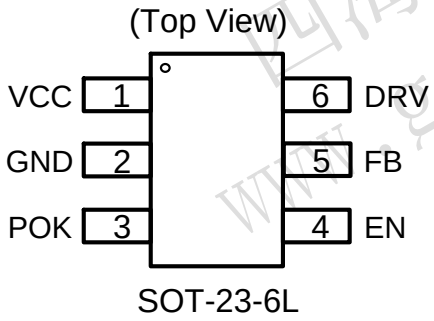
- Low ESR Output Capacitor (MLCC and POSCAP) Applicable
- 0.5V Reference Voltage with 2% accuracy
- Fast Transient Response
- Adjustable Output Voltage Down to 0.5V
- Enable Control
- Internal Soft-Start
- Under-Voltage Short Circuit Protection
- Drive N-Channel MOSFETs
- Power-OK Output with a Delay Time
- SOT-23-6L Pb-Free Package.

❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The package of AX6302 is SOT-23-6L the pin assignment is given by:



Name	Description
GND	GND pin
FB	Feedback pin
DRV	Gate drive to N-FET
EN	H：normal operation L：Shutdown
POK	Power OK Output Pin
VCC	Input Voltage

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX6302 X X Package Type: C：SOT-23-6L Packing: Blank: Bulk, A：Taping	ROYWX → ID code:internal WW:01~26 (A~Z), 27~52 (a~z) Year: A=2010, 1=2011 AX6302

❖ ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

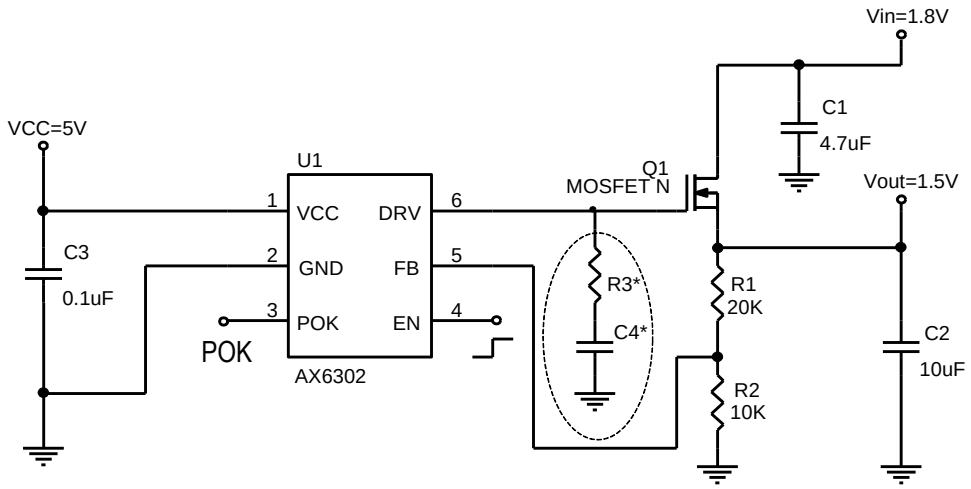
Characteristics	Symbol	Rating	Unit
VCC, EN,FB,POK		-0.3 to 7	V
DRV to GND	V_{DRV}	-0.3 to V_{CC}+0.3	V
Operating Temperature Range	T_{OP}	-40 to +85	°C
Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{ST}	-65 to +150	°C

❖ ELECTRICAL CHARACTERISTICS

(V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, T_A=25°C unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage range	V_{CC}		4.5	-	5.5	V
Input Voltage UVLO Threshold	V_{UVLO}	V_{CC} rising	-	3.75	-	V
Input Voltage UVLO Hysteresis	V_{HYST}	V_{CC} falling	-	0.25	-	V
Supply Current	I_{CC}	EN= V_{CC}	-	0.4	0.8	mA
Shutdown Current	I_{SD}	EN= 0V	-1	-	+1	uA
Feedback Voltage	V_{FB}		0.49	0.5	0.51	V
Feedback Pin Input Current	I_{FB}	V_{FB} =0.5V	-100	-	+100	nA
Soft Start Time	T_{SS}		-	1	-	mS
EN Pin Logic High threshold voltage	V_{ENH}	Enable	1.3	-	-	V
	V_{ENL}	Disable	-	-	0.5	
EN Pin Input Current	I_{EN}		-1	-	+1	uA
FB UVLO Threshold Voltage	$V_{TH(UV)}$	V_{FB} falling	0.2	0.25	0.3	V
DRV Output Current	$I_{DRV(SRC)}$	Sourcing, V_{FB}=0.48V	-	20	-	mA
	$I_{DRV(SINK)}$	Sinking ,V_{FB}=0.52V	-	20	-	mA
DRV Pin Output Voltage	V_{DRV}	V_{FB}=0.48V,V_{CC}=5V,no load	4.9	-	5.0	V
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising	90%	93%	96%	V_{FB}
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling	82%	85%	88%	V_{FB}
POK Low Voltage		POK sinks 1mA	-	35	50	mV
POK Delay Time	T_{DELAY}		0.8	2	10	mS
Thermal shutdown Temp	T_{SD}		-	150	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	50	-	°C

❖ APPLICATION CIRCUIT



$$VOUT = 0.5V * (1 + \frac{R1}{R2})$$

VFB = 0.5V ; R2 range 1 ~ 100k

R3*,C4* Option

❖ FUNCTION DESCRIPTIONS

Power-On-Reset

A Power-On-Reset (POR) circuit monitors input voltages at VCC pins to prevent wrong logic controls. The POR function initiates a soft-start process after the supply voltages exceed the rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCC voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 1mS.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.5V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation.

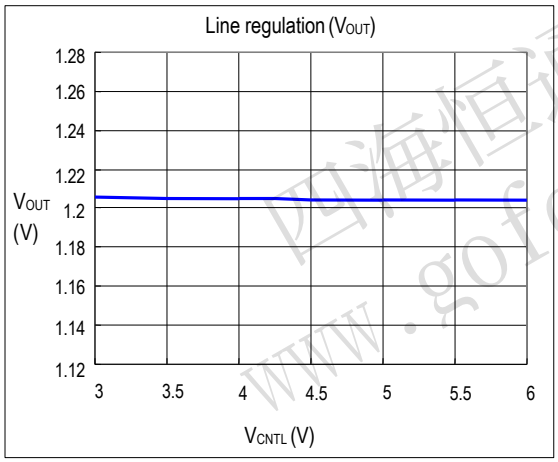
Under-Voltage Protection (UVP)

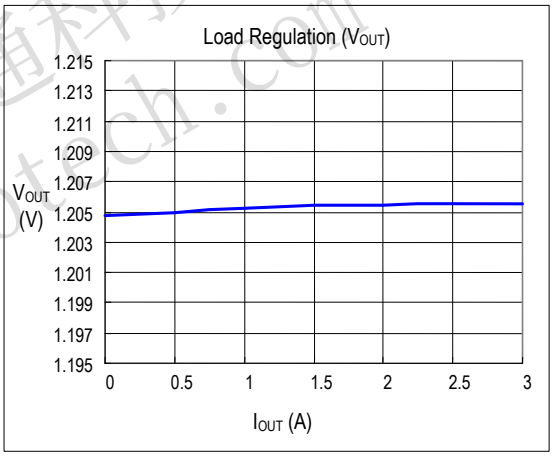
The AX6302 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while (~ 70% Duty), the AX6302 starts a new soft-start to regulate output.

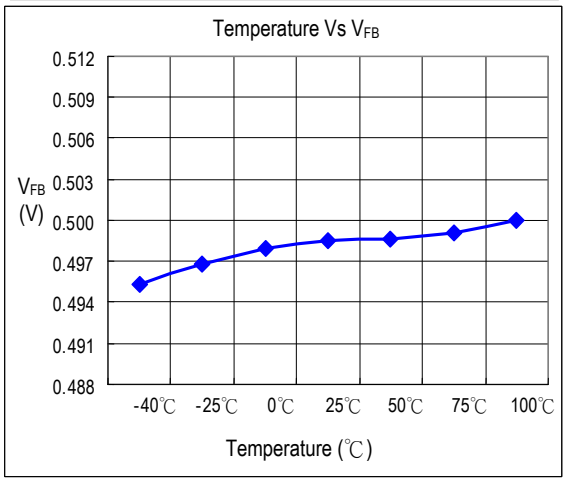
Thermal Shutdown

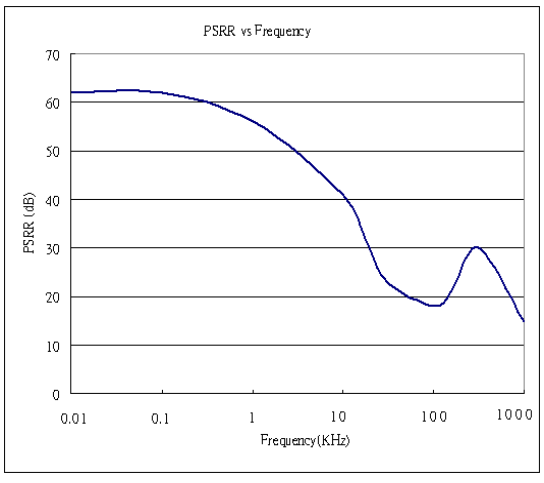
A thermal shutdown circuit limits the junction temperature of AX6302. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions.

❖ TYPICAL CHARACTERISTICS

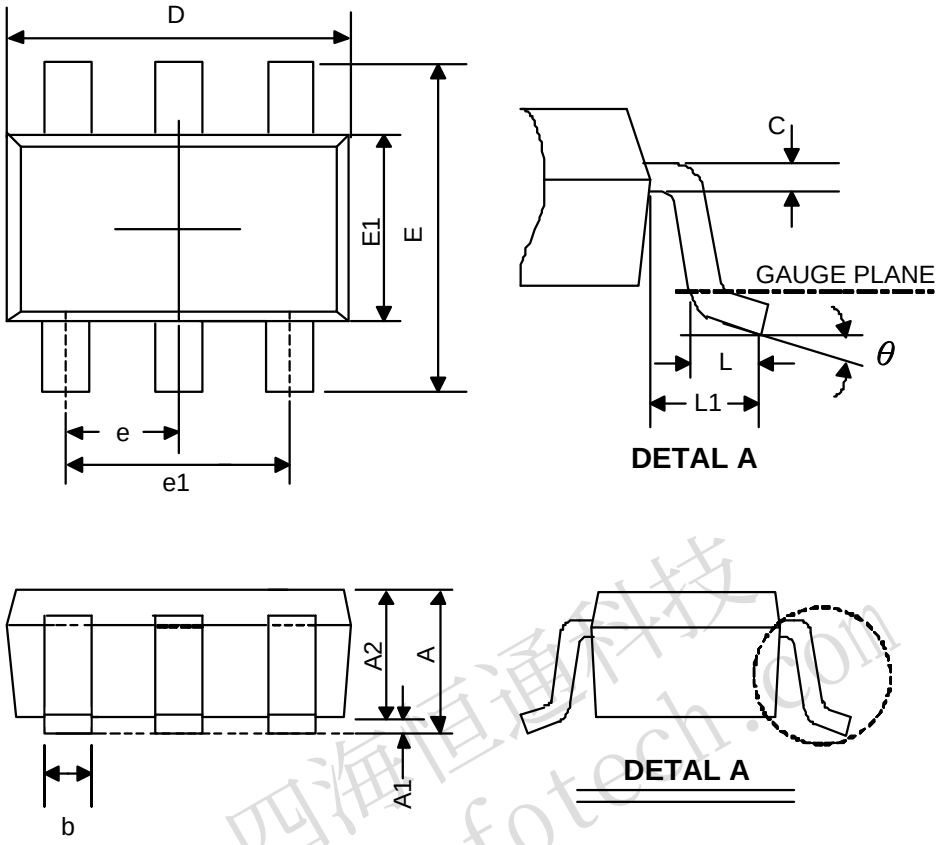








❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.45	-	-	0.057
A1	0	-	0.15	0	0.003	0.006
A2	0.9	1.1	1.3	0.035	0.043	0.051
b	0.3	0.4	0.5	0.012	0.016	0.02
C	0.08	-	0.22	0.003	0.006	0.009
D	2.7	2.9	3.1	0.106	0.114	0.122
E1	1.4	1.6	1.8	0.055	0.063	0.071
E	2.6	2.8	3	0.102	0.11	0.118
L	0.3	0.45	0.6	0.012	0.018	0.024
L1	0.5	0.6	0.7	0.02	0.024	0.028
e1	1.9 BSC			0.075 BSC		
e	0.95 BSC			0.037 BSC		
θ	0°	4°	8°	0°	4°	8°

JEDEC outline: MO-178 AB