

## **1A Ultra Low Dropout Linear Regulator**

### **❖ GENERAL DESCRIPTION**

The AX6613 is a 1A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The AX6613 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The AX6613 can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

The AX6613 is available in SOP-8L-EP, SOT-23-6L and TDFN-8L packages. That features small size as SOP-8L with an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

### **❖ FEATURES**

- Ultra Low Dropout - 0.2V(typical) at 1A Output Current
- Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit and Thermal Shutdown Protection
- Power-OK Output with a Delay Time
- SOP-8L with Exposed Pad, SOT-23-6L and TDFN-8L Pb-Free Packages.



❖ ORDER/MARKING INFORMATION

Order Information	Top Marking (SOP-8L-EP)
<p><b>AX6613 XX X</b></p> <p>Package Type C: SOT23-6L ES: SOP-8L-EP Z8: TDFN-8L(2*2)</p> <p>Packing Blank: Tube A: Taping</p>	<p>Logo ← <b>AX</b> 6 6 1 3 → Part number</p> <p>Y Y W W X → ID code: internal</p> <p>                    → WW: 01~52</p> <p>                    → Year: 10=2010                             11=2011</p>
Top Marking (SOT-23-6L)	Top Marking (TDFN-8L)
<p><b>GAY WX</b> → ID code:internal</p> <p>                    → WW:01~26 (A~Z)                             27~52 (a~z)</p> <p>                    → Year: A=2010                             1=2011</p> <p>AX6613</p>	<p><b>GA</b> → AX6613</p> <p><b>YWX</b> → ID Code: Internal</p> <p>                    → Week: 01~26(A~Z)                             27~52(a~z)</p> <p>                    → Year : A = 2010                             1 = 2011</p>

❖ ABSOLUTE MAXIMUM RATINGS (at T<sub>A</sub>=25°C)

Characteristics	Symbol	Rating	Unit
V <sub>CNTL</sub> Supply Voltage	V <sub>CNTL</sub>	-0.3 to 7	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>	-0.3 to 6	V
EN and FB Pin Voltage	V <sub>I/O</sub>	-0.3 to V <sub>CNTL</sub> +0.3	V
Power good Voltage	V <sub>POK</sub>	-0.3 to 7	V
Power Dissipation	SOP-8L-EP	3	W
	SOT-23-6L	0.4	
	TDFN-8L	0.8	
Storage Temperature Range	T <sub>ST</sub>	-65 to +150	°C
Junction Temperature Range	T <sub>J</sub>	-40 to 125	°C
Operating Temperature Range	T <sub>OP</sub>	-40 to +85	°C
Thermal Resistance from Junction to case	SOP-8L-EP	15	°C/W
	SOT-23-6L	180	
	TDFN-8L	20	
Thermal Resistance from Junction to ambient	SOP-8L-EP	40	°C/W
	SOT-23-6L	250	
	TDFN-8L	125	

Note: θ<sub>JA</sub> is measured with the PCB copper area (need connect to Expose-Pad) of approximately 1.5 in<sup>2</sup> (Multi-layer) by SOP-8L and DFN-8L packages.

❖ RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Conditions	Rating	Unit
V <sub>CNTL</sub> Supply Voltage	V <sub>CNTL</sub>		3 to 6.0	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>		1.0 to 5.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>CNTL</sub> -V <sub>OUT</sub> >1.9V	0.8 to 2.8	V
Output Current	I <sub>OUT</sub>		0 to 1.0	A

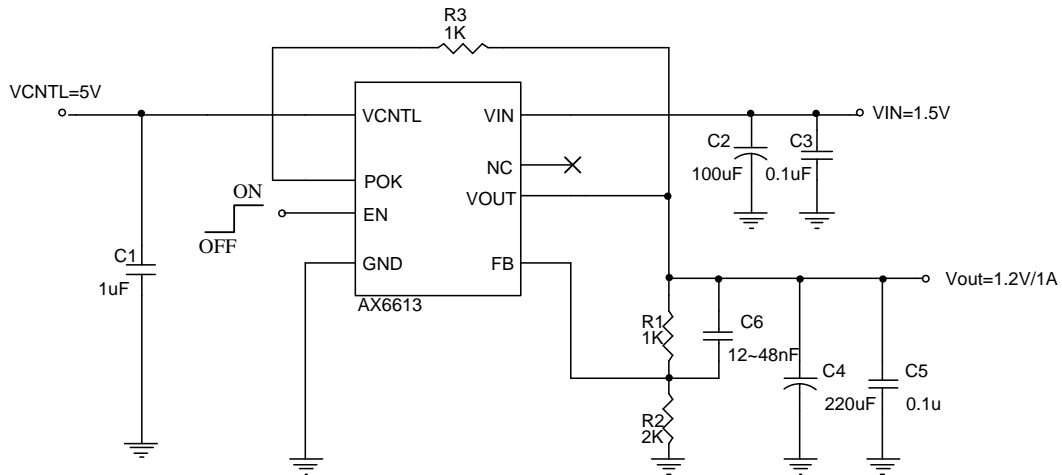
### ❖ ELECTRICAL CHARACTERISTICS

( $V_{CNTL} = 5V$ ,  $V_{IN} = 1.5V$ ,  $V_{OUT} = 1.2V$ ,  $T_A = 25^\circ C$  unless otherwise specified)

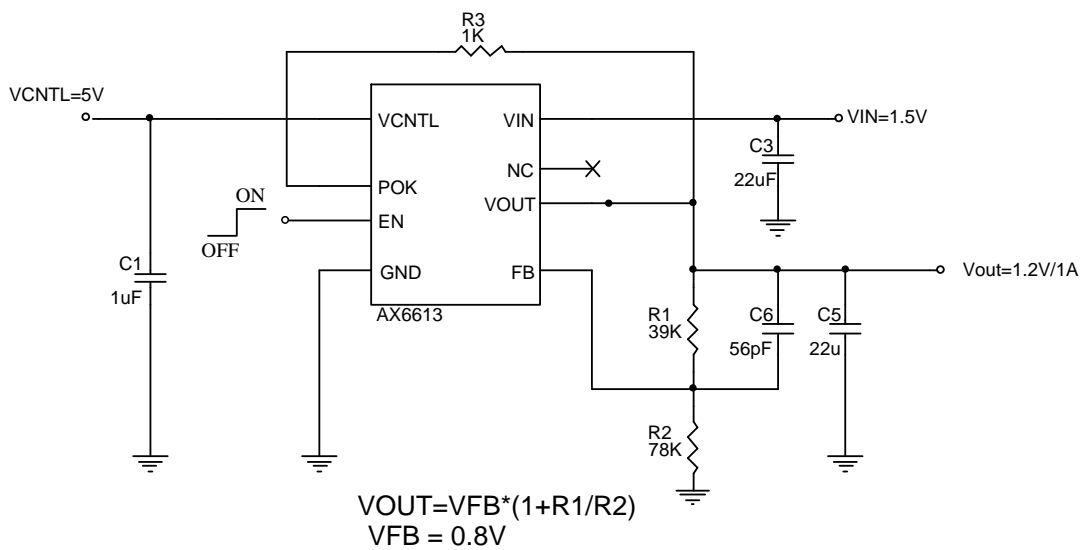
Characteristics	Symbol	Conditions	Min	Typ	Max	Units
$V_{CNTL}$ POR Threshold	$V_{CNTL}$		2.5	2.7	2.9	V
$V_{CNTL}$ POR Hysteresis	$V_{CNTL(hys)}$		-	0.4	-	V
$V_{IN}$ POR Threshold	$V_{IN}$		0.8	0.9	1.0	V
$V_{IN}$ POR Hysteresis	$V_{IN(hys)}$		-	0.5	-	V
$V_{CNTL}$ Nominal Supply Current	$I_{CNTL}$	EN= $V_{CNTL}$	0.4	1	2	mA
$V_{CNTL}$ Shutdown Current	$I_{SD}$	EN= 0V	-	10	30	uA
Feedback Voltage	$V_{FB}$	$V_{CNTL} = 3 \sim 6.0V$	0.784	0.8	0.816	V
Load Regulation		$I_{OUT} = 0A \sim 1A$	-	0.06	0.25	%
Dropout Voltage	$V_{DROP}$	$V_{OUT} < 2.0V, I_{OUT} = 1A$	-	200	250	mV
		$2.0V < V_{OUT} < 2.8V, I_{OUT} = 1A$	-	250	300	
$V_{OUT}$ Pull Low Resistance		EN=0V	-	90	120	$\Omega$
Soft Start Time	$T_{SS}$		-	2	-	mS
EN Pin Logic High threshold voltage	$V_{ENH}$	Enable	1.2	-	-	V
	$V_{ENL}$	Disable	-	-	0.4	
EN Hysteresis			-	50	-	mV
EN Pin Pull-Up Current	$I_{EN}$	EN=GND	-	10	-	uA
Current Limit	$I_{LIM}$	$V_{CNTL} = 3 \sim 6.0V$ , $T_J = -40 \sim 125^\circ C$	1.2	-	-	A
Ripple Rejection	$V_{IN}$	PSRR $F = 120Hz, I_{OUT} = 100mA$	-	70	-	dB
	$V_{CNTL}$		-	65	-	
Under-Voltage Threshold		VFB Falling	-	0.4	-	V
POK Threshold Voltage for Power OK	$V_{POK}$	VFB Rising	89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK	$V_{PNOK}$	VFB Falling	78%	81%	84%	VFB
POK Low Voltage		POK sinks 5mA	-	0.25	0.4	V
POK Delay Time	$T_{DELAY}$		0.8	2	10	mS
Thermal shutdown Temp	$T_{SD}$		-	150	-	$^\circ C$
Thermal Shutdown Hysteresis	$T_{SH}$		-	40	-	$^\circ C$

❖ APPLICATION CIRCUIT

1. Using an Output Capacitor with  $ESR \geq 20m\Omega$



2. Using an MLCC as the Output Capacitor



## ❖ FUNCTION PIN DESCRIPTIONS

### FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left( 1 + \frac{R1}{R2} \right) \quad (V)$$

Where R1 is connected from  $V_{OUT}$  to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100k $\Omega$ .

### VIN

Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

### VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

### POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the  $V_{POK}$  threshold or the falling FB voltage is below the  $V_{POK}$  threshold, indicating the output is not OK.

### EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, this pin is internal pulled up to  $V_{CNTL}$  voltage, enabling the regulator.

## VOUT

Output of the regulator. Please connect Pin 6 using wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

## ❖ FUNCTION DESCRIPTIONS

### Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at  $V_{CNTL}$  and  $V_{IN}$  pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the  $V_{CNTL}$  voltage falls below its falling POR threshold.

### Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2mS.

### Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from  $V_{IN}$  to  $V_{OUT}$ .

### Current-Limit

The AX6613 monitors the current via the output NMOS and limits the maximum current to prevent load and AX6613 from damages during overload or short circuit conditions.

### **Under-Voltage Protection (UVP)**

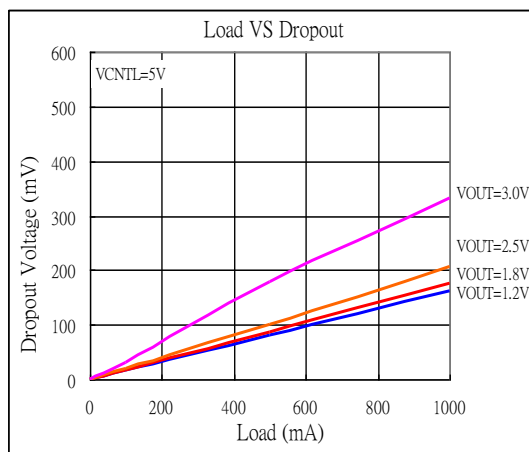
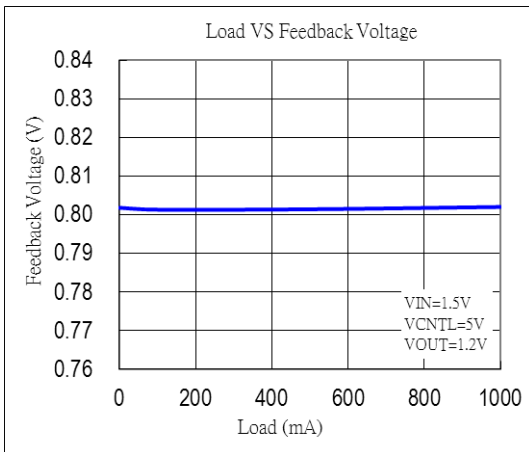
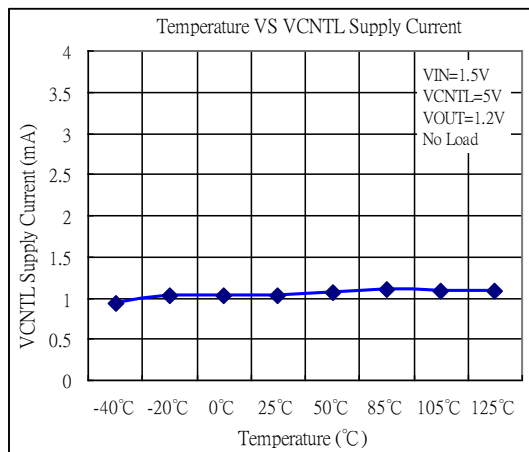
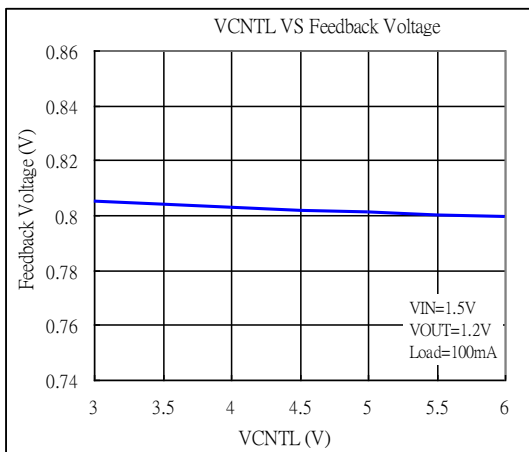
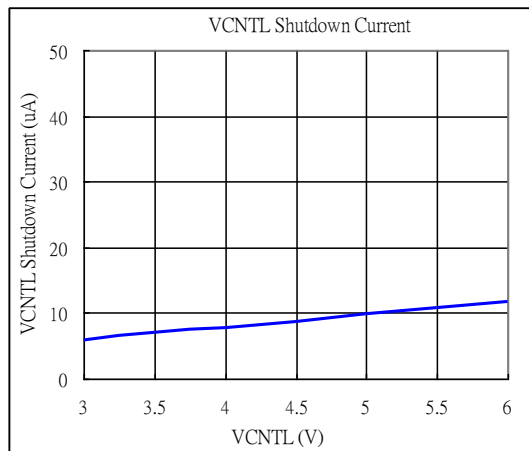
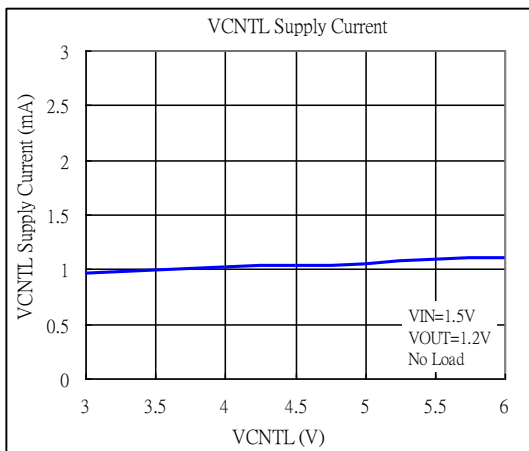
The AX6613 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the AX6613 starts a new soft-start to regulate output.

### **Thermal Shutdown**

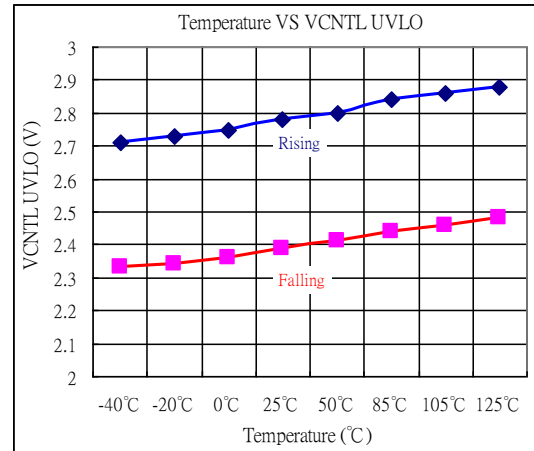
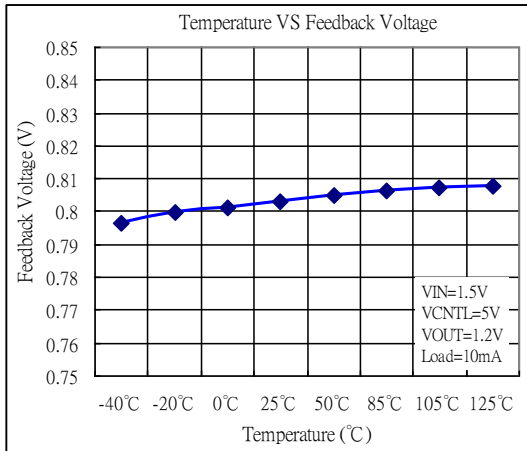
A thermal shutdown circuit limits the junction temperature of AX6613. When the junction temperature exceeds  $+150^{\circ}\text{C}$ , a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by  $40^{\circ}\text{C}$ , resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed



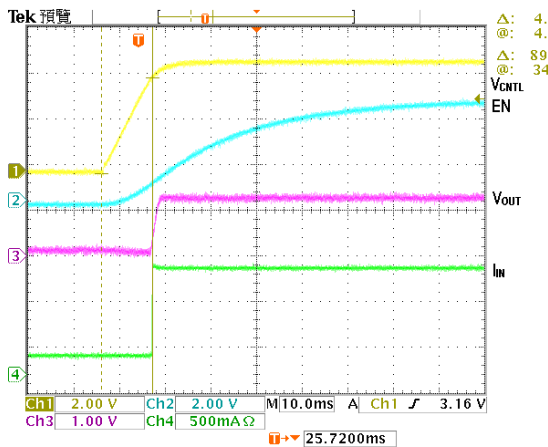
❖ TYPICAL CHARACTERISTICS



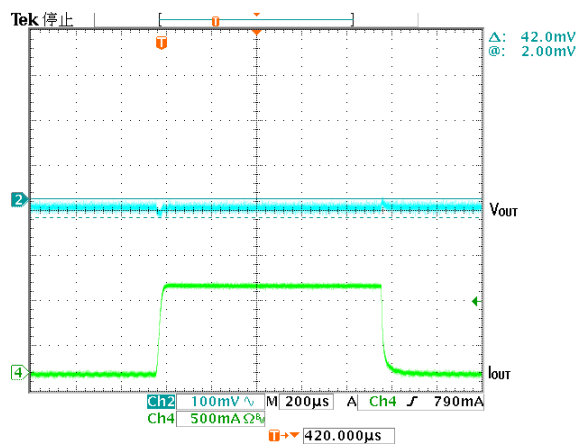
❖ TYPICAL CHARACTERISTICS (CONTINUOUS)



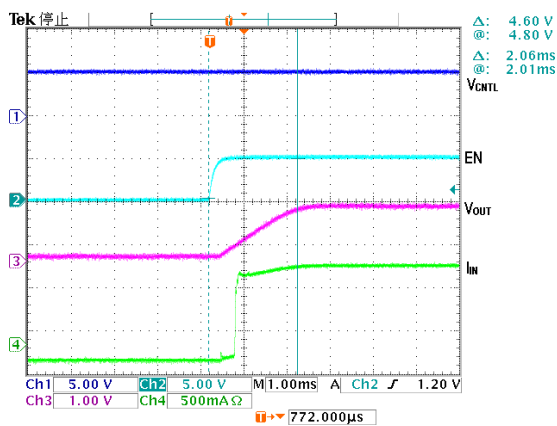
Power -ON  
( $V_{IN}=1.5V, V_{CNTL}=5V, V_{OUT}=1.2V, Load=1A$ )



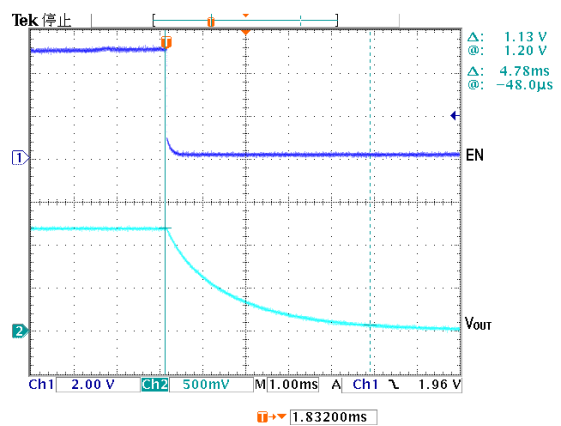
Load Transient  
( $V_{IN}=1.5V, V_{CNTL}=5V, V_{OUT}=1.2V, Load=10m\sim 1A$ )



Enable -ON  
( $V_{IN}=1.5V, V_{CNTL}=5V, V_{OUT}=1.2V, Load=1A$ )

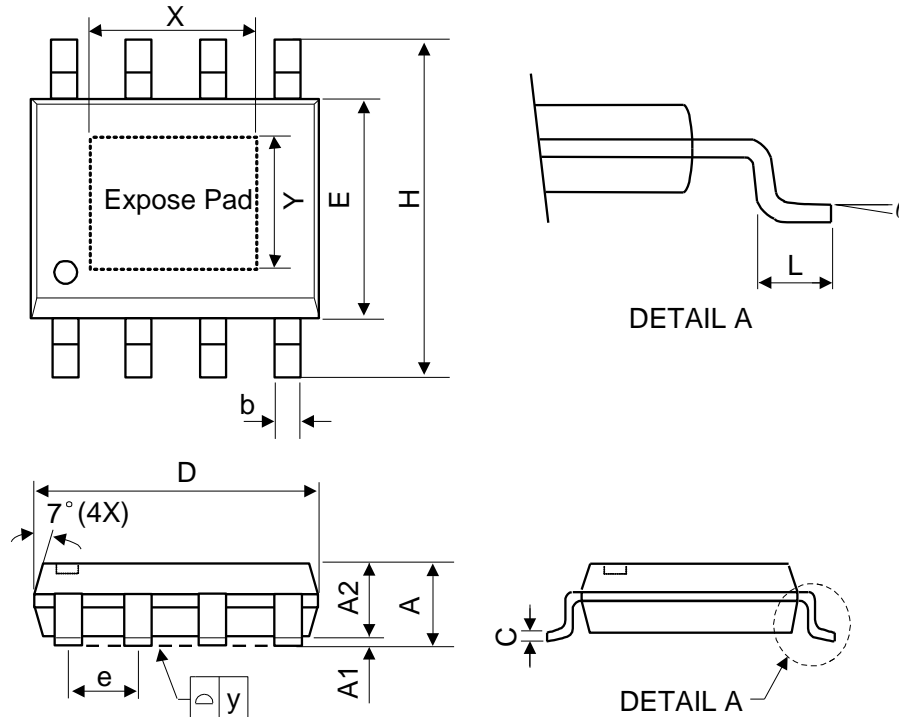


Enable -OFF  
( $V_{IN}=1.5V, V_{CNTL}=5V, V_{OUT}=1.2V, No\ Load$ )



❖ PACKAGE OUTLINES

(1) SOP-8L-EP

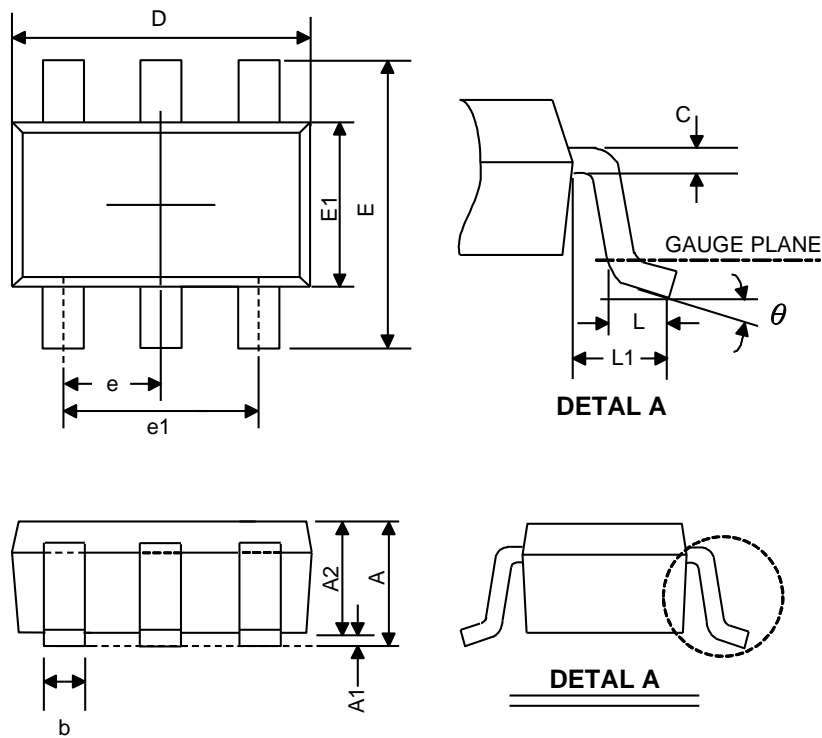


Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0	-	0.15	0	-	0.06
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
X	-	2.34	-	-	0.092	-
Y	-	2.34	-	-	0.092	-
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side

JEDEC outline: MS-012 BA

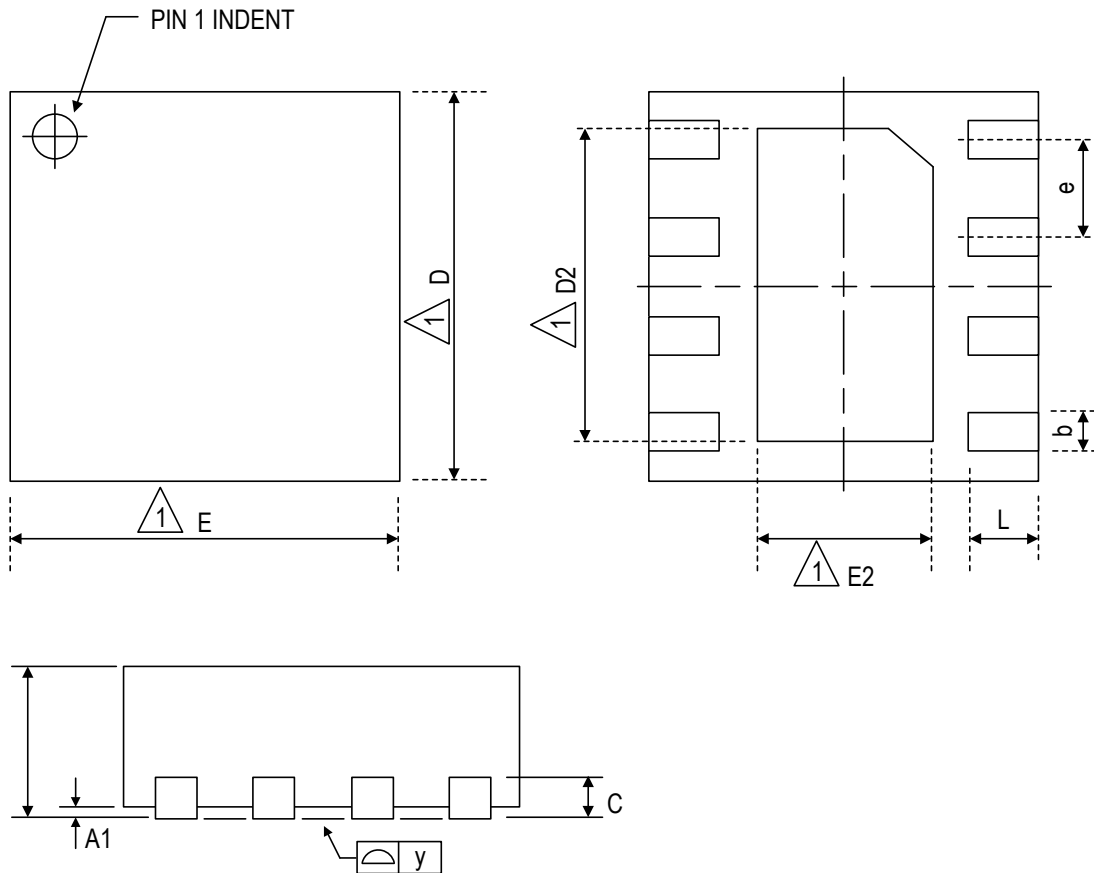
(2) SOT-23-6L



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.45	-	-	0.057
A1	0.00	-	0.15	0	0.003	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.40	0.50	0.012	0.016	0.020
C	0.08	-	0.22	0.003	0.006	0.009
D	2.70	2.90	3.10	0.106	0.114	0.122
E1	1.40	1.60	1.80	0.055	0.063	0.071
E	2.60	2.80	3.00	0.102	0.110	0.118
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.50	0.60	0.70	0.020	0.024	0.028
e1	1.9 BSC			0.075 BSC		
e	0.95 BSC			0.037 BSC		
θ	0°	4°	8°	0°	4°	8°

JEDEC outline: MO-178 AB

(3) TDFN-8L (2\*2 0.75mm)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.19	0.20	0.25	0.007	0.008	0.010
D	1.90	2.00	2.10	0.075	0.079	0.082
D2	1.55	1.60	1.65	0.061	0.063	0.065
E	1.90	2.00	2.10	0.075	0.079	0.082
E2	0.85	0.90	0.95	0.033	0.035	0.037
e	-	0.50	-	-	0.020	-
L	0.30	0.35	0.40	0.012	0.014	0.016
y	0.00	-	0.075	0	-	0.003