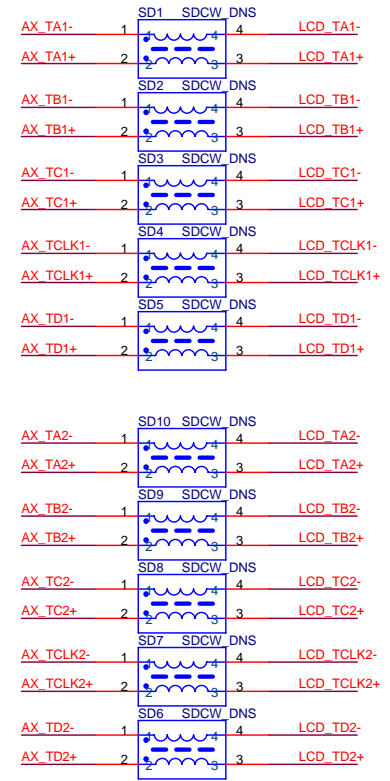
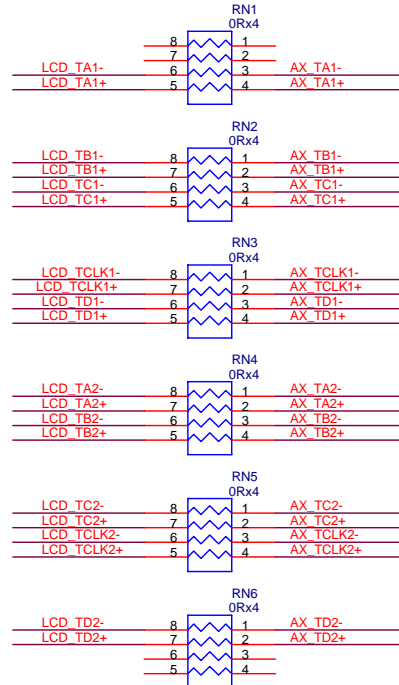
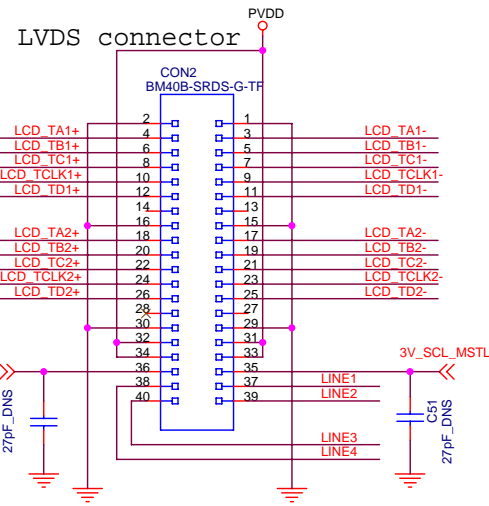
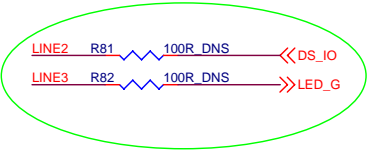
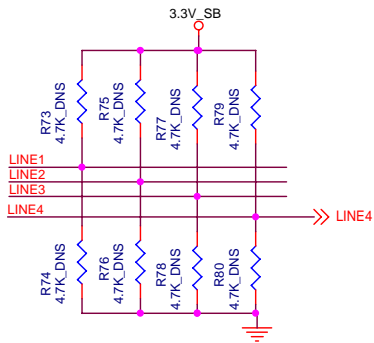
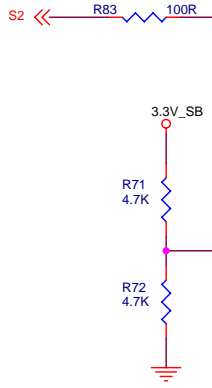
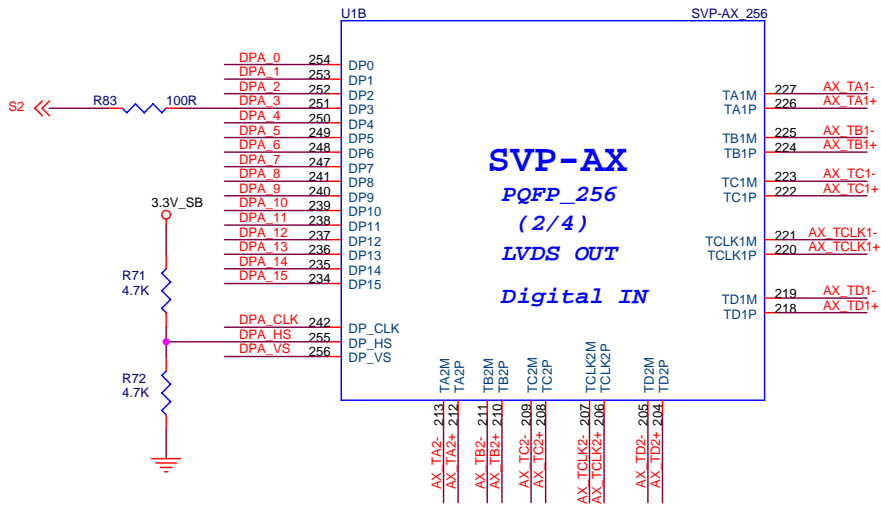
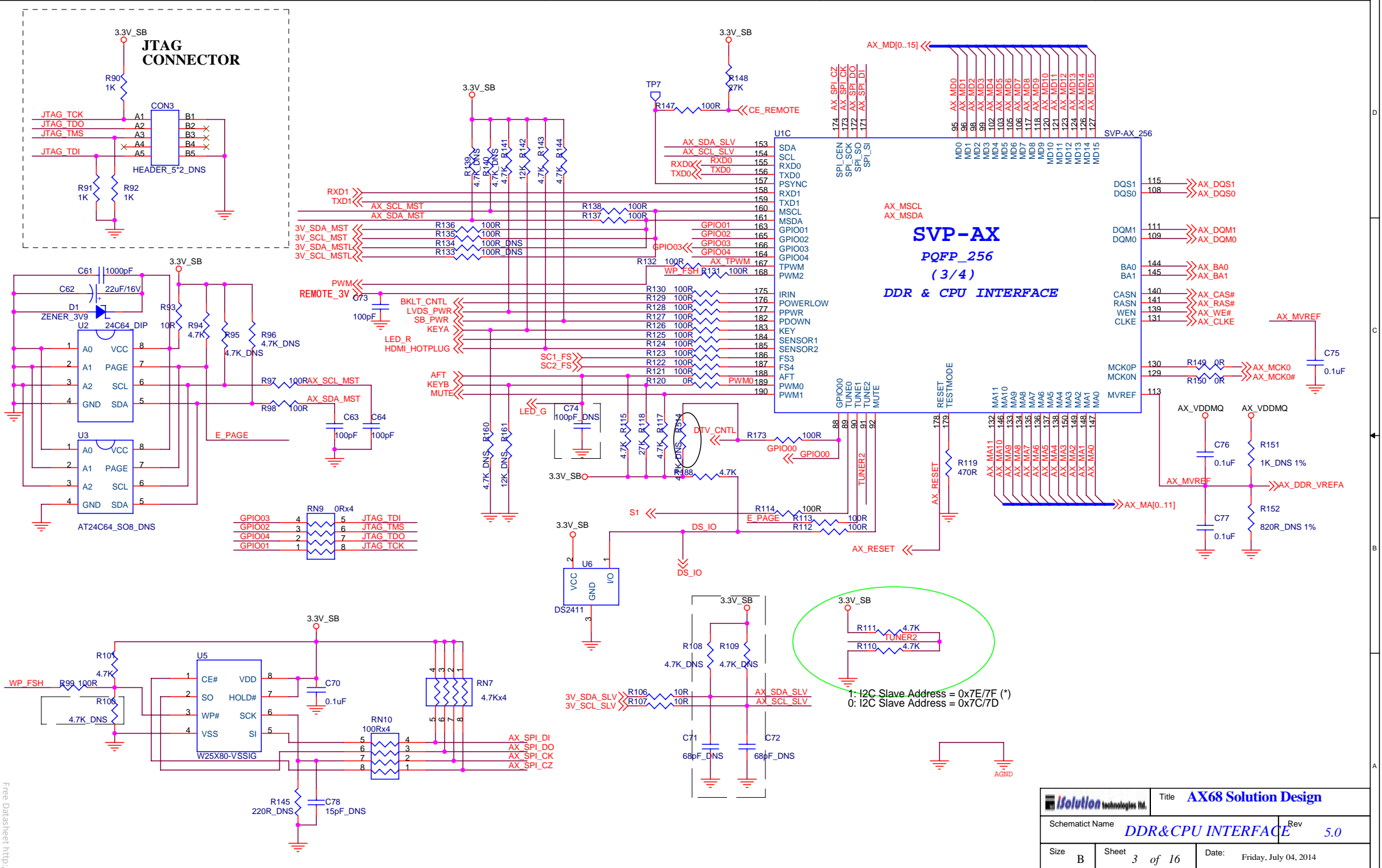


Pin Name	Pin No.	DEFINITION IN LCD301
CVBS1	52	MAIN TUNER INPUT
Y_G3	42	SVIDEO Y INPUT
PB_B3	43	SCART1 CVBS INPUT
PR_R3	44	SCART2 CVBS INPUT
FB1	57	SCART1 FB INPUT
FB2	56	SCART2 or 3 Chroma INPUT
FS1	55	SCART1 FS INPUT
FS2	54	SCART2 FS INPUT

		Title AX68 Solution Design	
Schematic Name ANALOG CHANNEL		Rev 5.0	
Size B	Sheet 1 of 16	Date: Friday, July 04, 2014	



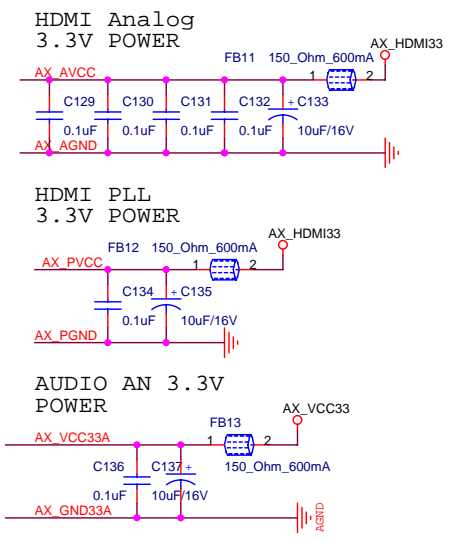
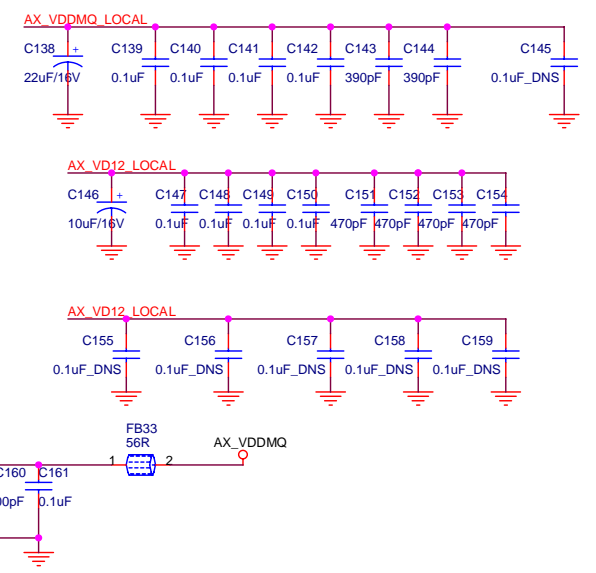
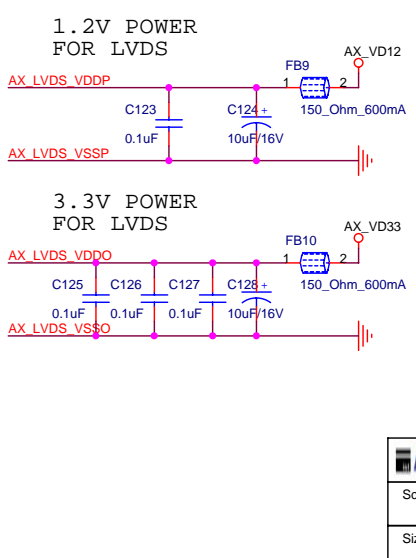
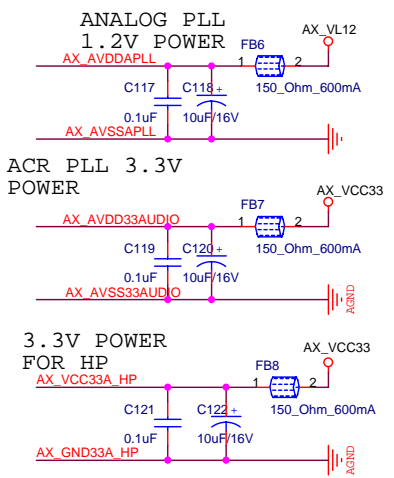
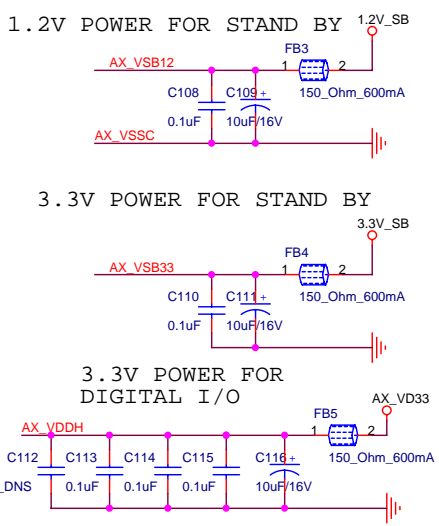
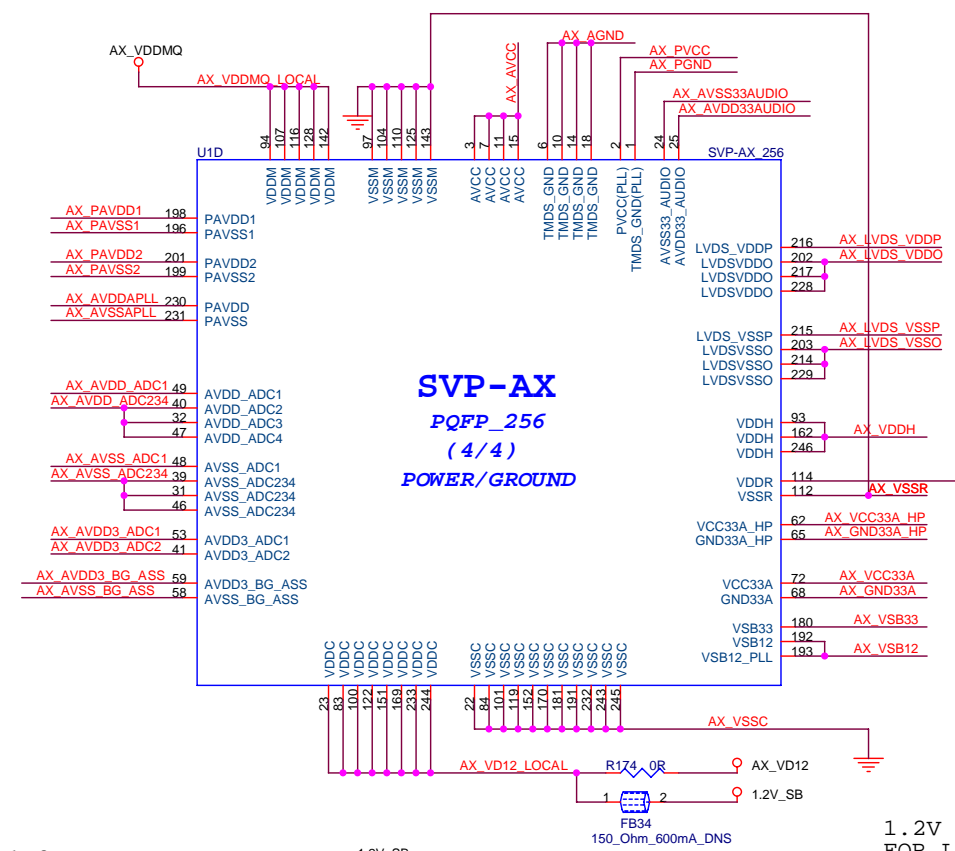
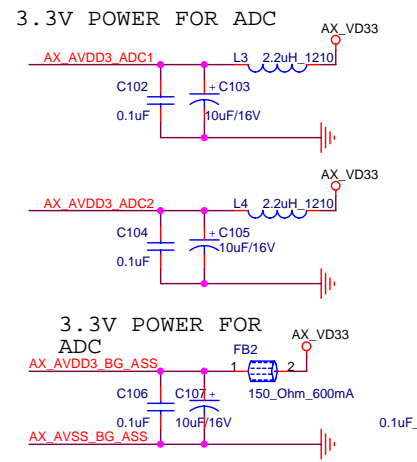
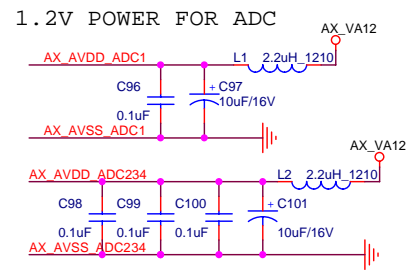
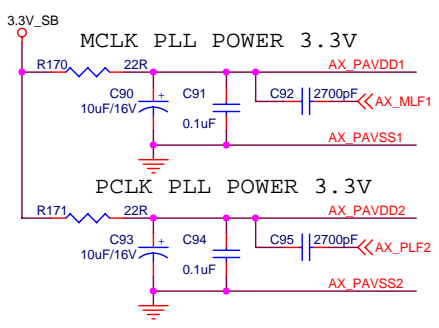
		Title AX68 Solution Design	
Schematic Name LVDS INTERFACE		Rev 5.0	
Size B	Sheet 2 of 16	Date: Friday, July 04, 2014	



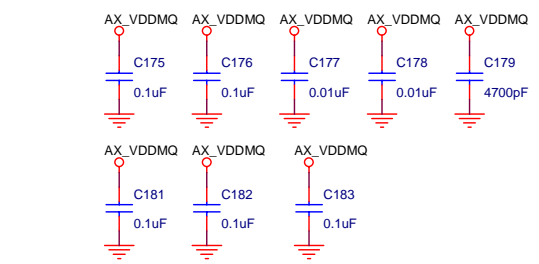
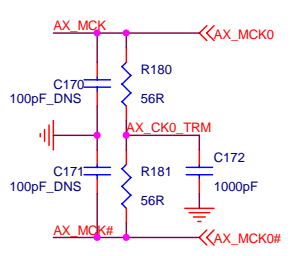
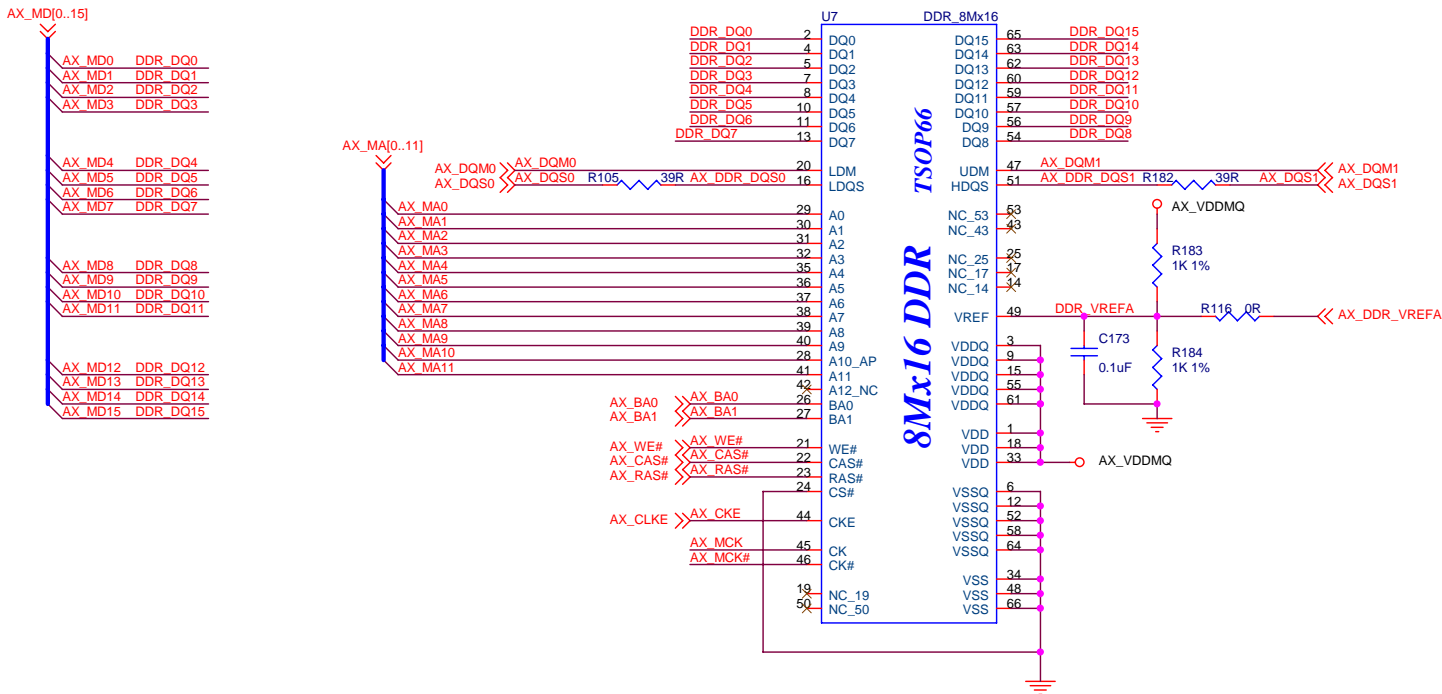
SVP-AX
PQFP_256
(3/4)
DDR & CPU INTERFACE

1: I2C Slave Address = 0x7E/7F (*)
 0: I2C Slave Address = 0x7C/7D

		Title AX68 Solution Design	
Schematic Name DDR&CPU INTERFACE		Rev 5.0	
Size B	Sheet 3 of 16	Date:	Friday, July 04, 2014

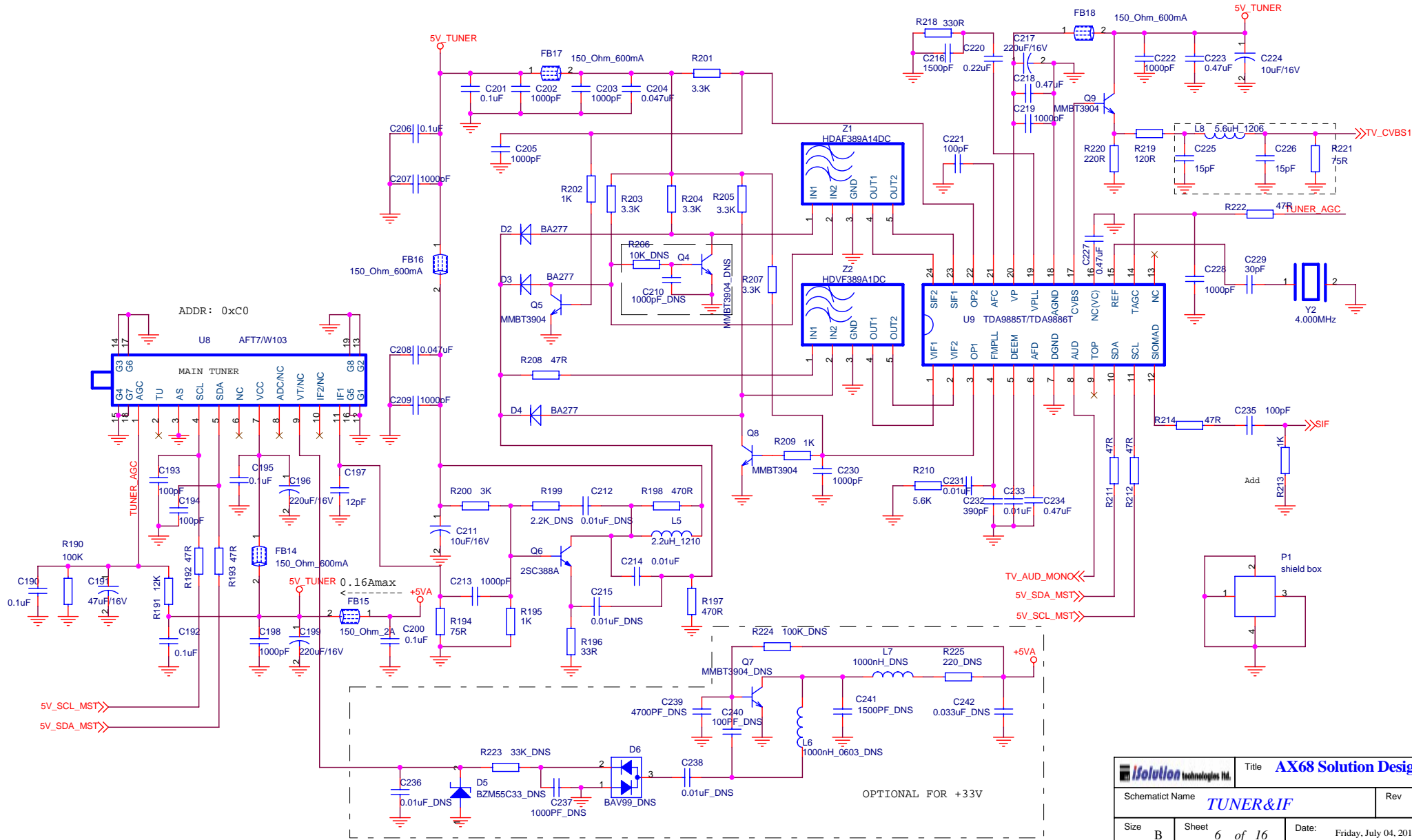


		Title AX68 Solution Design	
Schematic Name AX68 POWER		Rev 5.0	
Size B	Sheet 4 of 16	Date: Friday, July 04, 2014	

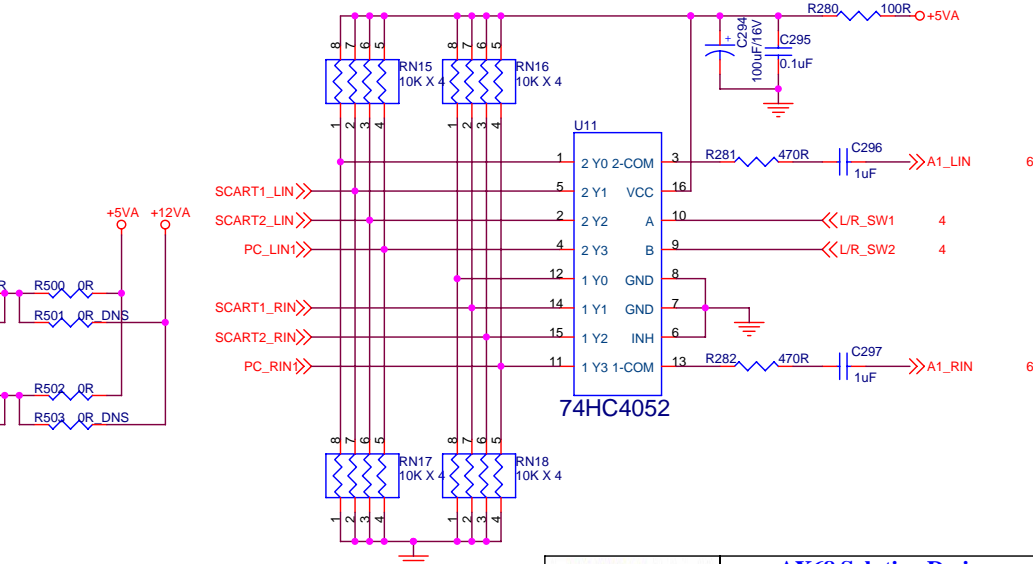
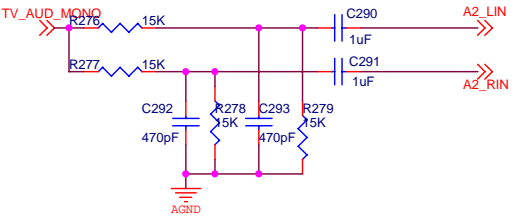
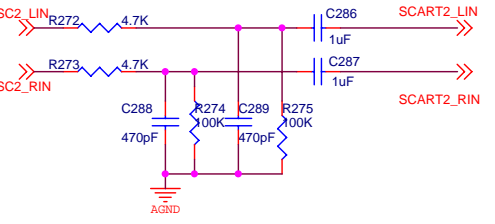
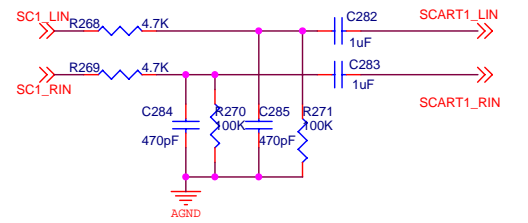
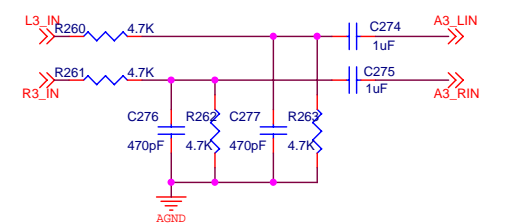
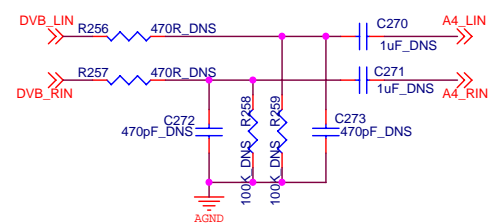
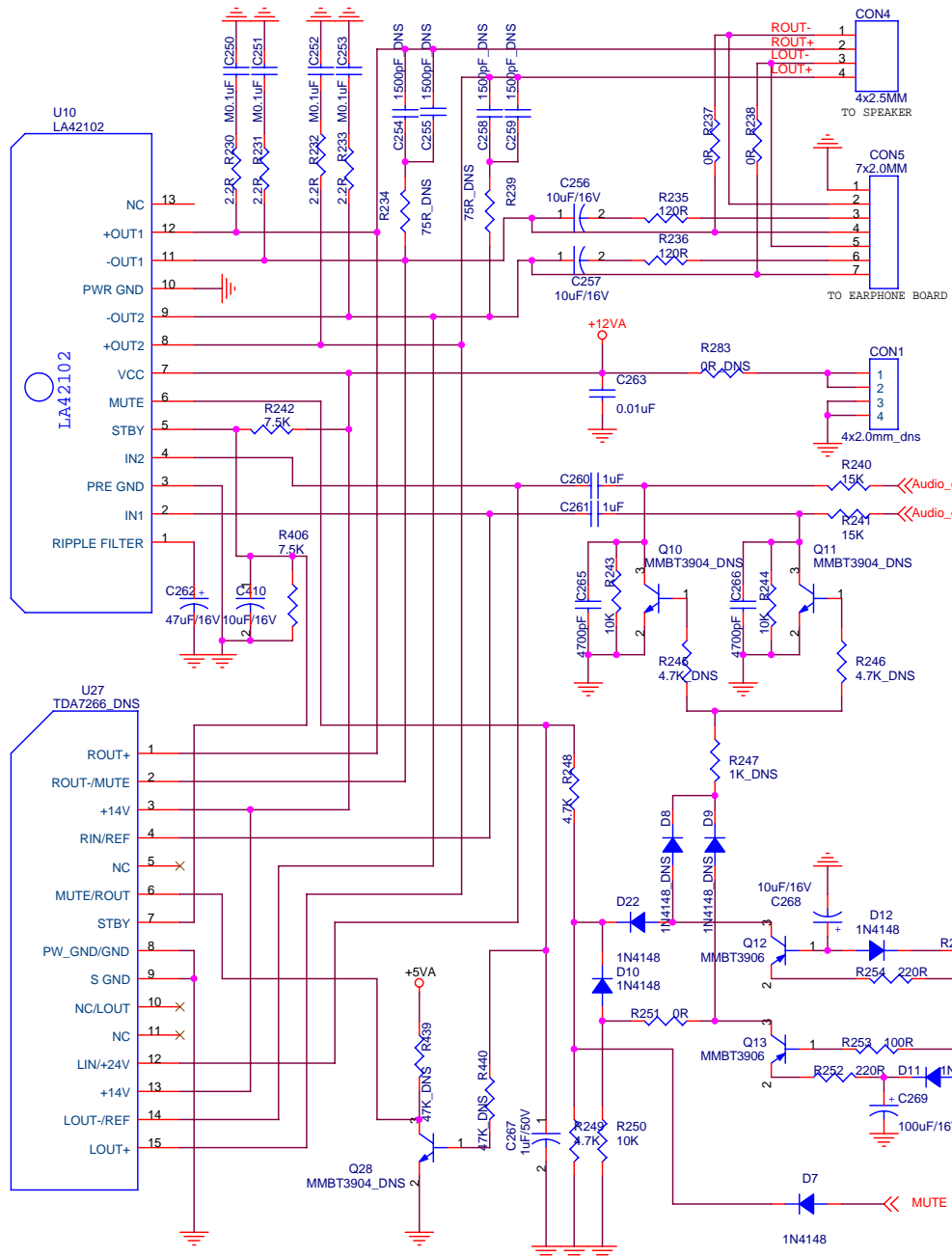


DDR DECOUPLING CAPACITORS

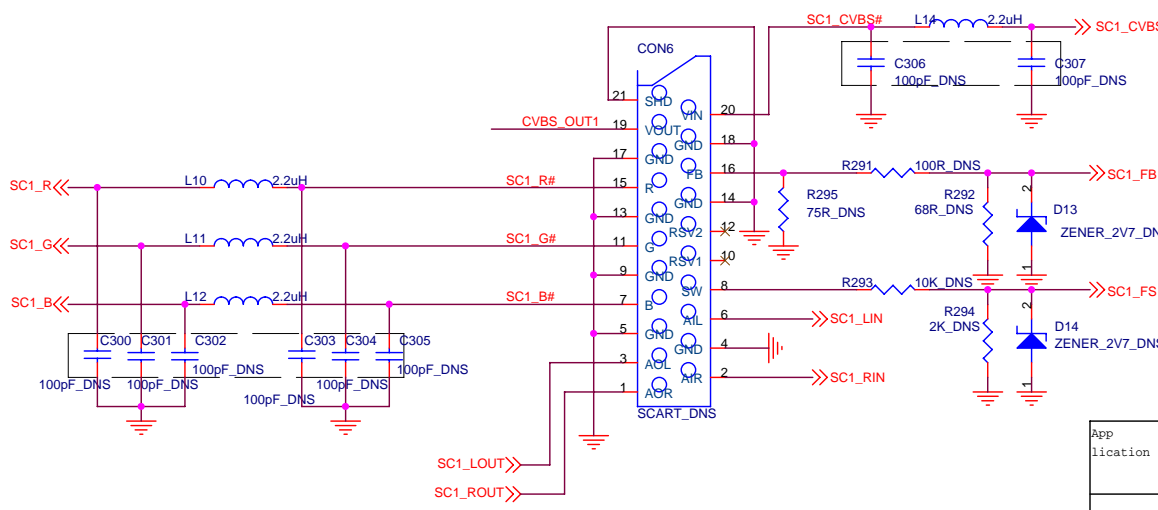
		Title AX68 Solution Design	
Schematic Name DDR MEMORY		Rev 5.0	
Size B	Sheet 5 of 16	Date: Friday, July 04, 2014	



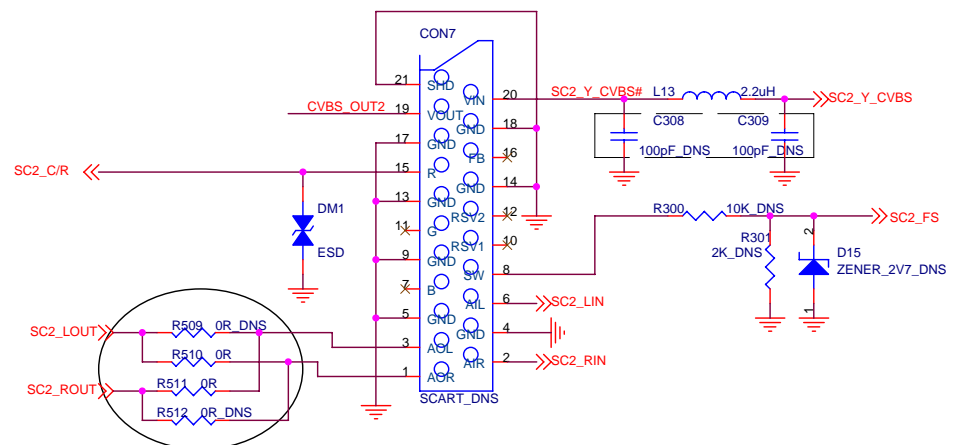
		Title AX68 Solution Design	
Schematic Name TUNER&IF		Rev 5.0	
Size B	Sheet 6 of 16	Date: Friday, July 04, 2014	



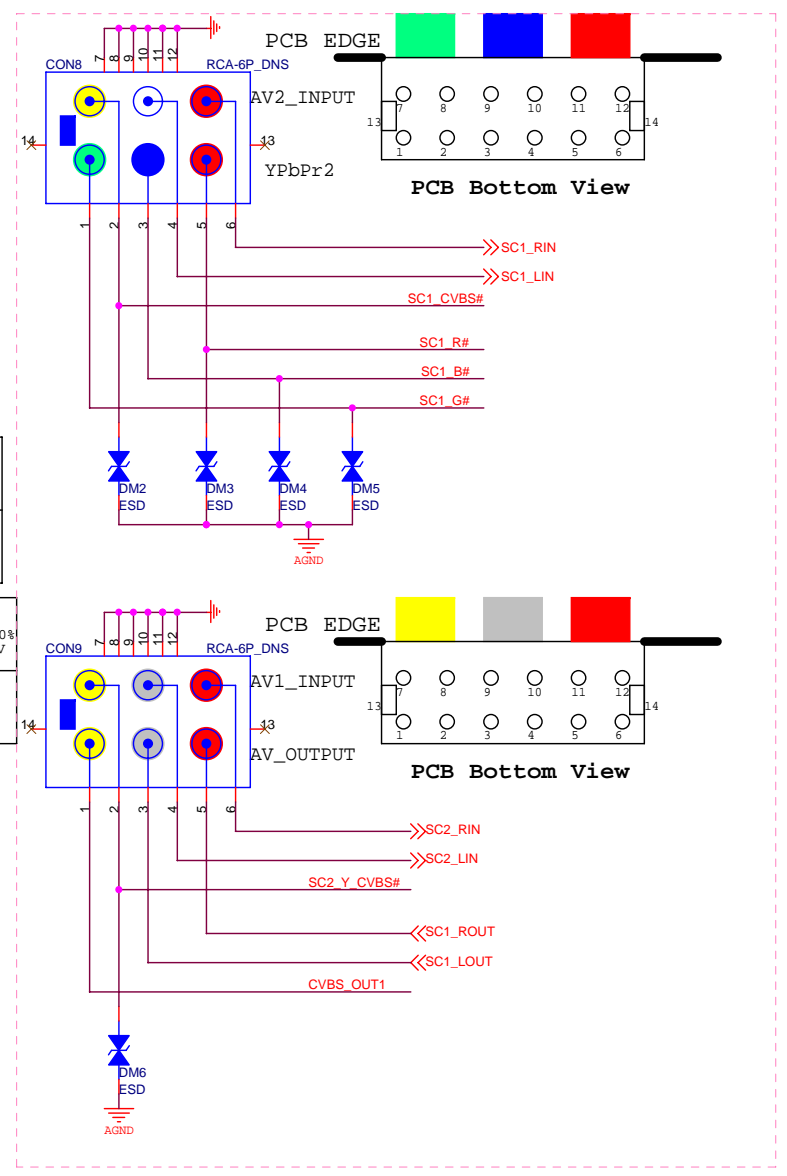
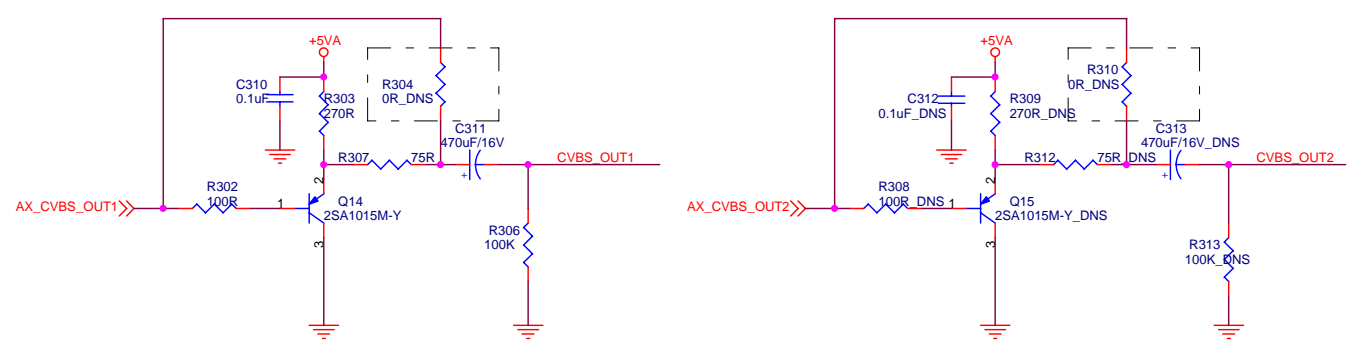
		Title AX68 Solution Design	
Schematic Name AUDIO		Rev 5.0	
Size B	Sheet 7 of 16	Date:	Friday, July 04, 2014



App lication	SCART input voltage range	voltage range at pin
AV MODE	0...12 V	0...1.304V

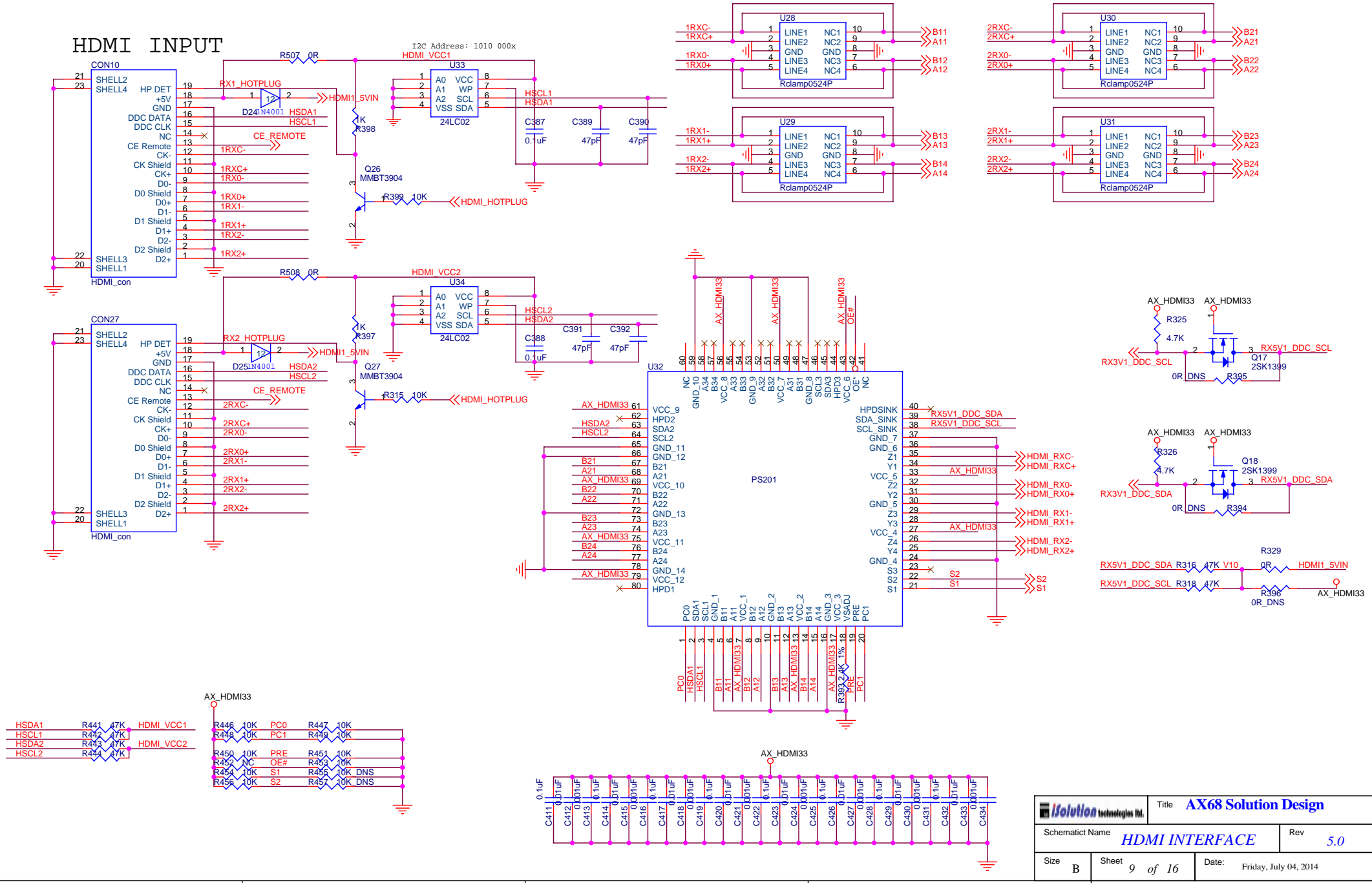


ADC-slices	0...16.7% of 1.304V	37.5...58.3% of 1.304V	79.2...100% of 1.304V
	LOW TV mode	Middle Wide screen	High A/V_MODE

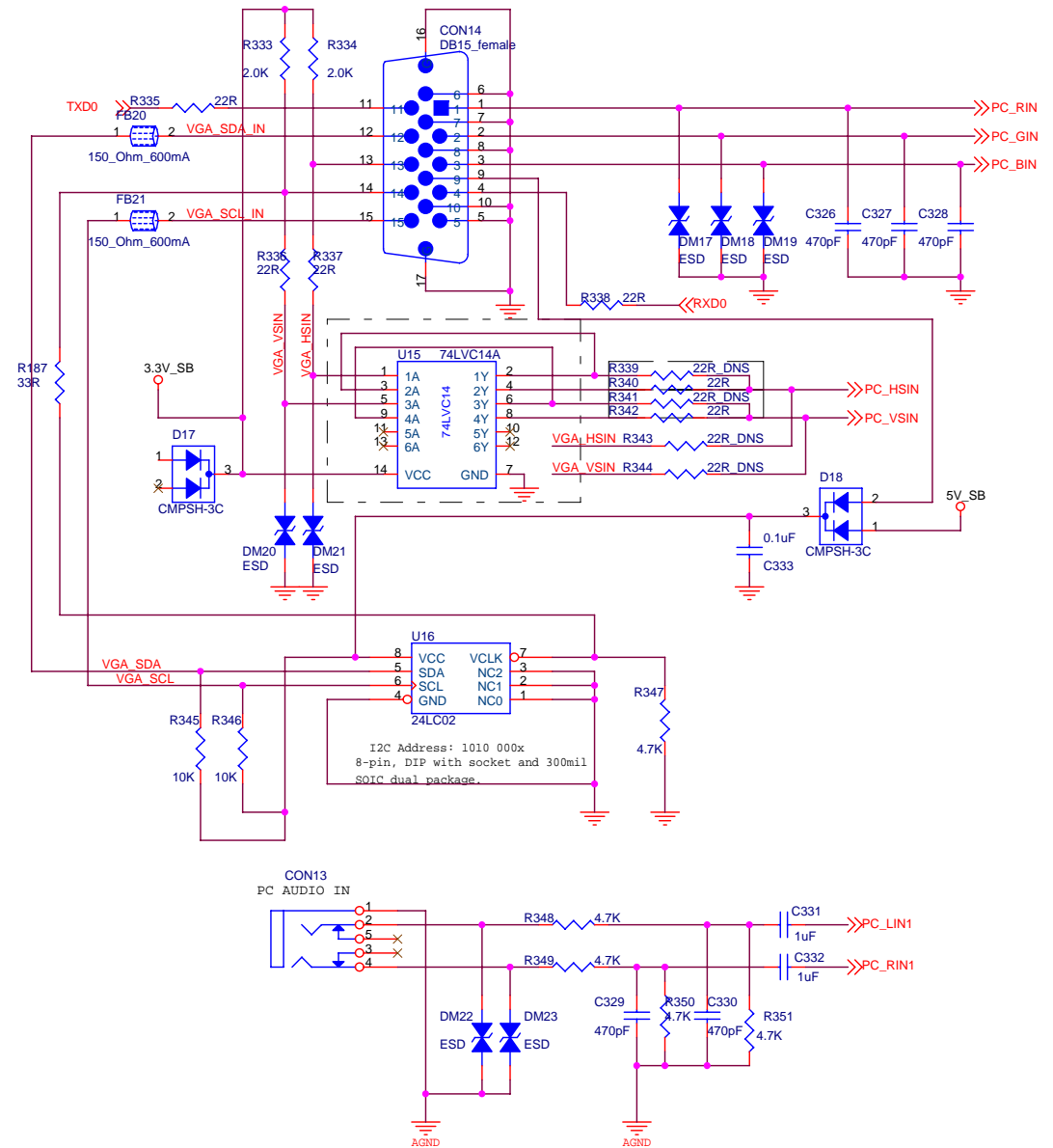
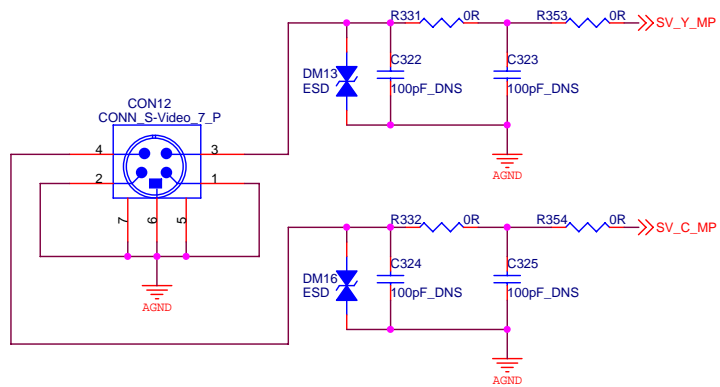
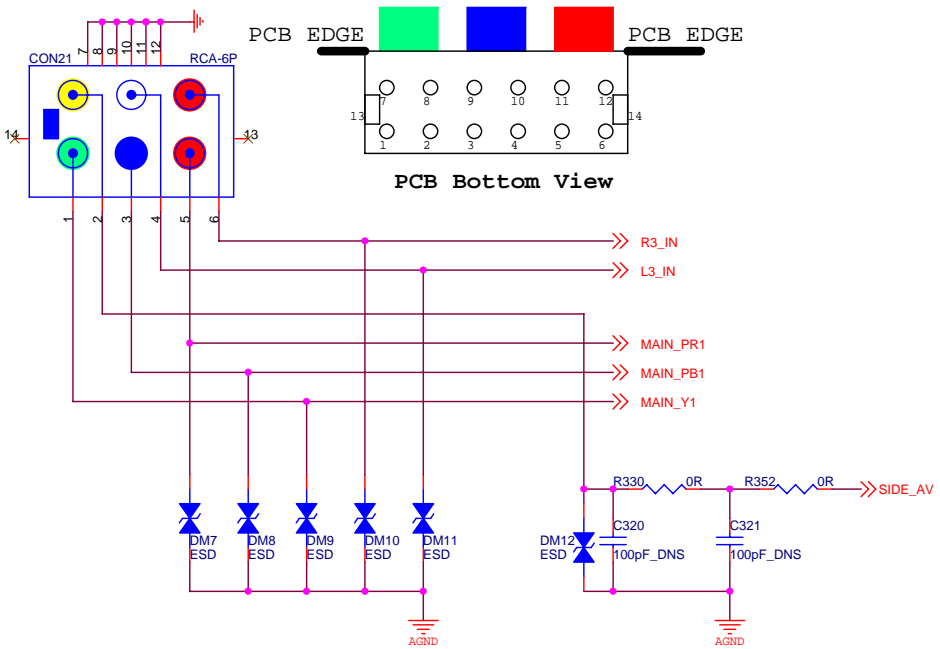


		Title AX68 Solution Design	
Schematic Name SCART&AV		Rev 5.0	
Size B	Sheet 8 of 16	Date: Friday, July 04, 2014	

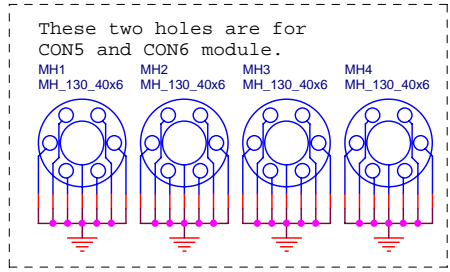
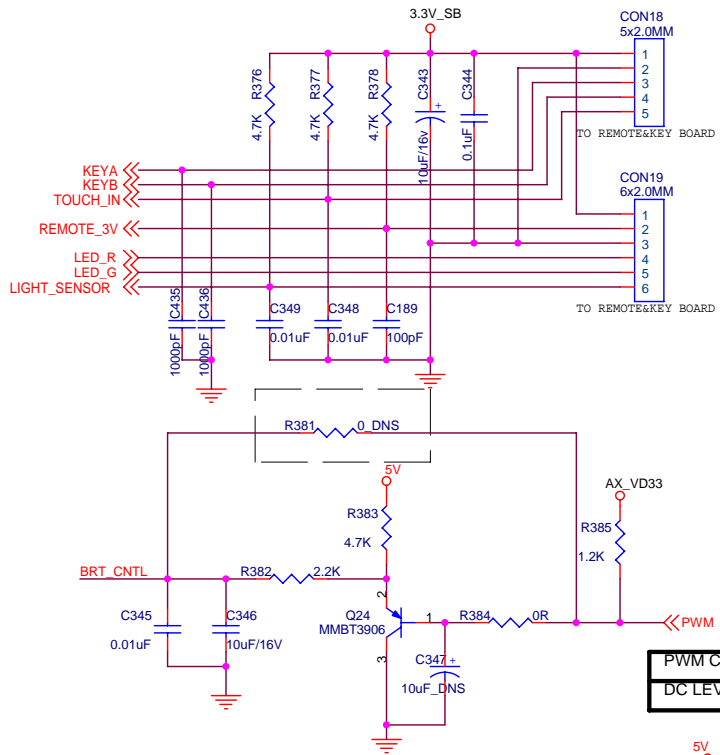
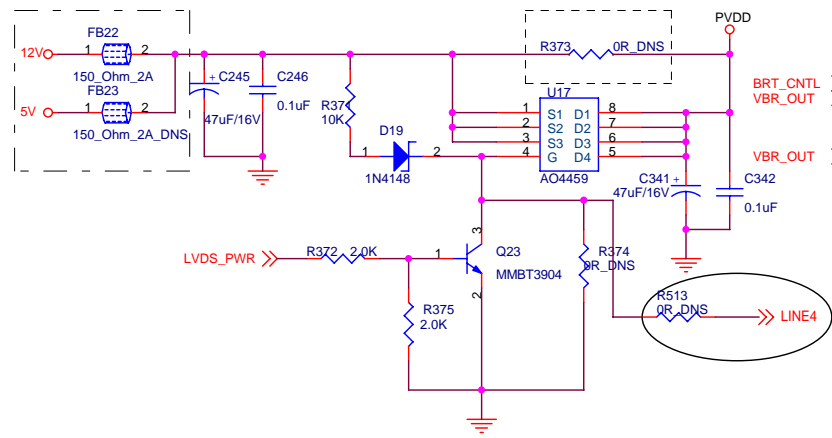
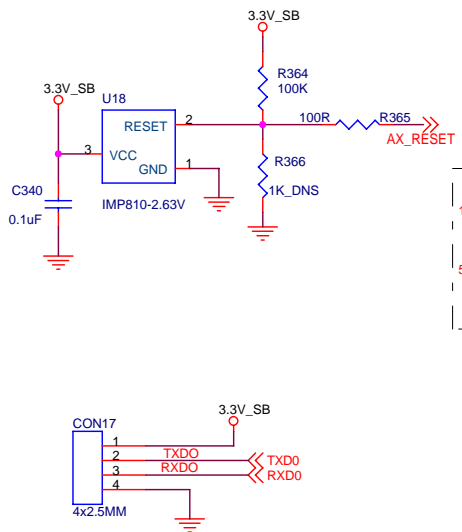
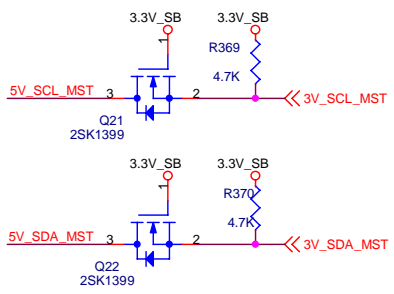
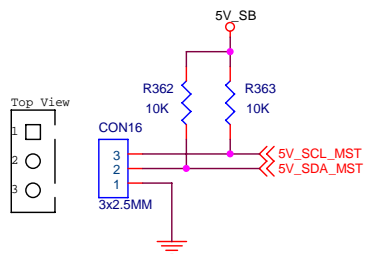
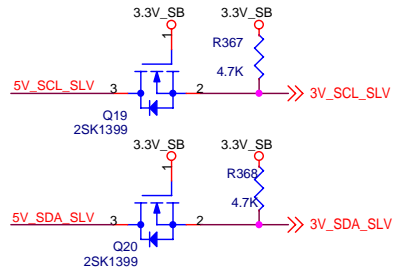
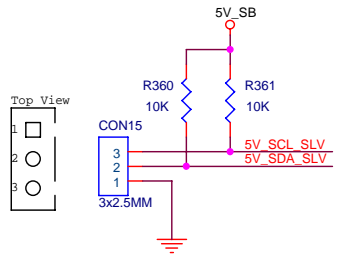
HDMI INPUT



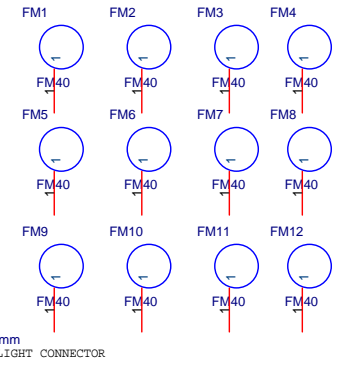
		Title AX68 Solution Design	
Schematic Name HDMI INTERFACE		Rev 5.0	
Size B	Sheet 9 of 16	Date: Friday, July 04, 2014	



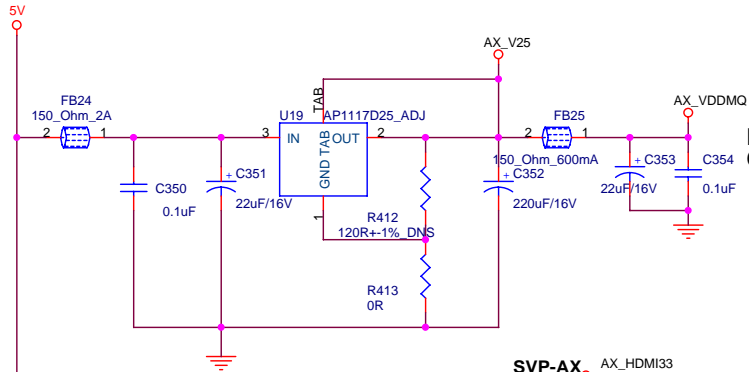
		Title AX68 Solution Design	
Schematic Name VGA&AV		Rev 5.0	
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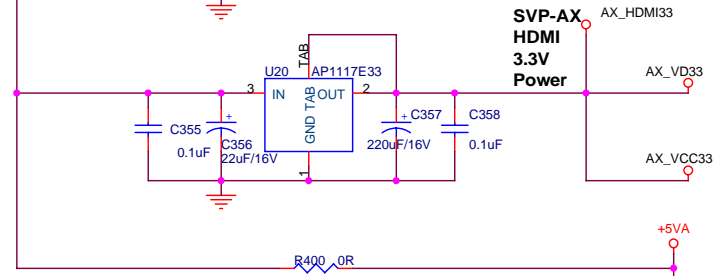
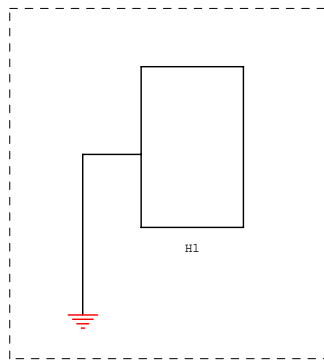
PWM CNTL
DC LEVEL CNTL



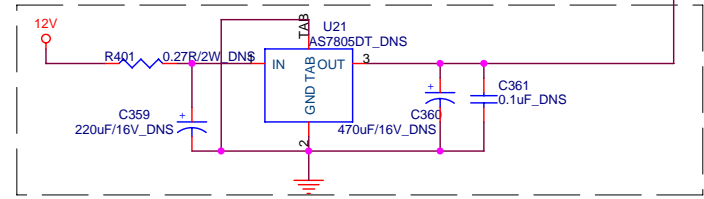
		Title AX68 Solution Design	
Schematic Name OTHER INTERFACE		Rev 5.0	
Size B	Sheet 11 of 16	Date: Friday, July 04, 2014	



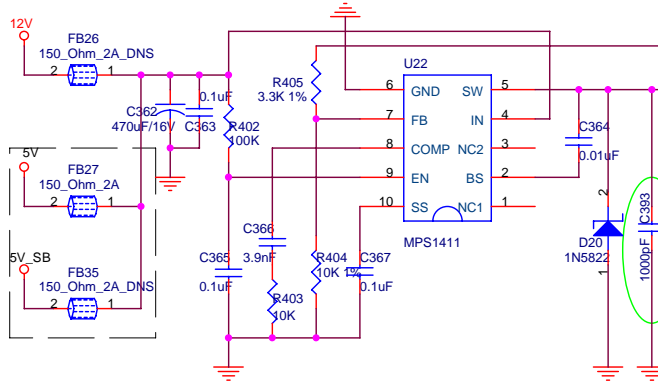
Power for DDR Core Logic



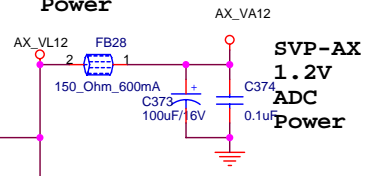
SVP-AX HDMI 3.3V Power



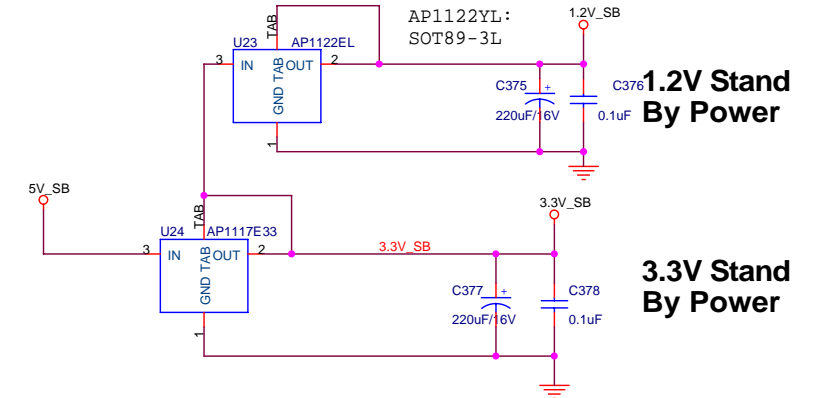
SVP-AX 3.3V Power



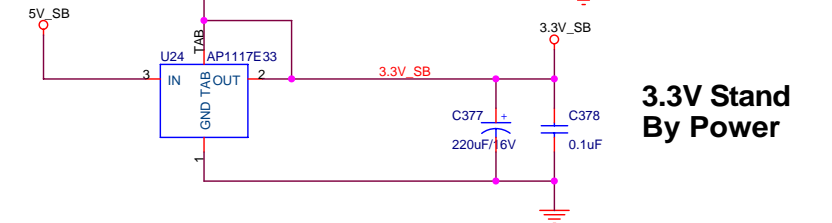
SVP-AX 1.2V Core Power



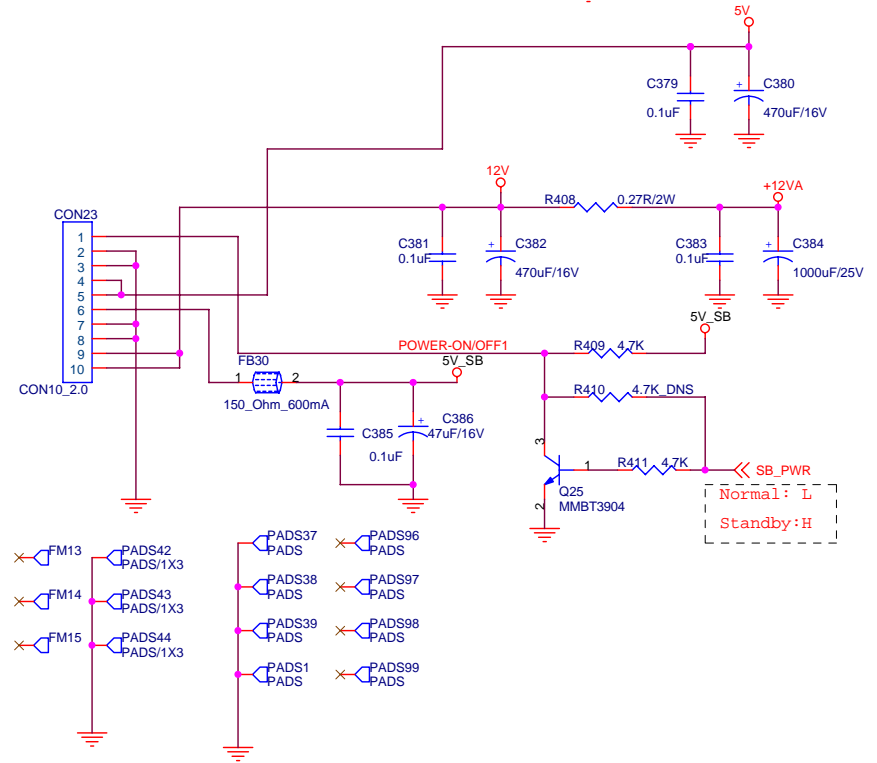
SVP-AX 1.2V ADC Power



1.2V Stand By Power

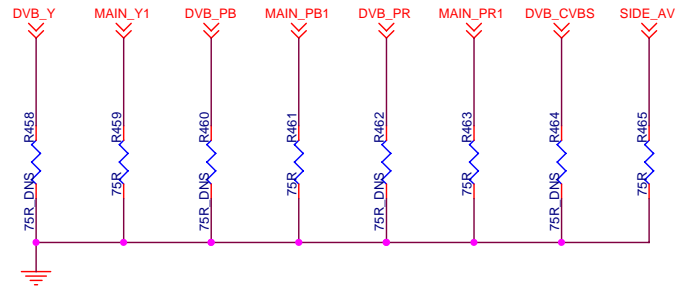
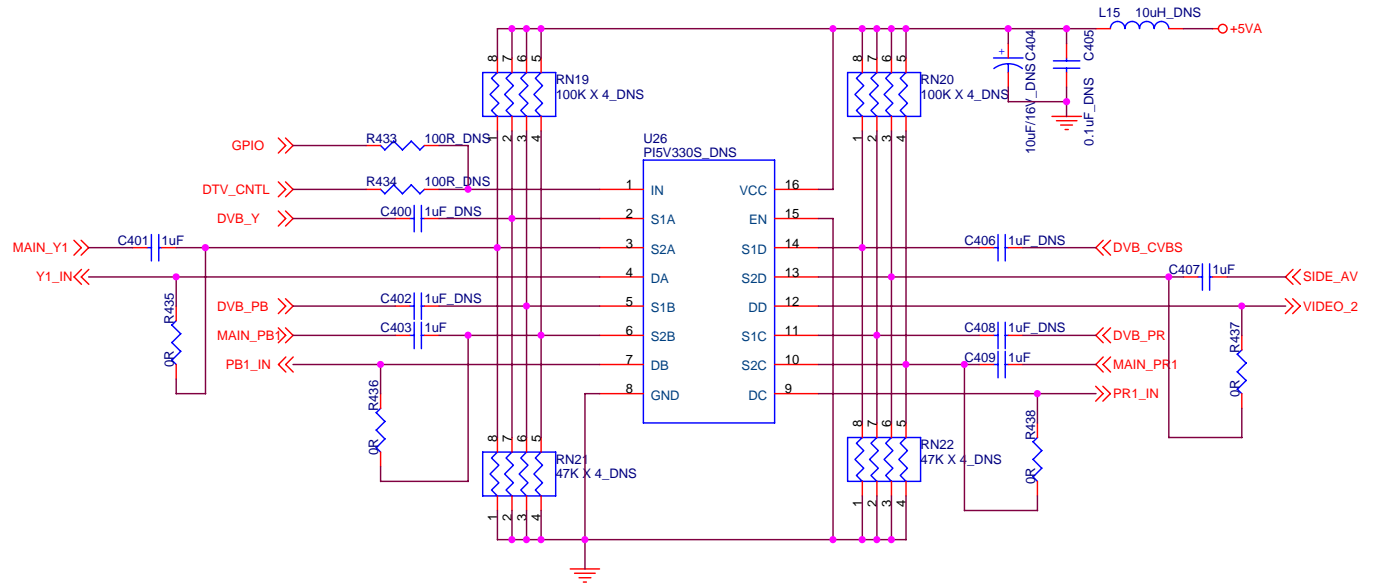
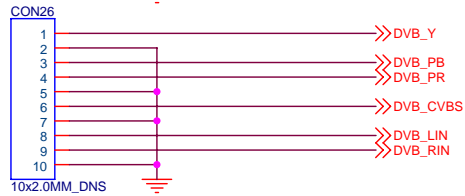
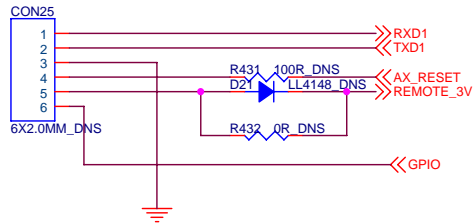
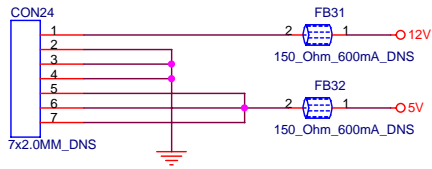


3.3V Stand By Power



Normal: L
Standby: H

		Title AX68 Solution Design	
Schematic Name TOTAL POWER		Rev 5.0	
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		Title AX68 Solution Design	
Schematic Name DTV INTERFACE		Rev 5.0	
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