# 5-Port 10/100BASE Ethernet Switch Controller

**Document No.: AX615-13 / V1.3 / Aug. 11 '99**

## Features

- Support 5 10/100 Mbps Ethernet ports with RMII/MII interface
  - ✓ Provides packet switching functions between 5 10/100 Mbps, auto-negotiated ports
  - ✓ Ideal for SOHO switches and its application
- Build in 5-ports 10/100Mbps Switch engine with following features
  - ✓ Low cost SSRAM interface to reduce system cost
  - ✓ One or two 64K*32bit SSRAM to buffer packets
  - ✓ 4/8 K MAC address look up Table is supported
  - ✓ Address mapping of look up table can be linear or use hash algorithm
  - ✓ Auto learning and filtering
  - ✓ Aging the look up table is supported optionally
  - ✓ Aging time can be 1min to 640 mins 7 steps
  - ✓ Three forwarding modes are supported : Store-and-Forward, Fragment-Free and Auto Forward which is based on network quality
  - ✓ Flow-control is supported optionally
  - ✓ 802.3x flow control is supported when running in full-duplex mode
  - ✓ Back-pressure base flow control is supported when running in half-duplex mode
  - ✓ Ext. Buffer Memory auto testing
  - ✓ Routing and Learning at wire speed (148800 packets/sec at 100Mbps)
- LED display buffer utilization (%) for whole system and external SSRAM test.
- Power on LED diagnosis. All the LED display will follow the "ON-OFF-ON-OFF-Normal" operation procedure during/after power on reset
- 60MHz Operation, 3.3volt, 208-pin PQFP

## Product description

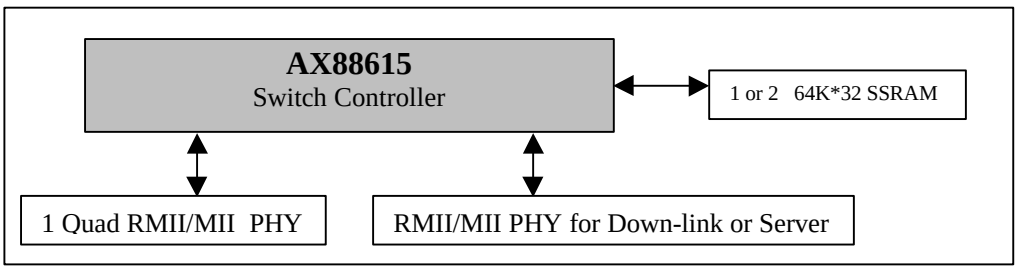
The AX88615 is a 5-ports 10/100 Mbps Ethernet switch with MII PHY or RMII PHY. It is design for low cost dumb Switch application, e.g. SOHO Ethernet Switch, with low cost 64K*32 SSRAM buffer memory.

## Key Applications

- ✓ SOHO Ethernet Switch
- ✓ IP Router

## System Block Diagram

5 Port 10/100Mb SOHO Switch






**ASIX ELECTRONICS CORPORATION** **First Released Date : APR/02/1999**
**2F, NO.13, Industry East Rd. II, Science-based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.**
**TEL: 886-3-579-9500** **FAX: 886-3-579-9558** **http://www.asix.com.tw**

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# FIGURES

# 1.0 AX88615 Overview

## 1.1 General Description

The AX88615 is a 5-ports 10/100 Mbps Ethernet switch with MII PHY or RMII PHY. A low cost Fast Ethernet switch can be implemented by using the AX88615 and low cost 64Kx32 SSRAM .

Data received from the MAC interface is stored in the external memory. All ports support multiple MAC addresses. The switch provides a look-up table for 8K MAC addresses with two 64Kx32 SSRAMs. The AX88615 provides three frame forwarding mode: store-and-forward mode, safe cut-through (fragment free) mode and dynamic-select-mode (auto). The dynamic-select-mode means the switch selects optimizes mode for forwarding packages automatically according to Network quality.

During transmission, the data is obtained from the buffer memory and routed to the destination port. For half-duplex operation, the MAC control will back off and retransmit in accordance to the IEEE802.3 CSMA/CD if collision occurs.

The AX88615 provides two flow control methods. For half-duplex operation, an optional jamming based flow control is available to avoid loss of data. This is also well known as back pressure. In the full-duplex mode, AX88615 utilizes IEEE802.3X as the flow control mechanism.

## 1.2 AX88615 Block Diagram:

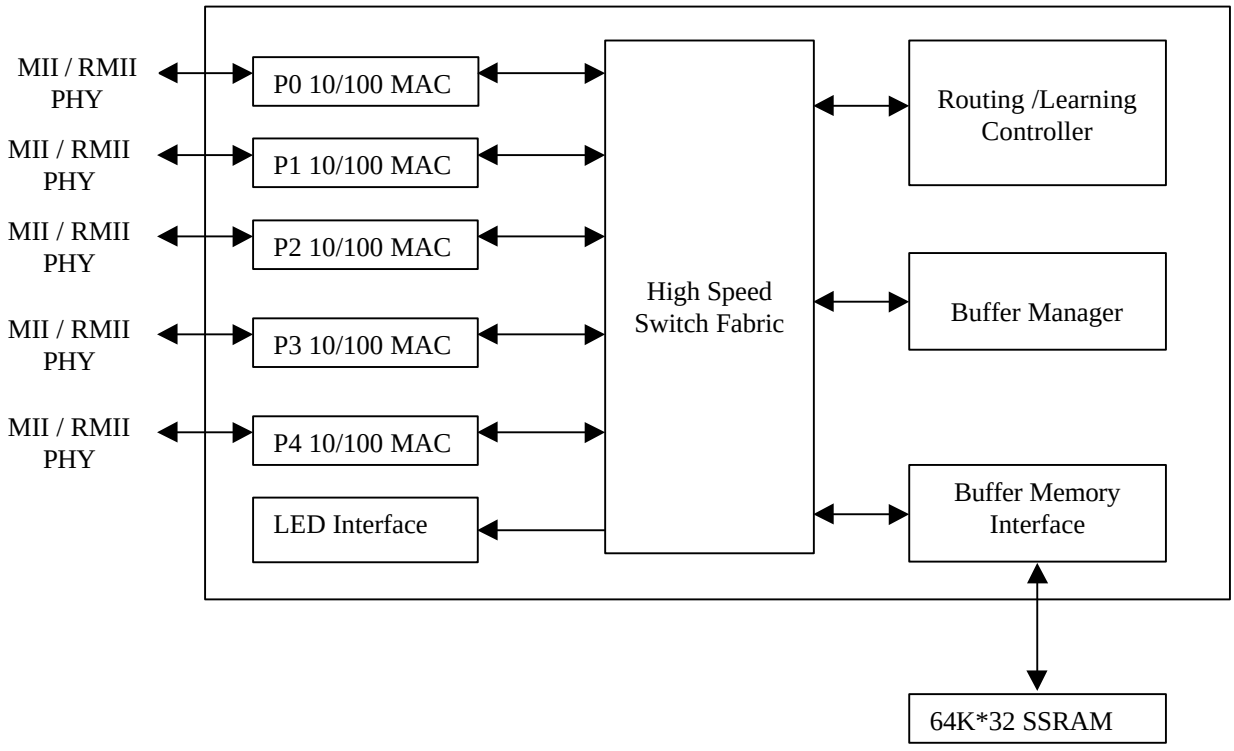



Fig - 1 AX88615 Block Diagram

## 1.3 Pin Connection Diagram

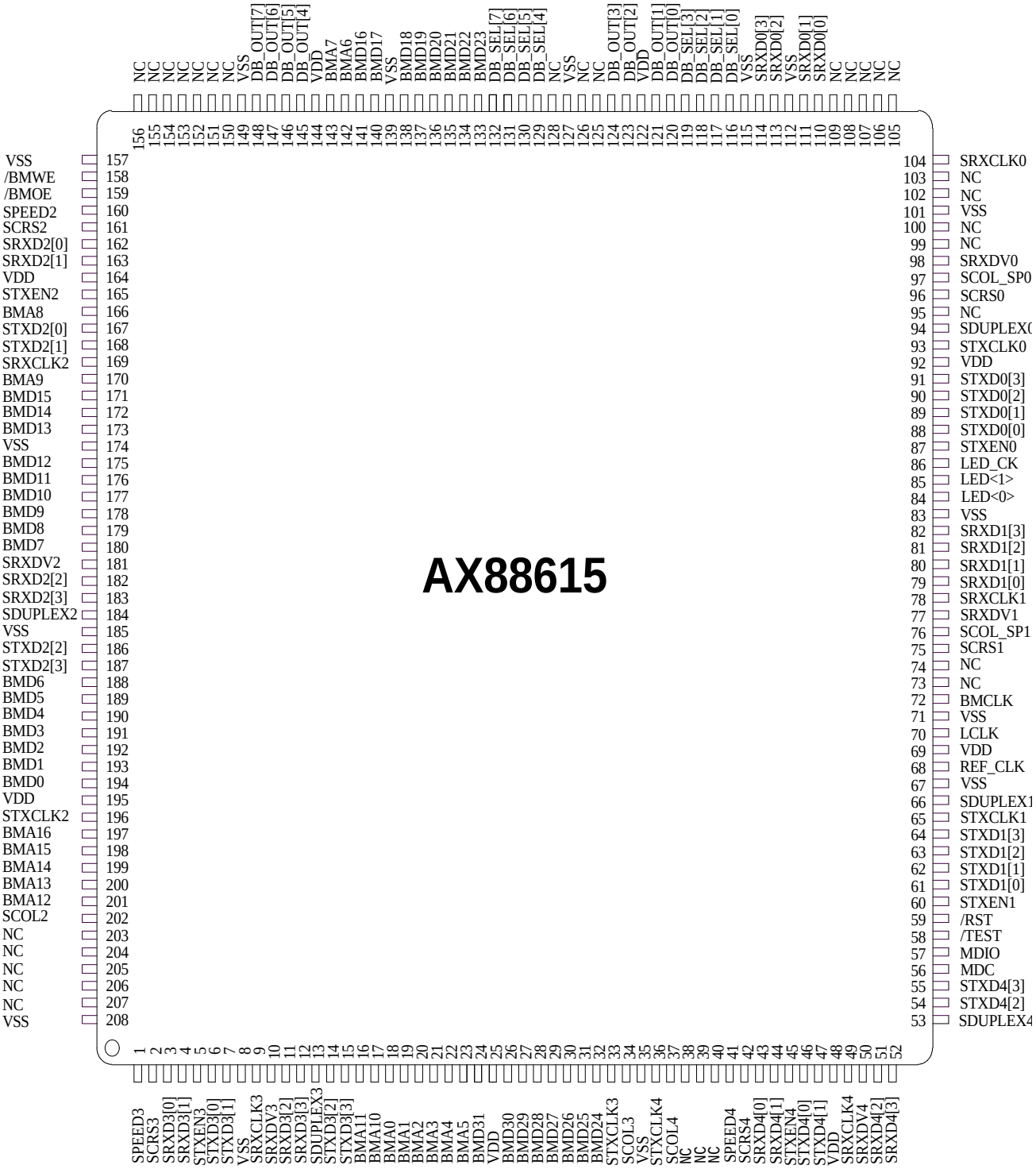



Fig - 2 Pin Connection Diagram

# 2.0 Pin Description

## 2.0 Pin Description

The following terms describe the AX88615 pinout:

All pin names with the "/" suffix are asserted low.

| | | |
|---|---|---|
| I | = | Input |
| O | = | Output |
| I/O | = | Input /Output |

## 2.1 MII/RMII interface for switch ports

### 2.1.1 Switch Port 0

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| STXEN0 | O | 87 | **Transmit Enable :** Active HIGH. This output indicates that the packet is being transmitted .If MII mode, TXEN0 is synchronous to STXCLK0. If RMII mode, TXEN0 is synchronous to REF_CLK. |
| STXD0[3:0] | O | 91,90,89,88 | **Transmit Data :** STXD0[3:0] is synchronous to the rising edge of STXCLK0 in MII mode. For each STXCLK period in which STXEN is asserted, TXD[3:0] are accepted for transmission by the PHY.<br>If RMII mode, STXD0[1:0] is synchronous to REF_CLK. TXD0[1:0] shall be "00" to indicate idle when TX_EN is disserted. Value that is not "00" is reserved for out-of-band signaling and shall be ignored by PHY. When TX_EN is asserted, TXD[1:0] are accepted for transmission by PHY |
| STXCLK0 | I | 93 | **Transmit Clock :** Provides the timing reference for the STXEN0, STXD0 signals in MII mode. STXCLK0 frequency is one fourth of the data rate (25 MHz for 100Mbps, 2.5 MHz for 10Mbps). |
| SDUPLEX0 | I | 94 | **Duplex Select :** DUPLEX0 is not standard MII/RMII signal. This input is connected to PHY directly to obtain the current data rate of Port0. |
| SCOL_SP0 | I | 97 | **Collision Detect:** Active HIGH. Indicates a collision has been detected on wire in MII mode. This input is not synchronous to any clock and ignored in full-duplex mode<br>If RMII mode, the signal is a speed indicator. Active for 10Mbps speed is selected depending on power on configuration. |
| SCRS0<br><br>or<br>SCRS_DV0 | I | 96 | **Carrier Sense :** Active HIGH. Indicates that either the transmit or receive medium is non-idle in MII mode. SCRS0 is not synchronous to any clock.<br>When RMII mode, the input is CRS_DV (Carrier Sense/Receive Data Valid ) that is asserted asynchronously on detection of carrier by the PHY when receive medium is non-idle. Loss of carrier shall result in the desertion of CRS_DV synchronous to the cycle of REF_CLK, which presents the first DI-bit of a nibble on to RXD0[1:0]. |
| SRXDV0 | I | 98 | **Receive Data Valid :** Active HIGH. Indicates that valid data is present on the SRXD0 lines. Synchronous to SRXCLK0. |
| SRXCLK0 | I | 104 | **Receive Clock :** Provides the timing reference for the SRXDV0, SRXD0 signals in MII mode. STXCLK0 frequency is one fourth of the data rate (25 MHz for 100Mbps, 2.5 MHz for 10Mbps). |
| SRXD0[3:0] | I | 114,113,<br>111,110 | **Receive Data :** Synchronously to the rising edge of RXCLK in MII mode.<br>If RMII mode, SRXD0[1:0] is synchronous to REF_CLK. SRXD0[1:0] shall be "00" to indicate idle when CRS_DV is disserted. Value that is not "00" is reserved for out-of-band signaling shall be ignored by MAC Upon assertion of CRS_DV, PHY shall ensure that RXD[1:0] = "00" until proper receive decoding takes place |

### 2.1.2 Switch Port 1

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| STXEN1 | O | 60 | **Transmit Enable :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXD1[3:0] | O | 64,63,62,61 | **Transmit Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXCLK1 | I | 65 | **Transmit Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SDUPLEX1 | I | 66 | **Duplex Select :** Please references section 2.1.1 SWITCH PORT0 description. |
| SCOL_SP1 | I | 76 | **Collision Detect:** Please references section 2.1.1 SWITCH PORT0 description. |
| SCRS1 or SCRS_DV1 | I | 75 | **Carrier Sense :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXDV1 | I | 77 | **Receive Data Valid :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXCLK1 | I | 78 | **Receive Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXD1[3:0] | I | 82,81,80,79 | **Receive Data :** Please references section 2.1.1 SWITCH PORT0 description. |

### 2.1.3 Switch Port 2

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| STXEN2 | O | 165 | **Transmit Enable :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXD2[3:0] | O | 187,186, 168,167 | **Transmit Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXCLK2 | I | 196 | **Transmit Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SDUPLEX2 | I | 184 | **Duplex Select :** Please references section 2.1.1 SWITCH PORT0 description. |
| SCOL2 | I | 202 | **Collision Detect:** Please references section 2.1.1 SWITCH PORT0 description. |
| SCRS2 or SCRS_DV2 | I | 161 | **Carrier Sense :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXDV2 | I | 181 | **Receive Data Valid :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXCLK2 | I | 169 | **Receive Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXD2[3:0] | I | 183,182, 163,162 | **Receive Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| SPEED2 | I | 160 | **Speed Indicator :** Identify data rate of Port 2 |

### 2.1.4 Switch Port 3

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| STXEN3 | O | 5 | **Transmit Enable :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXD3[3:0] | O | 15,14,7,6 | **Transmit Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXCLK3 | I | 33 | **Transmit Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SDUPLEX3 | I | 13 | **Duplex Select :** Please references section 2.1.1 SWITCH PORT0 description. |
| SCOL3 | I | 34 | **Collision Detect:** Please references section 2.1.1 SWITCH PORT0 description. |
| SCRS3<br>or<br>SCRS_DV3 | I | 2 | **Carrier Sense :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXDV3 | I | 10 | **Receive Data Valid :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXCLK3 | I | 9 | **Receive Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXD3[3:0] | I | 12,11,4,3 | **Receive Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| SPEED3 | I | 1 | **Speed Indicator :** Identify data rate of Port 3 |

### 2.1.5 Switch Port 4

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| STXEN4 | O | 45 | **Transmit Enable :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXD4[3:0] | O | 55,54,47,46 | **Transmit Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| STXCLK4 | I | 36 | **Transmit Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SDUPLEX4 | I | 53 | **Duplex Select :** Please references section 2.1.1 SWITCH PORT0 description. |
| SCOL4 | I | 37 | **Collision Detect:** Please references section 2.1.1 SWITCH PORT0 description. |
| SCRS4<br>or<br>SCRS_DV4 | I | 42 | **Carrier Sense :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXDV4 | I | 50 | **Receive Data Valid :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXCLK4 | I | 49 | **Receive Clock :** Please references section 2.1.1 SWITCH PORT0 description. |
| SRXD4[3:0] | I | 52,51,44,43 | **Receive Data :** Please references section 2.1.1 SWITCH PORT0 description. |
| SPEED4 | I | 41 | **Speed Indicator :** Identify data rate of Port 4 |

## 2.2 LED Display

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| LED[1:0] | O | 85, 84 | **SSRAM Fail / Buffer Memory Utilization LED :**<br>❖ As utilization of buffer memory<br>The buffer utilization of switch uses the following definition:<br>1: Led off<br>0: Led on<br><br>For detail , see the LED timing specification.<br><br>❖ SSRAM Fail<br>LED[0] : This signal also indicates SRAM chip 0 fail ( continue active low ) during the interval of sequence shift data.<br><br>LED[1] : This signal also indicates SRAM chip 1 fail ( continue active low ) during the interval of sequence shift data. |
| LED_CK | O | 86 | **LED Clock :** The signal is a discontinue clock for LED signals serial shift out. The clock period width is 400nS and last 32 cycle with every 52.4ms repeated. |

| Utilization (%) | UTI0 | UTI1 | UTI2 | UTI3 | UTI4 | UTI5 |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 | 1 | 1 |
| 20 | 0 | 0 | 1 | 1 | 1 | 1 |
| 40 | 0 | 0 | 0 | 1 | 1 | 1 |
| 60 | 0 | 0 | 0 | 0 | 1 | 1 |
| 80 | 0 | 0 | 0 | 0 | 0 | 1 |
| 95 | 0 | 0 | 0 | 0 | 0 | 0 |

## 2.3 Buffer memory pins group

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| BMA[16:0] | O | 197–201<br>16,17<br>170,166<br>143,142<br>23-18 | **SSRAM Address Bus** |
| BMD[31:24]<br>BMD[23:16]<br><br>BMD[15:8]<br><br>BMD[7:0] | I/O | 24, 26-32<br>133-138<br>140, 141<br>171-173<br>175-179<br>180,<br>188-194 | **SSRAM Data Bus** |
| /BMWE | O | 158 | **SSRAM Write Strobe** |
| /BMOE | O | 159 | **SSRAM Read Strobe** |
| BMCLK | O | 72 | **SSRAM CLOCK** |

## 2.4 Miscellaneous

| Signal Name | Type | Pin No. | Description |
|---|---|---|---|
| LCLK | I | 70 | **Local Clock :** 66Mhz. Used for system operation synchronous. |
| /RST | I | 59 | **Reset :** Active Low<br>The chip is reset when this signal is asserted Low. |
| REF_CLK | I | 68 | **Reference clock :** The input is a continue clock at 50Mhz for timing reference with RMII interface. |
| /TEST | I/PU | 58 | **Test Pin :** Active LOW<br>The pin is just for test mode setting purpose only. Must be pull high when normal operation. |
| MDIO | I/O | 57 | **Station Management Data In/Out :**<br>To read PHY Auto Negotiation Remote Capability register to get current speed and duplex status. (See appendix also) |
| MDC | O | 56 | **Station Management Data Clock Out :** For MDIO reference clock. |
| DB_SEL[7:0] | I/PU | 132-129, 119-116 | **Debug Mode Selection :**<br>Enable debug selection when /TEST pin = 0 |
| DB_OUT[7:0] | O | 148-145, 124,123, 121,120 | **Debug Mode Monitor Output :** |
| NC | O | 38,39,40, 56,57,73, 74,95,99, 100,102, 105-109, 125,126, 128, 150-156, 203-207 | **NC :** Keep no connection |
| VDD | I | 25, 48, 69, 92, 122, 144, 164, 195, | **POWER :** +3.3V +/-5% |
| VSS | I | 8, 35, 67, 71, 83, 101, 112,115, 127, 139, 149, 157, 174,185, 208 | **POWER:** 0V |

## 2.5 Power on configuration setup signals cross reference table

| Signal Name | Share with | Description |
|---|---|---|
| /Hash_En | BMA[16] | **Hash Algorithm Enable :**<br>0 : Enable look-up table addressing use hashing algorithm.<br>1 : Disable look-up table addressing use linear addressing |
| Aging_S[2:0] | BMA[15:13] | **Aging Timer Selection :**<br>**Aging_S2 Aging_S1 Aging_S0 Aging Time (Min)**<br>1 1 1 no aging (disable)<br>1 1 0 5<br>1 0 1 10<br>1 0 0 20<br>0 1 1 40<br>0 1 0 160<br>0 0 1 640<br>0 0 0 1 |
| RxFC_En | BMA[12] | **PAUSE Identification Enable :**<br>0 : Disable 802.3x receives flow control function in full duplex.<br>1 : Enable 802.3x receives flow control function in full duplex. |
| MII_S1 | BMA[11] | **MII Enable for Port 1, 2, 3, 4 :**<br>0 : Switch port 1, 2, 3, 4 "RMII" mode is selected<br>1 : Switch port 1, 2, 3, 4 "MII" mode is selected |
| MII_S0 | BMA[10] | **MII Enable for Port 0 :**<br>0 : Switch port 0 "RMII" mode is selected<br>1 : Switch port 0 "MII" mode is selected |
| /Part_En | BMA[9] | **TX Partition Enable :**<br>0 : Enable partition function of transition.<br>1 : Disable partition function of transition. |
| RAM_S | BMA[5] | **RAM Size Selection :** External packet buffer RAM size select<br>**RAM_S RAM SIZE**<br>1 64K * 32 SSRAM<br>0 128K * 32 SSRAM |
| NetQlty_S | BMA[4] | **Network Quality Selection:** Auto forwarding mode is based on packet error percentage to select Store-and-Forward or Fragment Free mode.<br>**NetQlty_S Error Packet Ratio**<br>1 20%<br>0 40% |
| FwTyp_S1<br>FwTyp_S0 | BMA[3]<br>BMA[2] | **Forward Type Selection :**<br>**FwTyp _S1 FwTyp _S0 Forward Mode**<br>1 1 Store & Forward<br>1 0 Store & Forward<br>0 1 Fragment Free<br>0 0 Auto |
| HiBndy_S1<br>HiBndy_S0 | BMA[1]<br>BMA[0] | **Threshold Selection for Flow Control :**<br>Flow control will be active when buffer memory is below the threshold:<br>**HiBndy_S1 HiBndy_S0 Buffers Left**<br>1 1 64 packets<br>1 0 32 packets<br>0 1 16 packets<br>0 0 96 packets |
| / FlowCtl _En4 | STXEN0 | **P4 Flow Control Enable :**<br>Enable flow control function of switch port 4, 802.3x for full duplex, back pressure for half duplex.<br>0 : Enable flow control function.<br>1 : Disable flow control function. |
| / FlowCtl _En3 | STXD0[3] | **P3 Flow Control Enable :** Enable flow control functions of switch port 3, |

| | | |
|---|---|---|
| | | 802.3x for full duplex, back pressure for half duplex.<br>0 : Enable flow control function.<br>1 : Disable flow control function. |
| / FlowCtl _En2 | STXD0[2] | **P2 Flow Control Enable :** Enable flow control functions of switch port 2, 802.3x for full duplex, back pressure for half duplex.<br>0 : Enable flow control function.<br>1 : Disable flow control function. |
| / FlowCtl _En1 | STXD0[1] | **P1 Flow Control Enable :** Enable flow control functions of switch port 1, 802.3x for full duplex, back pressure for half duplex.<br>0 : Enable flow control function.<br>1 : Disable flow control function. |
| /FlowCtl_En0 | STXD0[0] | **P0 Flow Control Enable :** Enable flow control functions of switch port 0, 802.3x for full duplex, back pressure for half duplex.<br>0 : Enable flow control function.<br>1 : Disable flow control function. |
| Speed_S1 | STXD1[2] | **Speed Setting for Port 1, 2, 3, 4 :** In RMII mode, speed "SCOL_SP1" pin function selection<br>0 : Port 1, 2, 3, 4 RMII mode, SCOL_SP1 pin is Low for 10M,high for 100M<br>1 : Port 1, 2, 3, 4 RMII mode, SCOL_SP1 pin is Low for 100M,high for 10M |
| Speed_S0 | STXD1[1] | **Speed Setting for Port 0 :** In RMII mode, speed "SCOL_SP0" pin function selection<br>0 : Port 0 RMII mode, SCOL_SP0 pin is Low for 10M,high for 100M<br>1 : Port 0 RMII mode, SCOL_SP0 pin is Low for 100M,high for 10M |
| FdpxHi_S1 | STXD1[0] | **Duplex Setting for Port 1, 2, 3, 4 :** Port 1, 2, 3, 4 "SDUPLEX1" pin function select<br>0 : SDUPLEX1 pin is Low for half duplex,high for full duplex<br>1 : SDUPLEX1 pin is Low for full duplex,high for half duplex |
| FdpxHi_S0 | STXEN1 | **Duplex Setting for Port 0 :** Port 0 "SDUPLEX0" pin function selection<br>0 : SDUPLEX0 pin is Low for half duplex,high for full duplex<br>1 : SDUPLEX0 pin is Low for full duplex,high for half duplex |
| /RdPhy_En | STXD4[0] | **MDIO read PHY Register 05h Information**<br>0 : Enable<br>1 : Disable |
| PktLenOpt | STXD3[0] | **Maximun Packet Length Selection**<br>0 : 1522 Byte<br>1 : 1518 Byte |

**All of the above signals are pull-up for default values.**

# 3.0 Functional Description

## 3.1 Basic Operation

In general, the basic operation of the switch is very simple. The switch receives incoming packets from one of its ports, searches in the Look-Up Table for the Destination MAC Address and then forwards the packet to the destination ports, if appropriate. If the destination MAC address is not found in the Look-Up Table, the switch treats the incoming packet as a broadcast packet and forwards it to all ports except itself. Basically the switch automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets. The device is updated the table with the Source MAC Address if the Source MAC Address does not exist the table.

## 3.2 Packet Filtering and Forwarding Process

During the receiving process, the switch will monitor the length of the received packet. Legal Ethernet packets should have a length of no less 64 bytes and nor more than 1528 bytes. The switch discards any packet with illegal length.

After a packet is received, its Source MAC Address and Destination MAC Address are received. The Source MAC Address is used to update the Look-Up Table and the Destination MAC Address is used to determine the destination port of the packet. Once a MAC Address has been learned, and the packet is buffered, it must be forwarded, That is, the packet forwarding mechanism for the switch is handled automatically based on the destination MAC Address.

Under the following conditions, received packets are filtered:

- The switch will check all received packets for errors, e.g., FCS error, runt packet, long packet, etc.
- Any packet handing to its own source port will be filtered. That is, its destination port is its source port.
- The incoming packet will be discarded if the switch's buffer memory is full.

The switch supports three forwarding modes: Store-and-Forward, Fragment-Free and Auto.

- Store-and-Forward Mode: An entry packet is received, checked and stored in the buffer memory before it is forwarded. That is, each forwarded packet is correct.
- Fragment-Free Mode: It is a simple improvement on Cut-Through method. The switch will forward a packet whose packet length is more than 64 bytes. All runt packets will be filtered in Fragment-Free mode.
- Auto Mode: In Auto mode, the switch select dynamically its optimized forwarding mode based on the current network quality of each port.

## 3.3 MAC Address Learning and Aging Process

The switch can learn up to 8K unique MAC addresses with a hashing algorithm. Addresses are stored in the Look-Up Table located in external SSRAM, then each packet updates the table.

The table lookup engine provides the switching information required routing the data packets. The address table is set up through auto address learning dynamically. After the switch receives a packet, the Source MAC Address and Destination MAC Address are received. The Source Address retrieved from the received packet is automatically stored in a SA buffer. The switch will check for error and perform a SA search. The switch will update the Look-Up Table with the Source MAC Address if there is no error.

The Look-Up Table is cleared on power-on, or hardware reset. When the aging option is enabled, the dynamically Learned SA will be cleared if it is not refreshed in less than configured time (2 or 5 min).

## 3.4 Flow Control Process

The switch can operate at two different modes: half-duplex and full-duplex. Each port can be configured to have flow control enabled or not. The switch supports 802.3X for full-duplex operation and uses back pressure for half-duplex.

In full-duplex mode, the switch will receive and transmit the packet in accordance to 802.3X. The transmission channel and the receiving channel operate independently. If the occupancy of the buffer memory is above the FlowControlActive

threshold, the MAC of port will send out a PAUSE frame with maximum delay. The switch will send out a PAUSE frame with zero delay after below FlowControlActive threshold.

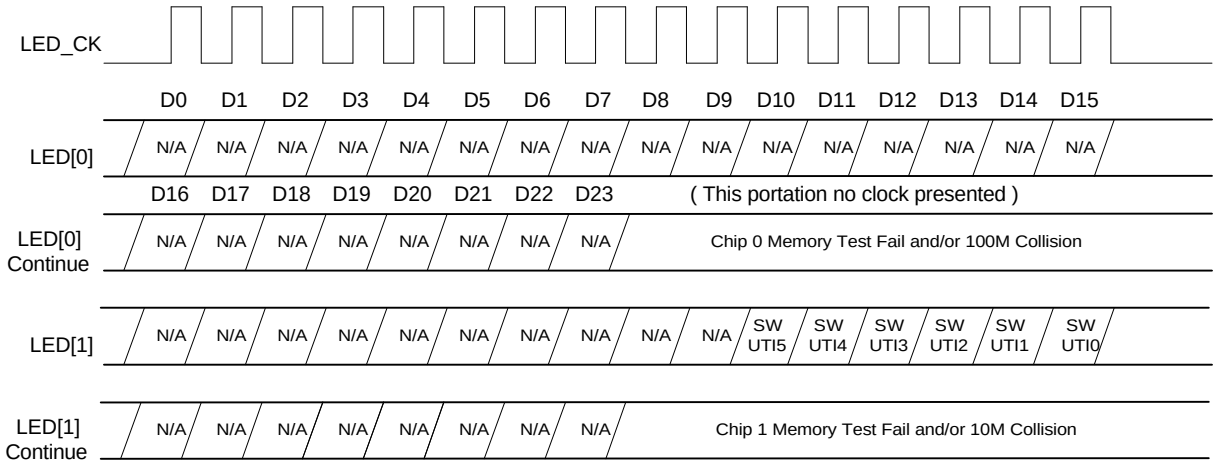
For the receiving channel, the switch will not transmit the next packet whenever received a PAUSE frame with non-zero delay. The switch will resume packet transmission either after the pause timer expired or a PAUSE frames with zero delay received.

In half-duplex mode, the switch will receive and transmit the packet in accordance to 802.3 CSMA/CD. If the occupancy of the buffer memory is above the FlowControlActive threshold, the MAC of port will send out JAM pattern .

## 3.5 LED Display Interface

AX88615 provides LED status indication for memory test and packet buffer utilization (%). All LED[2:0] perform active low.

LED[2:0] Status Driver Wave-form as follows :




It must use external shift register to decode data on LED[1]. The application shows as follows:

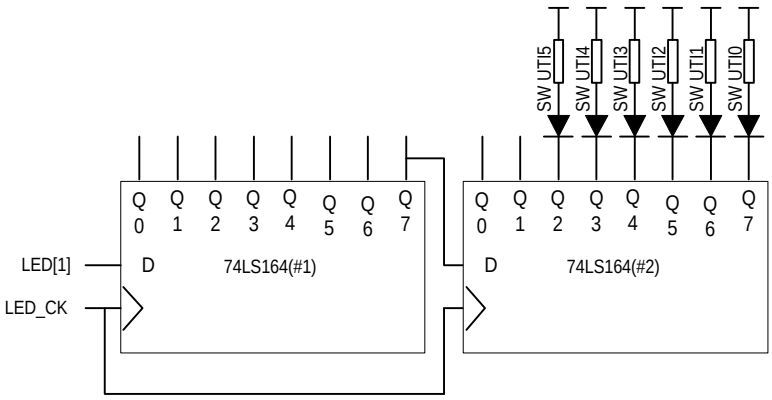



Fig - 3 Application for LED display

# 4.0 INTERNAL REGISTERS

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# 5.0 ELECTRICAL SPECIFICATION AND TIMING

## 5.1 Absolute Maximum Ratings

| Description | SYM | Min | Max | Units |
|---|---|---|---|---|
| Operating Temperature | Ta | 0 | +70 | °C |
| Storage Temperature | Ts | -55 | +150 | °C |
| Supply Voltage | Vcc | -0.3 | +4.0 | V |
| Input Voltage | Vin | -0.3 | Vdd+0.5 | V |
| Output Voltage | Vout | -0.3 | Vdd+0.5 | V |
| Lead Temperature (soldering 10 seconds maximum) | Tl | -55 | +220 | °C |

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

## 5.2 General Operation Conditions

| Description | SYM | Min | Max | Units |
|---|---|---|---|---|
| Operating Temperature | Ta | 0 | +70 | °C |
| Supply Voltage | Vdd | +3.0 | +3.6 | V |

## 5.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

| Description | SYM | Min | Max | Units |
|---|---|---|---|---|
| Low Input Voltage | Vil | Vss-0.3 | 0.8 | V |
| High Input Voltage | Vih | 2 | Vdd+0.5 | V |
| Low Output Voltage | Vol | | 0.4 | V |
| High Output Voltage | Voh | 2.4 | | V |
| Input Leakage Current 1 (Note 1) | Iil1 | | 10 | uA |
| Input Leakage Current 2 (Note 2) | Iil1 | | 500 | uA |
| Output Leakage Current | Iol | | 10 | uA |

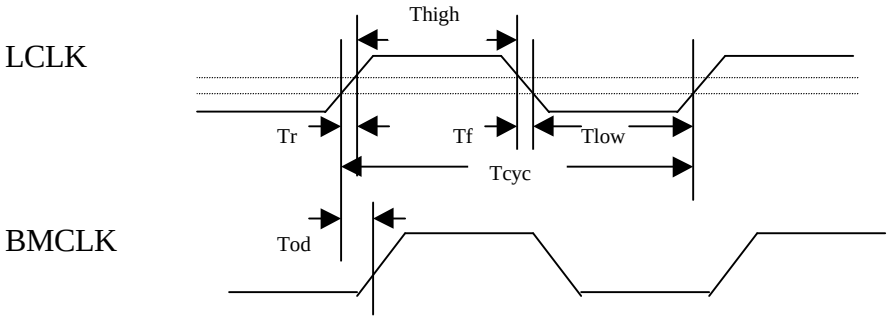
| Description | SYM | Min | Tpy | Max | Units |
|---|---|---|---|---|---|
| Power Consumption | Pc | | TBD | | mA |

Note :

1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

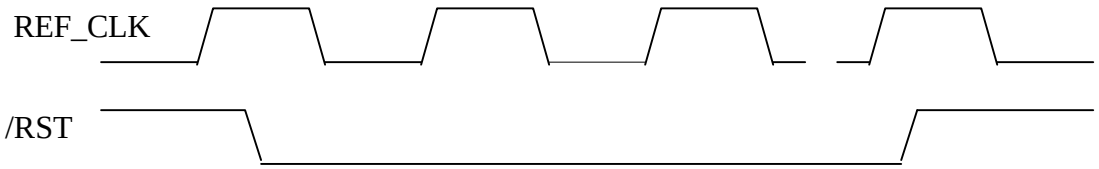
## 5.4 AC specifications

### 5.4.1 LCLK



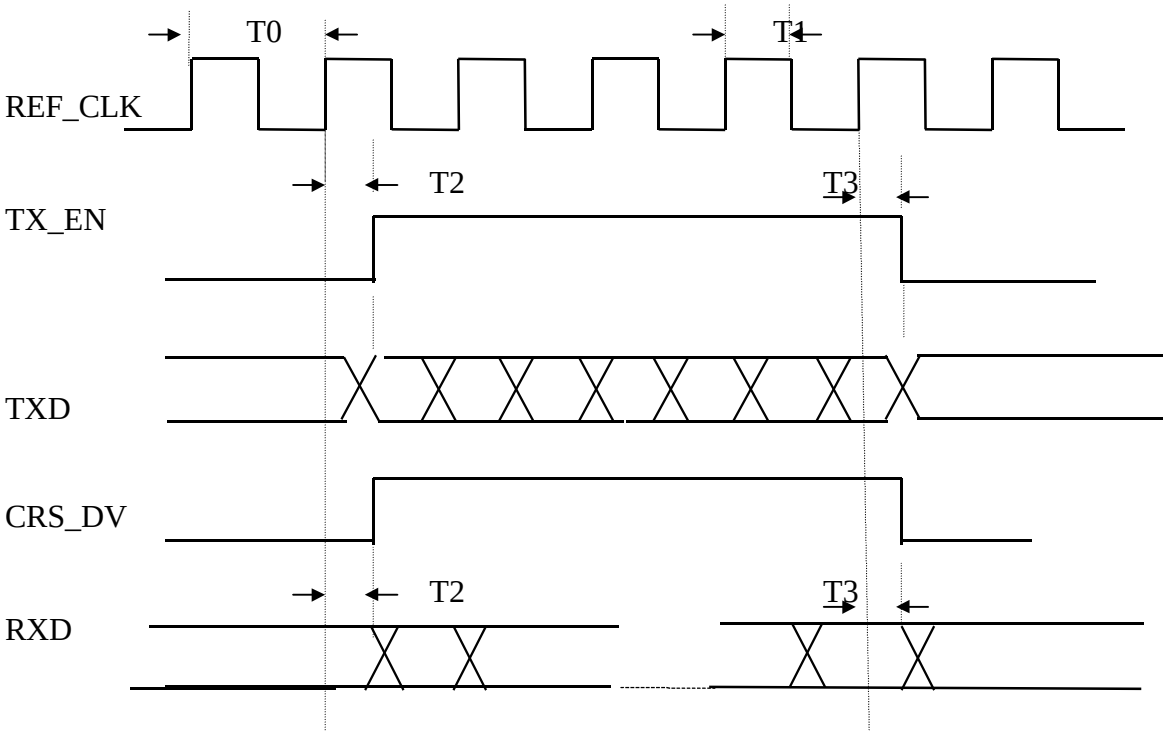

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tcyc | CYCLE TIME | | 16.6 | | ns |
| Thigh | CLK HIGH TIME | 6.64 | 8.3 | 9.96 | ns |
| Tlow | CLK LOW TIME | 6.64 | 8.3 | 9.96 | ns |
| Tr/Tf | CLK SLEW RATE | 1 | - | 4 | ns |
| Tod | LCLK TO BMCLK OUT DELAY | | 2 | | ns |

### 5.4.2 Reset Timing



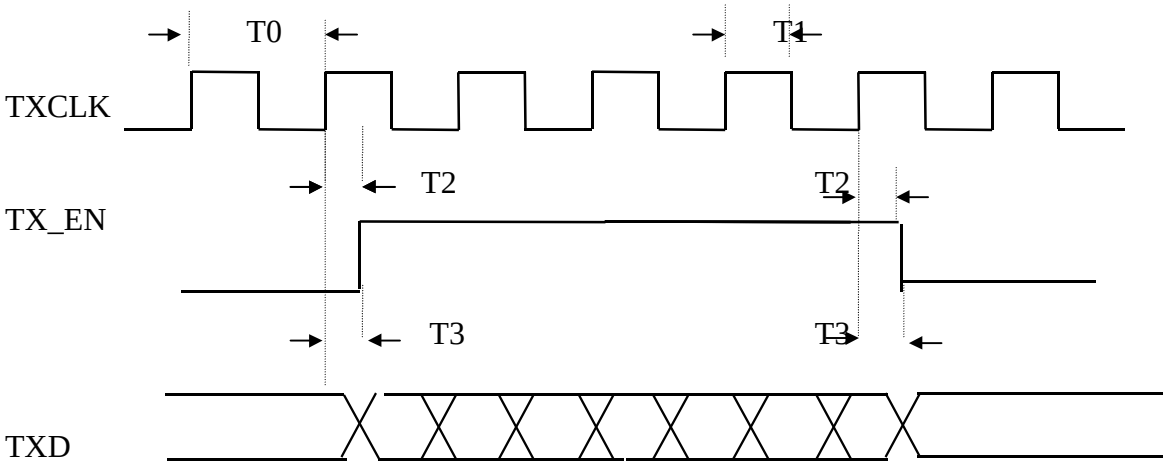

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Trst | Reset pulse width | 10 | - | - | REF_Clk |

### 5.4.3 RMII Interface Timing Tx & Rx

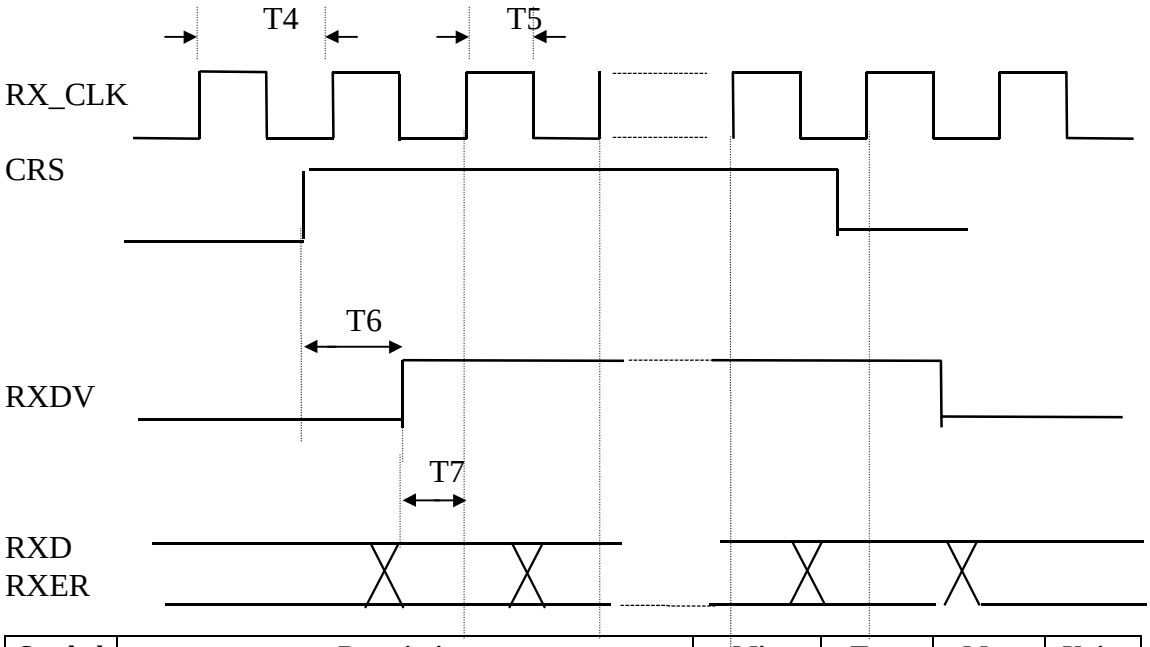



| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| T0 | REF_CLK Clock Cycle Time | 19.998 | 20 | 20.002 | ns |
| T1 | REF_CLK Clock High Time | 7 | 10 | 13 | ns |
| T2 | CRS_DV, RXD, TXEN and TXD data setup to REF_CLK rising edge | 4 | | | ns |
| T3 | CRS_DV, RXD, TXEN and TXD data hold from REF_CLK rising edge | 2 | | | ns |

### 5.4.4 MII Interface Timing Tx & Rx

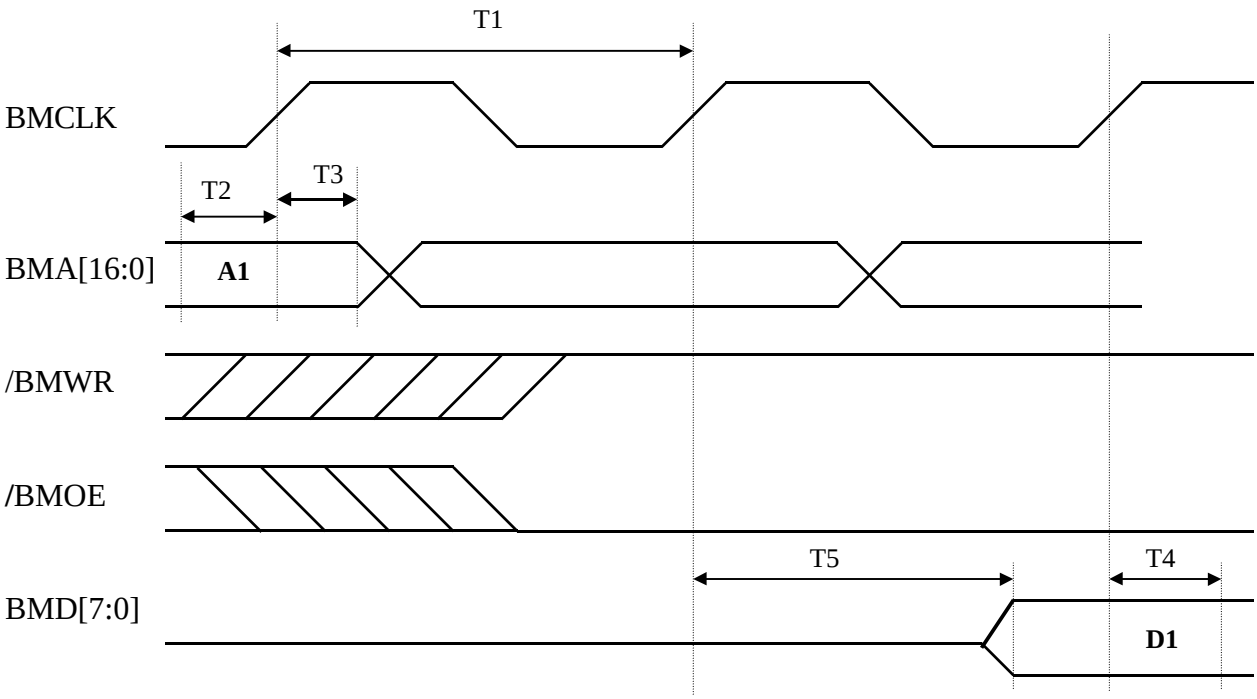



| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| T0 | TXCLK Cycle Time | 39.996 | 40 | 40.004 | ns |
| T1 | TXCLK High Time | 14 | 20 | 26 | ns |
| T2 | TX_EN Delay from TXCLK High | 7.440 | | 21.760 | ns |
| T3 | TXD Delay from TXCLK High | 3.410 | | 13.320 | ns |



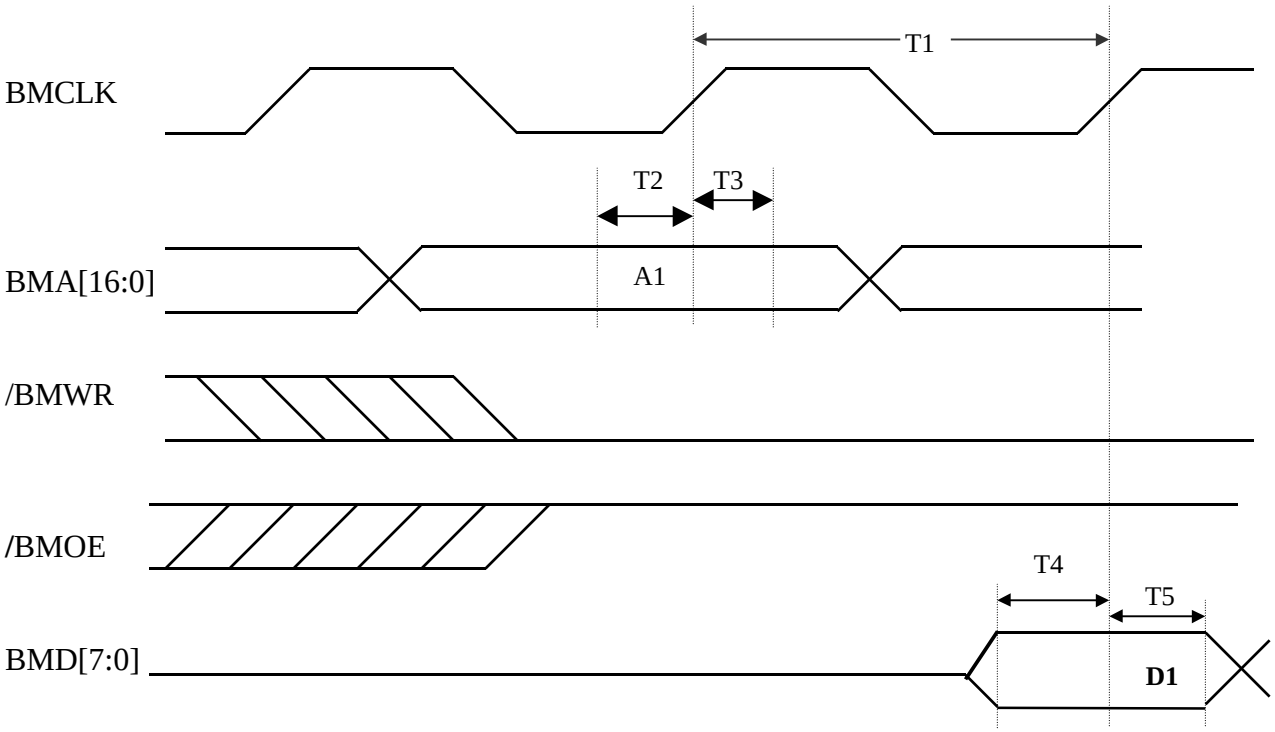

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| T4 | RX_CLK Clock Cycle Time | 39.996 | 40 | 40.004 | ns |
| T5 | RX_CLK Clock High Time | 14 | 20 | 26 | ns |
| T6 | CRS to RXDV Delay Requirement | 40 | | 160 | ns |
| T7 | RXD or RXDV setup to RX_CLK rise time | 10 | | - | ns |

### 5.4.5 SSRAM Read Cycle Timing



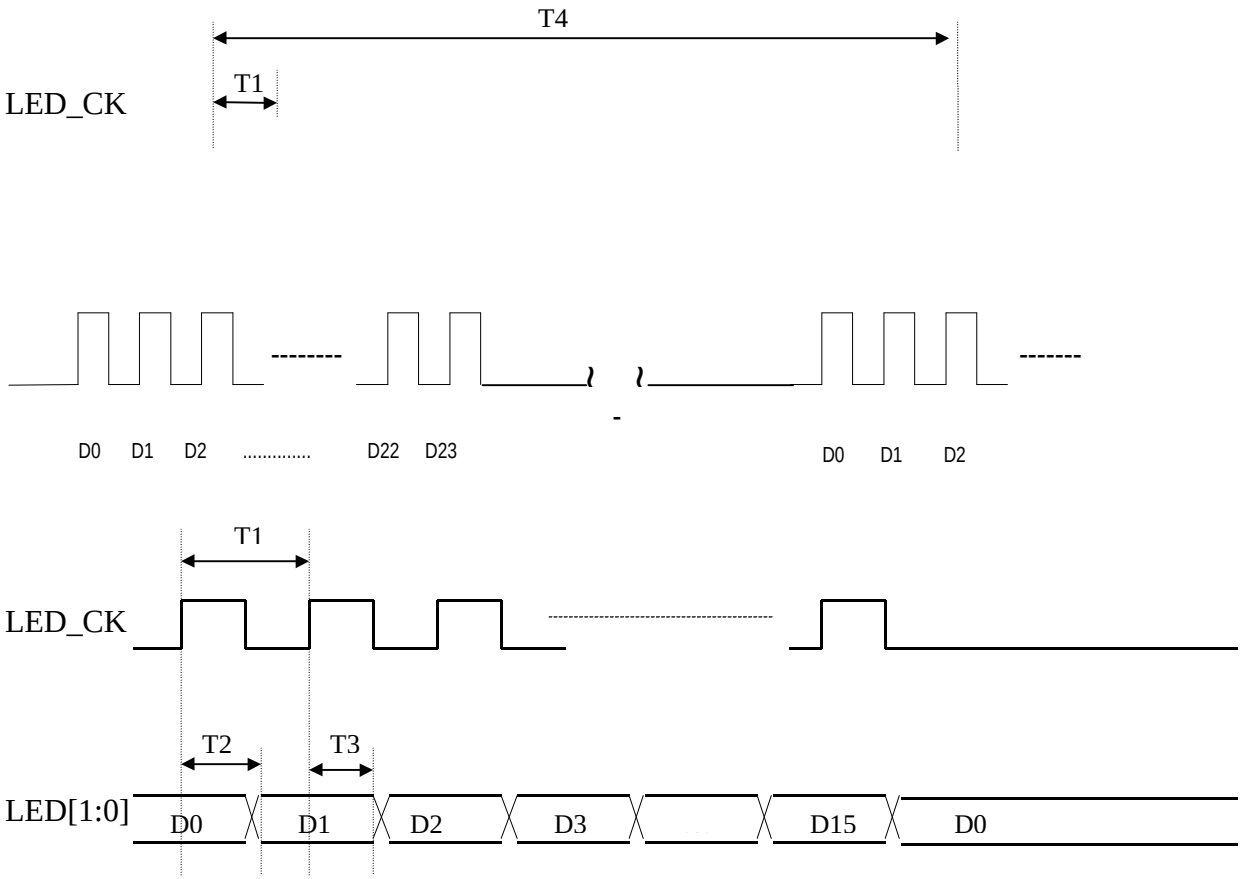

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| T1 | Clock Cycle Time | 15 | - | ns |
| T2 | Address Bus Setup Time | 2.5 | - | ns |
| T3 | Address Bus Hold Time | 0.5 | - | ns |
| T4 | Clock to Output Invalid | 2 | - | ns |
| T5 | Clock to Output Valid | - | 6 | ns |

### 5.4.6 SSRAM Write CycleTiming



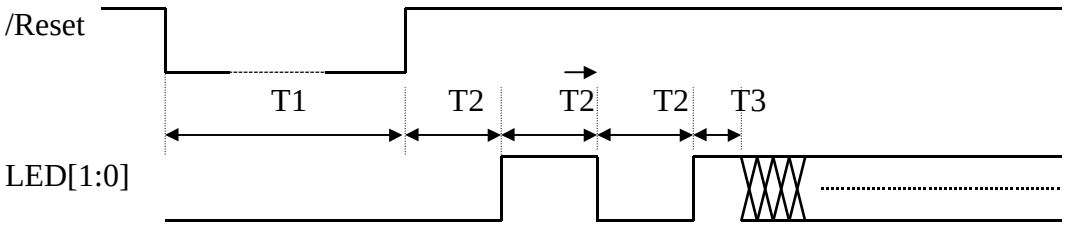

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| T1 | Clock Cycle Time | 15 | - | ns |
| T2 | Address Bus Setup Time | 2.5 | - | ns |
| T3 | Address Bus Hold Time | 0.5 | - | ns |
| T4 | Write Data Setup Time | 2.5 | - | ns |
| T7 | Write Data Hold Time | 0.5 | - | ns |

### 5.4.7 LED DISPLAY



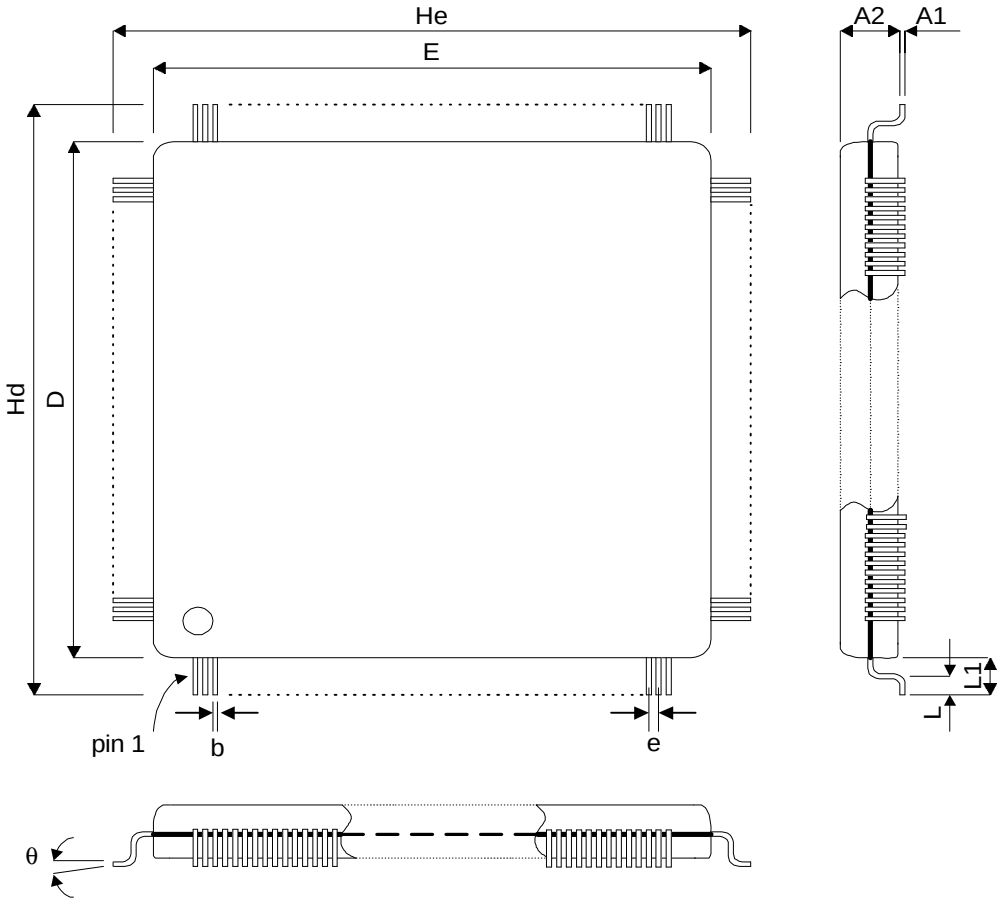

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| T1 | LED_CK Clock Cycle Time | | 400 | | ns |
| T2 | Clock to Output Valid | | | 206.5 | ns |
| T3 | Clock to Output Invalid | 200 | | | ns |
| T4 | continuous 32 LED_CK Cycle Time | | 52.4 | | ms |

### 5.4.8 LED Display After Reset




| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| T1 | Repeater reset time | 1000 | | | ns |
| T2 | LED Blink Time After Reset | | 838.4 | | ms |
| T3 | LED Dark Time Before Normal Display | | 419.2 | | ms |

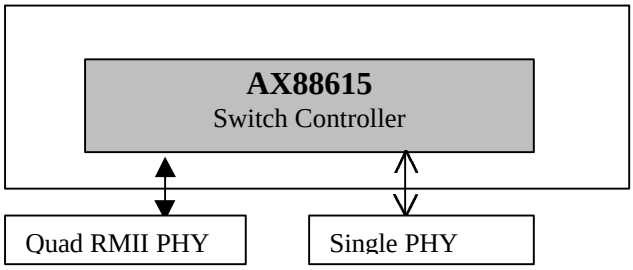
# 6.0 PACKAGE INFORMATION



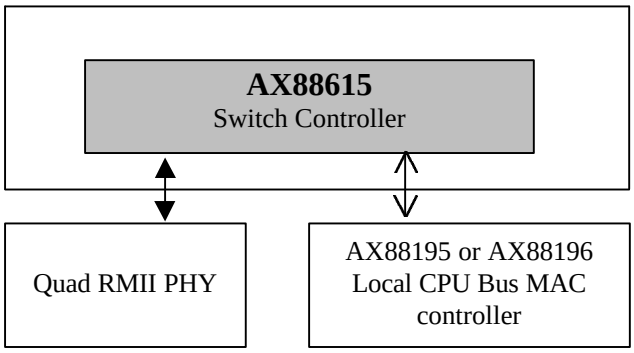

| SYMBOL | MILIMETER | | |
|---|---|---|---|
| | MIN. | NOM | MAX |
| A1 | 0.05 | 0.25 | 0.5 |
| A2 | 3.17 | 3.32 | 3.47 |
| b | 0.10 | 0.20 | 0.30 |
| D | 27.90 | 28.00 | 28.10 |
| E | 27.90 | 28.00 | 28.10 |
| e | | 0.50 | |
| Hd | 30.35 | 30.60 | 30.85 |
| He | 30.35 | 30.60 | 30.85 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.30 | |
| θ | 0 | | 10 |

# Appendix A: System Applications

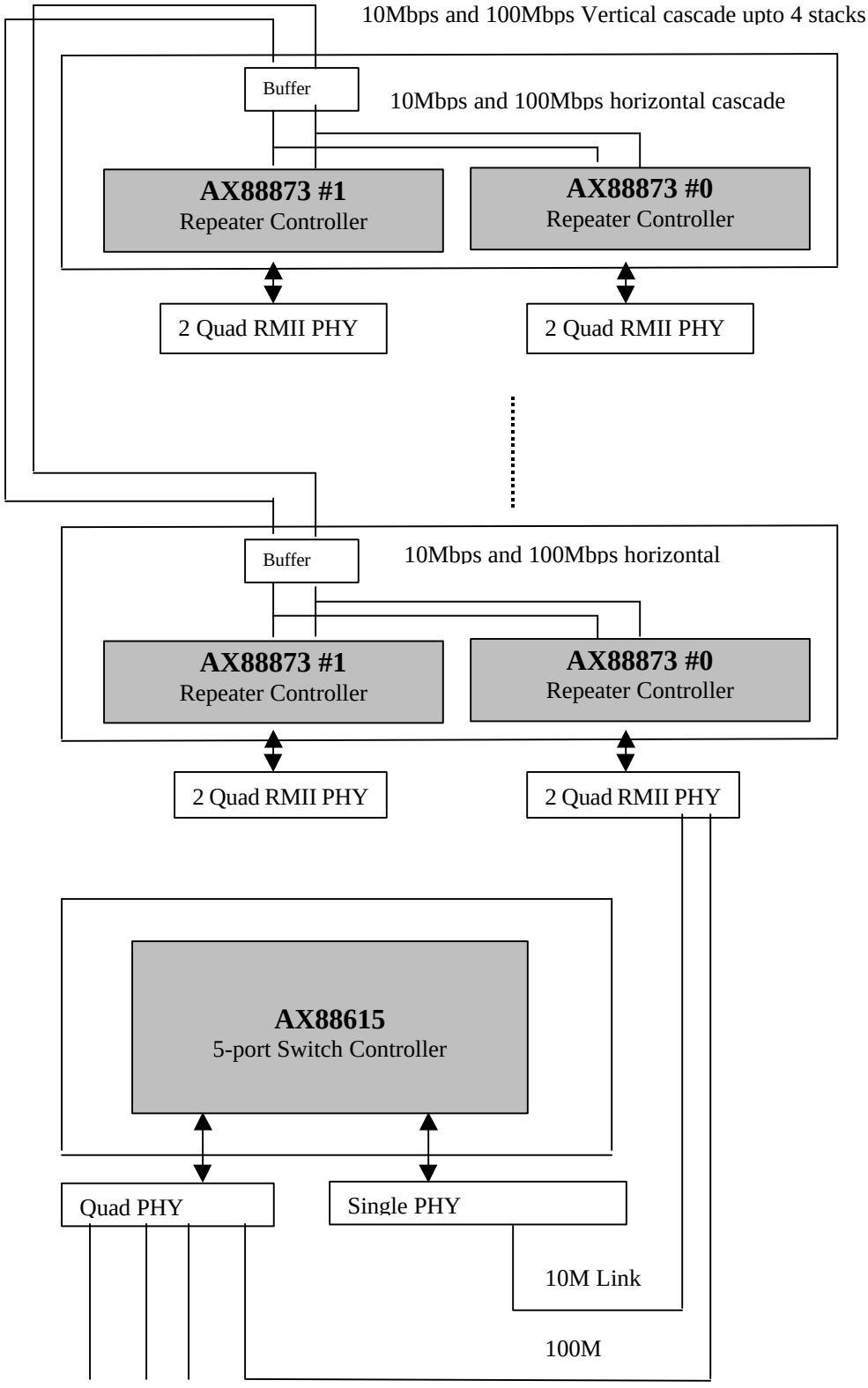
### A.1 AX88615 as 5-port standalone SOHO switch




### A.2 AX88615 for IP router application



### A.3 AX88615 as backend of dual speed repeaters



# Appendix B: Design Note

### B.1 Using Station Management (STA) Connection

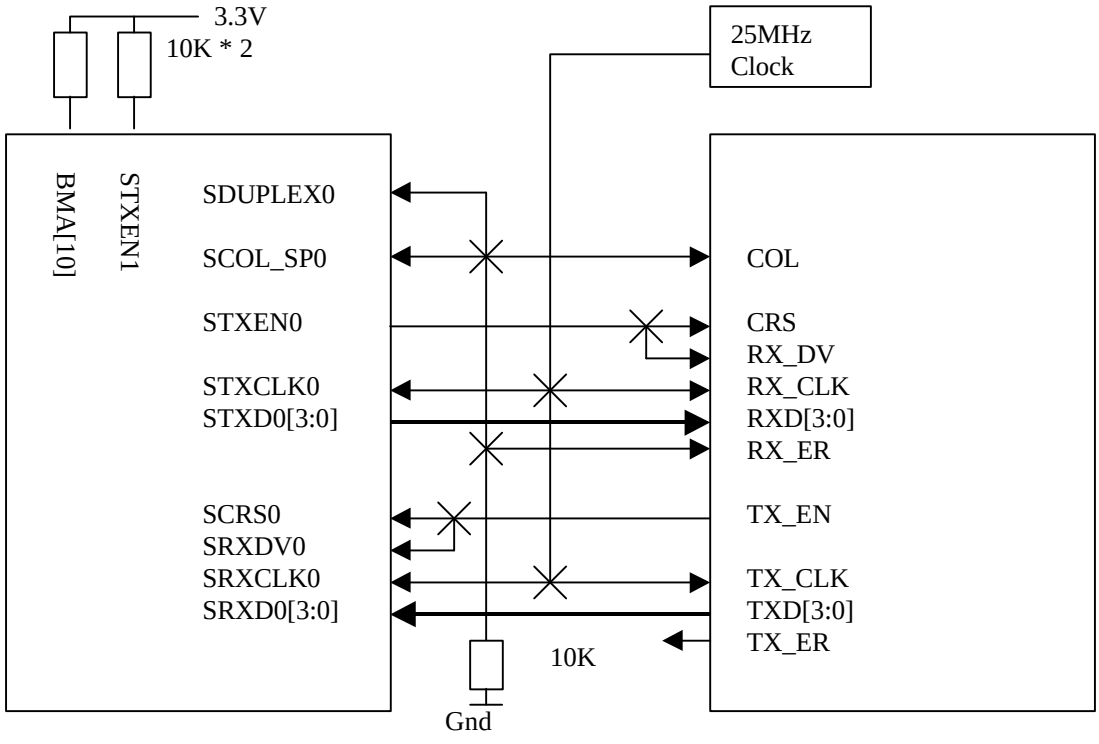
There are two methods to get per port speed and duplex information in AX88615 . One way is by hardware pins such as SPEED0, SDUPLEX0, SPEED1, SDUPLEX1. Ax88615 also provides 2 pins (MDC and MDIO, STA – Station Management connection) to read PHY Auto Negotiation Remote Capability register to get current speed and duplex status. When use STA function, the connected PHY address settings must be fixed as follows:

| Port 0 | Port 1 | Port 2 | Port 3 | Port 4 |
|---|---|---|---|---|
| 0fh | 10h | 11h | 12h | 13h |

The corresponding option setting
/RdPhy_En = 0

### B.2 Using MII I/F connects to MAC

Using MII interface to connect to MAC type device application for AX88615 is illustrated bellow.




Note : 1. The MAC needs to run at fullduplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embbeded MAC can also refer to this example