AX88760
USB 2.0 MTT HUB and USB2.0 to Ethernet Combo Controller

Features

Document No: AX88760/V1.01/07/07/10

- **USB 2.0 MTT Hub**
  - Fully compliant with Universal Serial Bus Specification Revision 2.0
  - Supports USB HS (480Mbps), FS (12Mbps) and LS (1.5Mbps) modes
  - Three downstream ports and one upstream port with integrated USB 2.0 transceivers
  - Multiple Transaction Translator (MTT) provides respective TT control logics for each downstream port
  - Supports one suspend LED indicator and three downstream port status LED indicator
  - On-chip 8-bit micro-processor (6 MIPS @12MHz) with 64-byte RAM and 2K internal ROM
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Supports both individual and gang modes of power management and over-current detection for downstream ports
  - Supports compound-device (non-removable in downstream ports) by I/O pin configuration
  - Improves output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- **10/100M Fast Ethernet Controller**
  - Integrates 10/100Mbps Fast Ethernet MAC/PHY
  - IEEE 802.3 10Base-T/100Base-TX compatible
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Embedded 16KB SRAM for RX packet buffering and 8KB SRAM for TX packet buffering
  - Supports both Full-duplex with flow control and Half-duplex with backpressure operation
  - Supports 2 VLAN ID filtering, received VLAN Tag (4 bytes) can be stripped off or preserved
  - MAC/PHY loop-back diagnostic capability
  - Support Wake-on-LAN Function
    - Supports Suspend mode and Remote Wakeup via Link-up, Magic packet, MS wakeup frame and external pin
    - Optional PHY power down during Suspend mode
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (US Patent Approval)
  - Supports USB to Ethernet bridging or vice versa in hardware
  - Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors for USB to LAN function)
  - Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- Integrates on-chip voltage regulator and only requires a single 3.3V power supply
- 12MHz and 25MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Package type with 100-pin LQFP RoHS compliant package
- Operating temperature range: 0˚C to 70˚C

Product Description

The AX88760 is a high performance and highly integrated USB/Ethernet and USB/USB connectivity solution which contains an USB 2.0 hub, three downstream USB 2.0 transceivers, an upstream USB 2.0 transceiver, a 10/100M Ethernet PHY, a 10/100M Ethernet MAC, a EEPROM controller, and a 24KB SRAM. The AX88760 is targeted for many applications such as desktops, notebook PC's, Ultra-Mobile PC's, docking stations, game consoles, multifunction printers, digital-home appliances, and any embedded system using a standard USB port.

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The AX88760's integrated USB hub is fully compliant with USB 2.0 Specification and supports Low-Speed, Full-Speed, and High-Speed downstream devices on all of the enabled downstream ports. The AX88760 implements multiple TT architecture that provides dedicated TT to each downstream (DS) port, which guarantee maximum bandwidth for each connected device when operating multiple mixed-speed peripherals device. The AX88760 provides full hub features such as (1) One suspend LED indicator and three downstream port status LED indicators, (2) Individual/Gang mode power management scheme and over-current detection for downstream ports, and (3) Non-removable declaration configured by I/O pin during power-on reset…etc

The AX88760 integrates on-chip Fast Ethernet MAC and PHY, which is IEEE802.3 10Base-T and IEEE802.3u 100Base-TX compatible, and 24KB embedded SRAM for packet buffering to accommodate high bandwidth applications. The AX88760 has a wide array of features including support for HP Auto-MDIX, Wake-on-LAN power management, and IEEE 802.3x and backpressure flow control.

Application Diagram

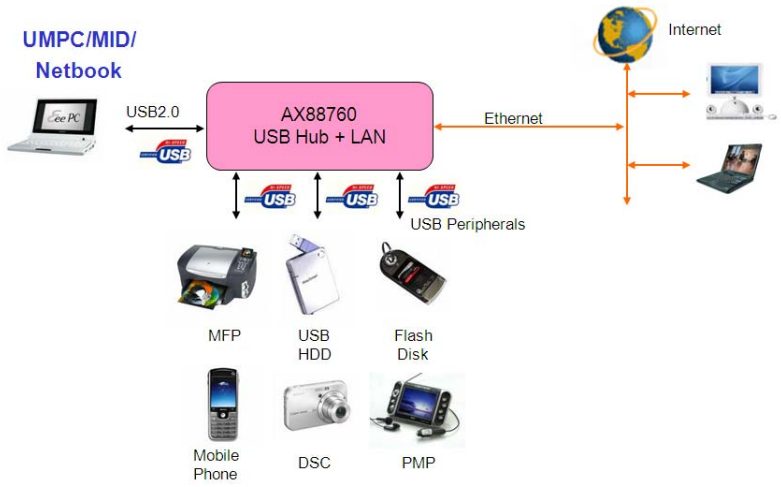


Figure 1 : AX88760 Application Block Diagram

Target Applications

Figure 2 : Target Applications

Table of Contents

List of Figures

List of Tables

1.0 Introduction

1.1 Block Diagram

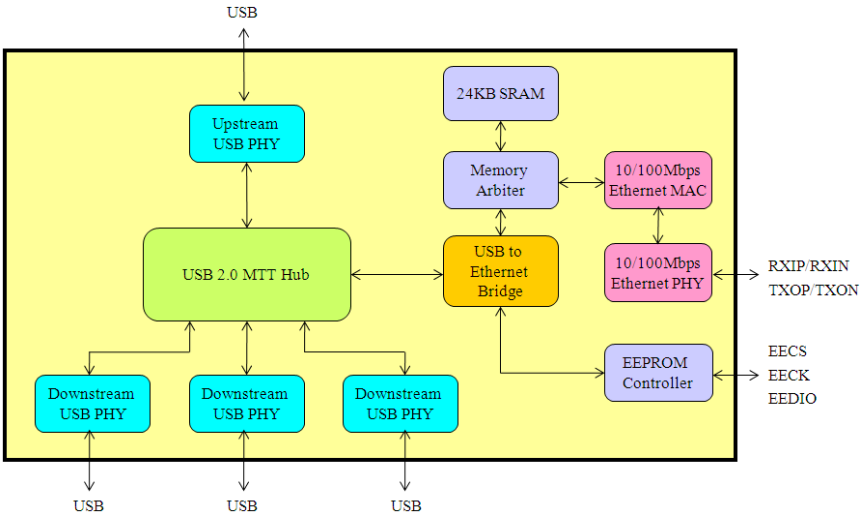


Figure 3 : AX88760 Block Diagram

1.2 Pinout Diagram

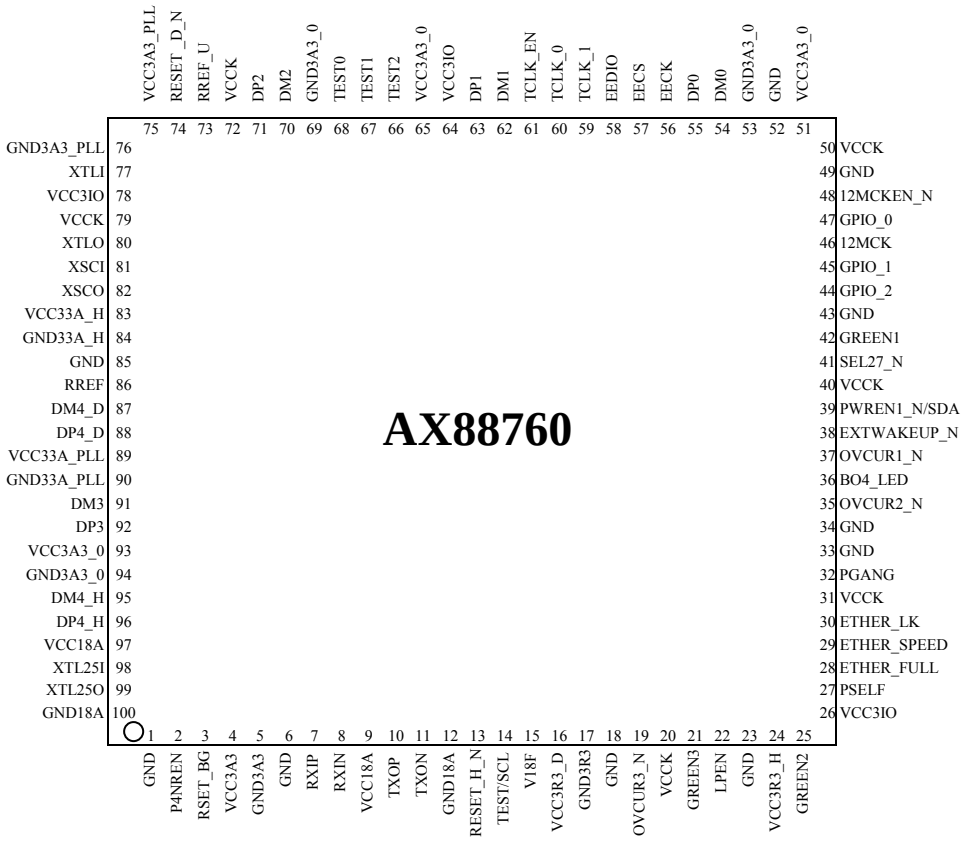


Figure 4 : AX88760 Pinout Diagram

2.0 Signal Description

The following abbreviations apply to the following pin description table.

I18	**Input, 1.8V**	**AO**	**Analog Output**
I3	**Input, 3.3V**	**AB**	**Analog Bi-directional I/O**
I5	**Input, 3.3V with 5V tolerant**	**PU**	**Internal Pull Up (75K)**
O3	**Output, 3.3V**	**PD**	**Internal Pull Down (75K)**
O5	**Output, 3.3V with 5V tolerant**	**P**	**Power Pin**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**S**	**Schmitt Trigger**
		AI	**Analog Input**
B	**Bi-directional I/O, 3.3V**	**T**	**Tri-stateable**

Note: Every output or bi-directional I/O pin is 8mA driving strength.

2.1 AX88760 Pinout Description

Pin Name	Type	Pin No	Pin Description
USB			
DM0	AB	54	USB signals for USPORT (Upstream Port)
DP0	AB	55	
DM1	AB	62	USB signals for DSPORT1 (Downstream Port 1)
DP1	AB	63	
DM2	AB	70	USB signals for DSPORT2 (Downstream Port 2)
DP2	AB	71	
DM3	AB	91	USB signals for DSPORT3 (Downstream Port 3)
DP3	AB	92	
DP4_H, DM4_H	AB	96, 95	USB 2.0 positive and negative differential pins.
DP4_D, DM4_D	AB	88, 87	USB 2.0 positive and negative differential pins. Please connect to pin 96, 95 by parallely.
RREF_U	AI	73	For USB PHY's internal biasing. Please connect to analog GND through a resistor (680ohm±1%).
RREF	AI	86	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
OVCUR1_N, OVCUR2_N, OVCUR3_N,	I5/PU	37 35 19	Active low. Open-Drian Input. Over current indicator for DSPORT1~3 OVCUR1_N is the only over current flag for Gang mode.
PSELF	I5	27	0: HUB controller is bus-power mode 1: HUB controller is self-power mode
PGANG/SUSPEND	B	32	This pin is default put in input mode after power-on reset. Individual/Gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When HUB is suspended, this pin will output low. Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend
P4NREN	I3	2	Port4 Non-Removable Enable, Active high. Please connect to digital 3.3V power through a resistor (10Kohm ±5%).
LPEN	I3	22	Low Power Enable, Active high. Please connect to digital high.
Ethernet			
RXIP	AB	7	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	8	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	10	Transmit data output positive pin for both 10BASE-T and 100BASE-TX
TXON	AB	11	Transmit data output negative pin for both 10BASE-T and 100BASE-TX
RSET_BG	AO	3	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
Clocks			

XTLI	I3	77	12MHz Crystal / 27MHz OSC clock input for HUB controller
XTLO	O3	80	12MHz Crystal output for HUB controller
XSCI	I3	81	12MHz Crystal input for LAN controller
XSCO	O3	82	12MHz Crystal output for LAN controller
XTL25I	I18	98	25MHz ± 0.005% Crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25O	O18	99	25MHz Crystal or oscillator clock output.
12MCK	O3	46	12MHz clock output if 12MCKEN_N was in low state
12MCKEN_N	I3 /PU	48	0: Enable 12MCK 1: Disable 12MCK
SEL27_N	I3/PU	41	0: XTLI pin clock source is 27MHz clock input 1: XTLI / XTLO clock source is 12MHz Crystal or XTLI clock source is 12MHz clock input
EEPROM Interface			
EECK	B5/PD/T	56	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	57	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	58	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
USB LED			
GREEN1, GREEN2, GREEN3,	O3, B/PD, O3,	42 25 21	Green LED indicator for DSPORT1~3 For compound application or embedded system, downstream ports that always connected inside the system can be set as non-removable based on the state of corresponding status LED, pin GREEN 1~3. If the pin is pull high in the initial stage (POR reset), the corresponding port will be set as non-removable. (Feature Limitation: Green 1 & Green 2 pull-high concurrently will enable vendor proprietary function that may affect system compatibility. System integrator should evade configuring both port #1 and #2 as non-removable by this strapping feature)
BO4_LED	O5	36	This pin drives high and low in turn (blinking) to indicate TX data transfer going on whenever the downstream bulk out data transfer on DP4/DM4. This pin drives low if no downstream bulk out data transfers.
Ethernet LED			
LINK_LED	O5	30	Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state.
SPEED_LED	O5	29	Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode.
FDX_LED	O5	28	Full Duplex and collision detected LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode. When in half duplex mode and the Ethernet PHY detects collision, it will be driven low (or blinking).
Misc. Pins			
RESET_H_N	I5	13	Active low. External reset input.
RESET_D_N	I5/PD/S	74	Active low. External reset input.
EXTWAKEUP_N	I5/PU/S	38	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 12MHz clock to be effective.
GPIO_2	B5/PD	44	General Purpose Input/ Output Pin 2.
GPIO_1	B5/PD	45	General Purpose Input/ Output Pin 1.
GPIO_0/PME	B5/PD	47	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wakeup event detected. Please refer to 4.1.2 Flag of bit 12 (PME_PIN).

TEST/SCL	I3/PD B	14	0: Normal operation 1: Test mode active I2C: Clock output (24C02)
PWREN1_N/SDA	B	39	Active low. Power enable output for DSPORT1~3 PWREN1_N is the only power-enable output for Gang mode.
TEST0	I5/S	68	Test pin. For normal operation, users should connect to ground.
TEST1	I5/S	67	Test pin. For normal operation, users should connect to ground.
TEST2	I5/PU/S	66	Test pin. For normal operation, users should keep this pin NC.
TCLK_EN	I5/PD/S	61	Test pin. For normal operation, users should keep this pin NC.
TCLK_0	I5/PD	60	Test pin. For normal operation, users should keep this pin NC.
TCLK_1	I5/PD	59	Test pin. For normal operation, users should keep this pin NC.
On-chip Regulator Pins			
VCC3R3_D	P	16	3.3V Power supply to on-chip 3.3V to 1.8V voltage regulator.
GND3R3	P	17	Ground pin of on-chip 3.3V to 1.8V voltage regulator.
V18F	P	15	1.8V voltage output of on-chip 3.3V to 1.8V voltage regulator.
Power and Ground Pins			
VCCK	P	20, 31, 40, 50, 72, 79	1.8V Digital core power.
VCC3IO	P	26, 64, 78	3.3V Digital I/O power.
VCC3R3_H	P	24	3.3V Power supply.
GND	P	1, 6, 18, 23, 33, 34, 43, 49, 52, 85	Digital ground.
VCC3A3_0	P	51, 65, 93	3.3V analog power input for analog circuit
GND3A3_0	P	53, 69, 94	Analog ground input for analog circuit
VCC33A_H	P	83	3.3V Analog power for USB transceiver.
GND33A_H	P	84	Analog ground for USB transceiver.
VCC33A_PLL	P	75, 89	3.3V Analog power for USB PLL.
GND33A_PLL	P	76, 90	Analog ground for USB PLL.
VCC3A3	P	4	3.3V Analog power for Ethernet PHY bandgap.
GND3A3	P	5	Analog ground for Ethernet PHY.
VCC18A	P	9, 97	1.8V Analog power for Ethernet PHY and 25MHz crystal oscillator.
GND18A	P	12, 100	Analog ground for Ethernet PHY and 25MHz crystal oscillator.

Table 1 : AX88760 Pinout Description

2.2 Hardware Setting

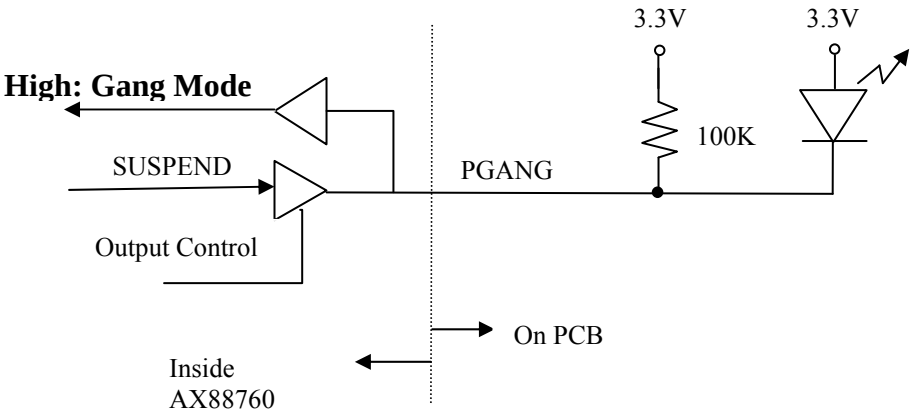
2.2.1 SELF/BUS Power mode setting

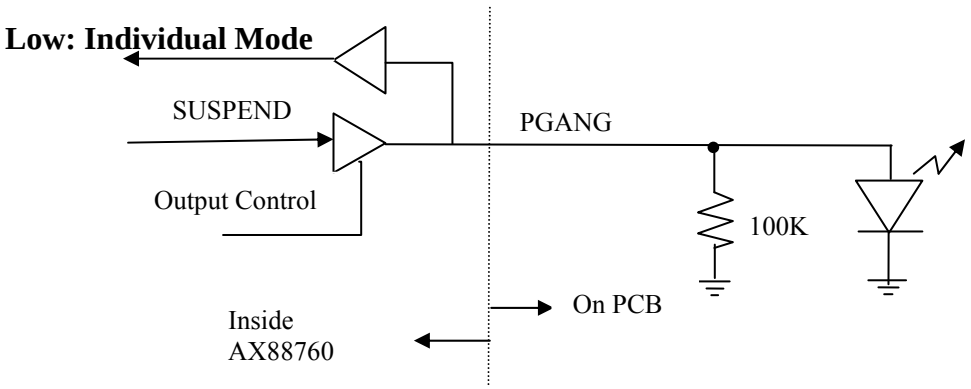
The AX88760 is a high performance USB 2.0 MTT hub with integrated 10/100 Fast Ethernet controller and it is suitable to implement on those self-pwer applications such as the embedded system, docking station, etc. AX88760 can be configured to self-power mode by pulling high the PSELF signal.

Name	Description
PSELF	0: HUB controller is bus-power mode 1: HUB controller is self-power mode

2.2.2 PGANG/SUSPEND setting

The HUB individual/gang power mode setting by PGANG pin setting within 20us after power on reset. PGANG pin will become output mode as a suspend LED indicator after 50ms of release hardware reset.





2.2.3 Non-removable port setting

For a compound application or embedded system, downstream ports that always connected inside the system can be set as non-removable based on the state of corresponding status LED, pin GREEN 1~3. If the pin is pulling high during the initial stage (power on reset) the corresponding port will be set as non-removable. (Feature Limitation: GREEN1 & GREEN2 should evade configuring both port #1 and #2 as non-removable by this strapping feature)

2.2.4 Clock source setting

The HUB controller supports optional 12/27 MHz clock source by SEL27_N pin.

Name	Description
SEL27_N	0: XI pin clock source can be 27MHz OSC-in 1: XI/XO clock source is 12MHz XTAL or OSC-in

3.0 Function Description

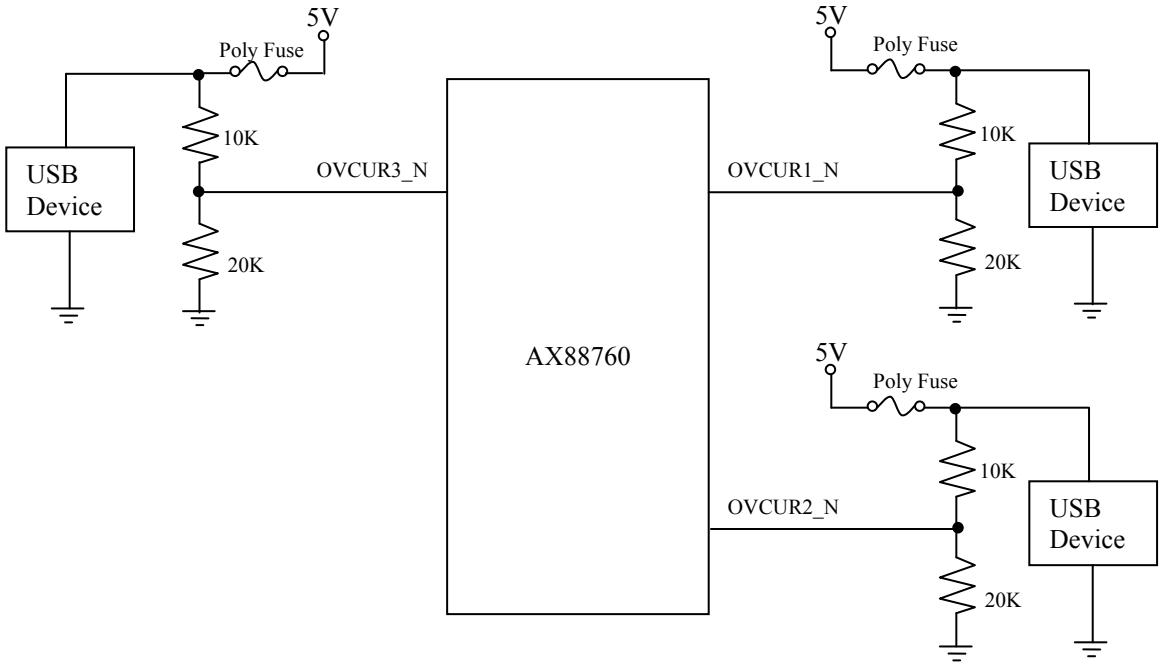
3.1 USB 2.0 MTT HUB

The integrated USB 2.0 MTT HUB is fully complies with Universal Serial Bus Specification Revision 2.0. It implements multiple TT architecture that provide dedicated TT to each downstream (DS) port, which guarantee maximum bandwidth for each connected device when operating multiple mixed-speed peripherals device.

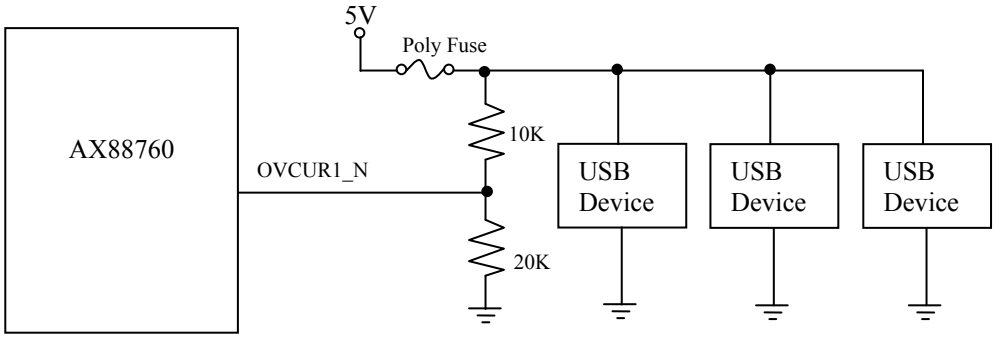
The HUB downstream port supports connection/disconnection detection, over current detection and LED control. The LED control pins GREEN1, GREEN2 and GREEN3 will turn on LED when detects USB device connected on individual downstream port1, port2 and port3.

3.1.1 Individual Mode Port Power Control Using Poly Fuse

The poly fuse will open when over-current situation happening. This will make OVCUR_N to go to 0 volts then detects over-current situation.



3.1.2 Gang Mode Port Power Control Using Poly Fuse



3.2 USB to Ethernet Bridge, 10/100M Ethernet Controller and PHY

The integrated Ethernet Controller of AX88760 is fully compatible with ASIX's AX88772A USB2.0 to 10/100 Fast Ethernet Controller, therefore AX88772A driver can bring up AX88760 Ethernet controller function without any modification.

3.3 Serial EEPROM Controller

The serial EEPROM controller is responsible for reading configuration data automatically from the external serial EEPROM after power-on reset. If the content of EEPROM offset 0x00 (first word) is 0x0000 or 0xFFFF, the Serial EEPROM Loader will not auto-load the EEPROM. In that case, the chip internal default value will be used to configure the chip operation setting and to respond to USB commands, etc.

3.4 Reset Generation

The AX88760 integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset system logic after 1.8V core power ramping up to 1.2V (typical threshold). The external hardware reset input pin, RESET_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RESET_N timing, please refer to 5.4.2 Reset Timing.

3.5 Voltage Regulator

The AX88760 contains an internal 3.3V to 1.8V low-dropout-voltage and low-standby-current voltage regulator. The internal regulator provides up to 240mA of driving current for the 1.8V core/analog power of the chip to satisfy the worst-case power consumption scenario. Also, for the purpose of lowering power consumption before USB configuration, the internal regulator can operate in standby mode to consume less current when the required driving current is less than 30mA. For more details on voltage regulator DC characteristic, please refer to 5.1.6 DC Characteristics of Voltage Regulator.

4.0 Serial EEPROM Memory Map

4.1 Serial EEPROM Memory Map for Ethernet Controller

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00H	5Ah	15h
01H	Flag	
02H	Length of High-Speed Device Descriptor (bytes)	EEPROM Offset of High-Speed Device Descriptor
03H	Length of High-Speed Configuration Descriptor (bytes)	EEPROM Offset of High-Speed Configuration Descriptor
04H	Node ID 1	Node ID 0
05H	Node ID 3	Node ID 2
06H	Node ID 5	Node ID 4
07H	Language ID High Byte	Language ID Low Byte
08H	Length of Manufacture String (bytes)	EEPROM Offset of Manufacture String
09H	Length of Product String (bytes)	EEPROM Offset of Product String
0AH	Length of Serial Number String (bytes)	EEPROM Offset of Serial Number String
0BH	Length of Configuration String (bytes)	EEPROM Offset of Configuration String
0CH	Length of Interface 0 String (bytes)	EEPROM Offset of Interface 0 String
0DH	Length of Interface 1/0 String (bytes)	EEPROM Offset of Interface 1/0 String
0EH	Length of Interface 1/1 String (bytes)	EEPROM Offset of Interface 1/1 String
0FH	EtherPhyMode / PHY Register Offset 1 for Interrupt Endpoint	100 / PHY Register Offset 2 for Interrupt Endpoint
10H	Max Packet Size High Byte	Max Packet Size Low Byte
11H	Secondary PHY_Type [7:5] and PHY_ID [4:0]	Primary PHY_Type [7:5] and PHY_ID [4:0]
12H	Pause Frame Free Buffers High Water Mark	Pause Frame Free Buffers Low Water Mark
13H	Length of Full-Speed Device Descriptor (bytes)	EEPROM Offset of Full-Speed Device Descriptor
14H	Length of Full-Speed Configuration Descriptor (bytes)	EEPROM Offset of Full-Speed Configuration Descriptor

Table 2 : Serial EEPROM Memory Map for Ethernet Controller

4.1.1 Word Count for Preload (00h)

The signature value of 5Ah indicates EEPROM was programmed.
The number of words to be preloaded by the EEPROM loader = 15h.

4.1.2 Flag (01h)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PME_IND	PME_TYP	PME_POL	PME_PIN	0	Reserved	TDPE	CEM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TACE	RDCE	SCPR	0	1	RWU	0	SP

SP: Self-Power (for USB standard command Get Status)
1: Self power.
0: Bus power (default).

RWU: Remote Wakeup support.
1: Indicate that this device supports Remote Wakeup (default).
0: Not support.
SCPR: Software Control PHY Reset.
1: IPRL bit in Vendor command Software Reset Register (20h) resets the embedded Ethernet PHY (default).
0: The USB_Reset on USB bus resets the embedded Ethernet PHY.
RDCE: RX Drop CRC Enable.
1: CRC byte is dropped on received MAC frame forwarding to host (default).
0: CRC byte is not dropped.
TACE: TX Append CRC Enable.
1: CRC byte is generated and appended by the ASIC for every transmitted MAC frame (default).
0: CRC byte is not appended.
CEM: Capture Effective Mode.
1: Enable Capture effective mode (default).
0: Disabled.
TDPE: Test Debug Port Enable.
1: Enable test debug port for chip debug purpose.
0: Disable test debug port and the chip operate in normal function mode (default).

PME_PIN: PME / GPIO_0
1: Set GPIO_0 pin as PME (default).
0: GPIO_0 pin is controlled by vendor command.
PME_POL: PME pin active Polarity.
1: PME active high.
0: PME active low (default).
PME_TYP: PME I/O Type.
1: PME output is a Push-Pull driver.
0: PME output to function as an open-drain buffer (default).
PME_IND: PME indication.
1: A 1.363ms pulse active when detecting wakeup event.
0: A static signal active when detecting wakeup event (default).

4.1.3 Node ID (04~06h)

The Node ID 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 01-23-45-67-89-AB, then Node ID 0 = 01, Node ID 1 = 23, Node ID 2 = 45, Node ID 3 = 67, Node ID 4 = 89, and Node ID 5 = AB.

Default values: Node ID {0,1,2,3,4,5} = 00-0E-C6-87-72-01.

4.1.4 PHY Register Offset for Interrupt Endpoint (0Fh)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
EtherPhyMode			PHY Register Offset 1				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100			PHY Register Offset 2				

PHY Register Offset 1: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 5 and 6 of Interrupt Endpoint packet (default = 00101)

PHY Register Offset 2: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 7 and 8 of Interrupt Endpoint packet (default = 11100)

EtherPhyMode: as below table (default = 000),

EtherPhyMode [2:0]	Function
000	Auto-negotiation enable with all capabilities
001	Auto-negotiation with 100BASE-TX FDX / HDX ability
010	Auto-negotiation with 10BASE-TX FDX / HDX ability
011	Reserved
100	Manual selection of 100BASE-TX FDX
101	Manual selection of 100BASE-TX HDX
110	Manual selection of 10BASE-T FDX
111	Manual selection of 10BASE-T HDX

Note:

1. EtherPhyMode is used to set the operation mode of embedded Ethernet PHY directly. For normal operation mode, set them to 000.
2. This value is latched into embedded Ethernet PHY right after it leaves reset. After that, software driver can still make change Ethernet PHY link ability through vendor command PHY Write Register to access embedded Ethernet PHY register.

4.1.5 Max Packet Size High/Low Byte (10h)

Fill the maximum RX/TX MAC frame size supported by this ASIC. The number must be even number in terms of bytes and should be less than or equal to 2500 bytes (default = 0600h).

4.1.6 Primary/Secondary PHY_Type and PHY_ID (11h)

The 3 bits PHY_Type field for both Primary and Secondary PHY is defined as follows,
000: 10/100M Ethernet PHY or 1M HomePNA PHY.
111: non-supported PHY. For example, the High Byte value of "E0h" means that secondary PHY is not supported.
Default values: Primary {PHY_Type, PHY_ID} = 10h. Secondary {PHY_Type, PHY_ID} = E0h. Note that the PHY_ID of the embedded 10/100M Ethernet PHY is being assigned to "10h".

4.1.7 Pause Frame Free Buffers High Water and Low Water Mark (12H)

When operating in full-duplex mode, correct setting of this field is very important and can affect the overall packet receive throughput performance a great deal. The High Water Mark is the threshold to trigger sending Pause frame and the Low Water Mark is the threshold to stop sending Pause frame. Note that each free buffer count here represents 128 bytes of packet storage space in SRAM.

These setting values are also used in half-duplex mode to activate Backpressure to send /stop jam signal.

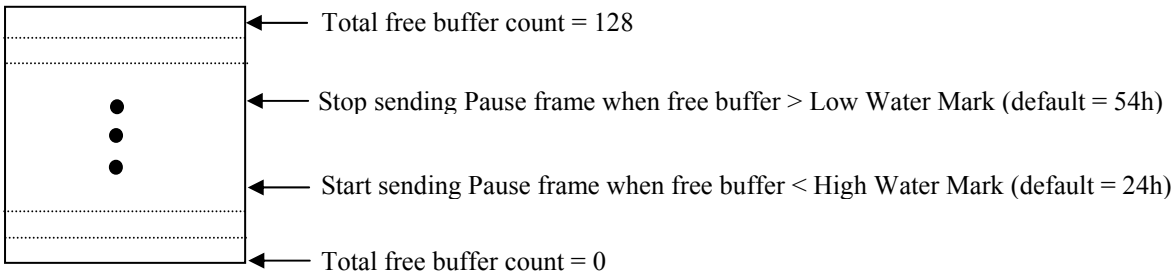


Figure 5 : Water level setting for flow control

4.2 EEPROM Default Settings for Ethernet Controller

The AX88760 supports default EEPROM settings inside chip hardware to enable it to communicate with USB host controller during enumeration when the external EEPROM is blank (prior to being programmed). The default settings inside chip facilitate users to update the EEPROM content through a Windows PC during R&D validation process or program a blank EEPROM mounted on target system PCB during manufacturing process.

Below table shows AX88760's hardware default EEPROM settings being used in the case of blank EEPROM on board. Each of the address offset contains 16-bit data from left to right representing the low-byte and high-byte, respectively. For example, in offset address 0x01, the 0xFC is low-byte data and the 0x11 is high-byte data.

Offset Address	0 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
0x00 0x08	15 00 6E 22	FC 11 7F 12	20 12 19 0E	29 35 44 04	00 0E 44 04	C6 87 44 04	72 01 44 04	09 04 9C 05
0x10 0x18	00 06 FF FF	10 E0 0E 03	42 24 30 00	47 12 30 00	50 35 30 00	FF FF 30 00	00 00 30 00	FF FF 31 00
0x20 0x28	12 01 03 01	00 02 09 02	FF FF 35 00	00 40 01 01	95 0B 04 A0	2A 77 7D 09	01 00 04 00	01 02 00 05
0x30 0x38	FF FF 02 00	00 07 07 05	07 05 03 02	81 03 00 02	08 00 00 07	0B 07 05 84	05 82 02 00	02 00 02 00
0x40 0x48	07 05 00 02	05 02 FF FF	00 02 00 08	00 FF 95 0B	04 03 2A 77	30 00 01 00	FF FF 01 02	12 01 03 01
0x50 0x58	09 02 00 07	35 00 07 05	01 01 81 03	04 A0 08 00	7D 09 A0 07	04 00 05 82	00 05 02 40	FF FF 00 00
0x60 0x68	07 05 05 02	03 02 40 00	40 00 00 DD	00 07 FF FF	05 84 AA AA	02 40 BB BB	00 00 22 03	07 05 41 00
0x70 0x78	53 00 2E 00	49 00 20 00	58 00 43 00	20 00 6F 00	45 00 72 00	6C 00 70 00	65 00 2E 00	63 00 12 03
0x80	41 00	58 00	38 00	38 00	37 00	37 00	32 00	20 00
0x88~FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF

Table 3 : EEPROM Default Settings for Ethernet Controller

4.3 An Example of EEPROM Settings for Ethernet Controller

Below table shows the typical (93C56) EEPROM settings for Ethernet controller.

Each of the address offset contains 16-bit data from left to right representing the low-byte and high-byte, respectively. For example, in offset address 0x01, the 0xED is low-byte data and the 0x71 is high-byte data.

Offset Address	0 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
0x00 0x08	15 5A 60 22	**ED 71** 71 12	20 12 19 0E	29 27 3D 04	**00 00** 3D 04	**00 00** 3D 04	**00 01** 3D 04	09 04 9C 05
0x10 0x18	00 06 FF FF	**10 E0** **0E 03**	54 24 **30 00**	40 12 **30 00**	49 27 **30 00**	FF FF **30 00**	00 00 **30 00**	FF FF **31 00**
0x20 0x28	12 01 03 01	00 02 09 02	FF FF 27 00	00 40 01 01	**95 0B** 04 **E0**	**2A 77** **00** 09	01 00 04 00	01 02 00 03
0x30 0x38	FF FF 02 00	00 07 07 05	07 05 03 02	81 03 00 02	08 00 00 FF	0B 07 04 03	05 82 30 00	02 00 FF FF
0x40 0x48	12 01 03 01	00 02 09 02	FF FF 27 00	00 08 01 01	**95 0B** 04 **E0**	**2A 77** **00** 09	01 00 04 00	01 02 00 03
0x50 0x58	FF FF 00 00	00 07 07 05	07 05 03 02	81 03 40 00	08 00 00 DD	A0 07 FF FF	05 82 AA AA	02 40 BB BB
0x60 0x68	**22 03** **65 00**	**41 00** **63 00**	**53 00** **2E 00**	**49 00** **20 00**	**58 00** **43 00**	**20 00** **6F 00**	**45 00** **72 00**	**6C 00** **70 00**
0x70 0x78	**2E 00** **32 00**	**12 03** **41 00**	**41 00** FF FF	**58 00** FF FF	**38 00** FF FF	**38 00** FF FF	**37 00** FF FF	**37 00** FF FF
0x80~FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF

Table 4 : An Example of EEPROM Settings for Ethernet Controller

4.3.1 EEPROM User-defined Fields for Ethernet Controller

Users can define some EEPROM fields to identify their Ethernet controller such as the Vendor/Product IDs, MAC address, Serial number, etc. The following table shows the user-defined fields of Ethernet controller EEPROM content, users can change these fields based on their application requirement.

Field Definition	Address Offset	Default Values	Description
Vender ID (VID)	0x24 0x44	95 0B	ASIX's VID is 0x0B95
Product ID (PID)	0x25 0x45	2A 77	The PID of AX88760's Ethernet controller
Node ID	0x04 ~0x06	00 00 00 00 00 01	Node ID 0 ~ 5
Power Mode	0x01 0x2C 0x4C	ED 01(disable Serial Interfaces) E0 (high-byte only) E0 (high-byte only)	Self Power mode (Note 1)
Remote Wakeup	0x01 0x2C 0x4C	ED 01(disable Serial Interfaces) E0 (high-byte only) E0 (high-byte only)	Enable the "remote wakeup" function. (Note 1)
Maximum Power under High Speed Mode	0x2D	00 (low-byte only)	0mA (Note 2)
Maximum Power under Full Speed Mode	0x4D	00 (low-byte only)	0mA (Note 2)
Ethernet PHY Type/ID	0x11	10 E0	Primary PHY ID is 0x10 Secondary PHY is not supported (Note 3)
Manufacture String	0x60~0x70	22 03 41 00 53 00 49 00 58 00 20 00 45 00 6C 00 65 00 63 00 2E 00 20 00 43 00 6F 00 72 00 70 00 2E 00	"ASIX Elec. Corp." (Note 4)
Product String	0x71~0x79	12 03 41 00 58 00 38 00 38 00 37 00 37 00 32 00 41 00	"AX88772A" (Note 4)
Serial Number String	0x19~0x1F	0E 03 30 00 30 00 30 00 30 00 30 00 31 00	"000001" (Note 4)

Table 5 : EEPROM User-defined Fields for Ethernet Controller

Note 1: Power Mode/Remote Wakeup/PME Settings

The offset 0x01 field of Ethernet controller EEPROM is used to configure the Power mode, Remote Wakeup and PME.
The high byte of EEPROM offset 0x2C and 0x4C fields are used to configure the "bmAttributes" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus Spec Rev 2.0 for the detailed description of the "bmAttributes" field of Standard Configuration Descriptor.

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
7	*bmAttributes*	1	Bitmap	Configuration characteristics D7: Reserved (set to one) D6: Self-powered D5: Remote Wakeup D4...0: Reserved (reset to zero) D7 is reserved and must be set to one for historical reasons. A device configuration that uses power from the bus and a local source reports a non-zero value in *bMaxPower* to indicate the amount of bus power required and sets D6. The actual power source at runtime may be determined using the GetStatus(DEVICE) request (see Section 9.4.5). If a device configuration supports remote wakeup, D5 is set to one.

Users should refer to below **Table 6** to modify the values of EEPROM offset 0x01, 0x2C and 0x4C based on your application requirement.

Power Mode	Remote Wakeup	EEPROM Offset 0x01		EEPROM Offset 0x2C and 0x4C	
		Low Byte	High Byte	Low Byte	High Byte
Self Power	Enable	ED	71	04	E0
	Disable	E9	71	04	C0

Table 6 : Power Mode and Remote Wakeup Setting for Ethernet Controller

Note 2: Maximum Power Consumption from Bus

The low byte of EEPROM offset 0x2D and 0x4D fields are used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported the value of maximum power consumption from bus to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. User should configured the integrated of Ethernet controller as a non-removable and self-powered device. Therefore the value of maximum power consumption from bus can be zero.

Offset	Field	Size	Value	Description
8	*bMaxPower*	1	mA	Maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. The USB System Software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

Table 7 : Standard Configuration Descriptor

Note 3: Ethernet PHY ID/Type Setting

The default PHY ID of embedded Ethernet PHY is designated to 0x10. The Secondary PHY ID field is unnecessary. Users can keep 0xE0 for Secondary PHY ID field.

Note 4: Manufacture String, Product String, and Serial Number String Settings

In these string fields, the first byte indicates the string length, for example, 0x22 in Manufacturing String means that there are 34 bytes total in the entire string, including the length indication byte. The second byte is the string type indication, which should be 0x03 for ASCII characters. The actual characters of desired string start from the 3rd byte.

5.0 Electrical Specifications

5.1 DC Characteristics

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCK	Digital core power supply	- 0.3 to 2.16	V
VCC18A	Analog Power. 1.8V	- 0.3 to 2.16	V
VCC3IO	Power supply of 3.3V I/O	- 0.3 to 4	V
VCC3R3_D	Power supply of on-chip voltage regulator	- 0.3 to 4	V
VCC3R3_H	Power supply of 3.3V	- 0.3 to 4	V
VCC3A3_0	Analog Power 3.3V for USB HUB controller	- 0.3 to 3.8	V
VCC3A3	Analog Power 3.3V for Ethernet PHY bandgap	- 0.3 to 3.8	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	- 0.3 to 4	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	- 0.3 to 4	V
V_{IN18}	Input voltage of 1.8V I/O	- 0.3 to 2.16	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.3 to 4.0	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.3 to 5.8	V
T_{STG}	Storage temperature	- 40 to 150	℃
I_{IN}	DC input current	20	mA
I_{OUT}	Output short circuit current	20	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

5.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC3R3_D	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3R3_H	Power supply of 3.3V	2.97	3.3	3.63	V
VCC3A3_0	Analog Power 3.3V for USB HUB controller	2.97	3.3	3.63	V
VCC3A3	Analog Power 3.3V for Ethernet PHY bandgap	2.97	3.3	3.63	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	2.97	3.3	3.63	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	2.97	3.3	3.63	V
V_{IN18}	Input voltage of 1.8 V I/O	0	1.8	1.98	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.63	V
	Input voltage of 3.3 V I/O with 5V tolerance	0	3.3	5.25	V
T_j	Commercial junction operating temperature	0	25	125	℃
T_a	Commercial operating temperature	0	-	70	℃

- Thermal Characteristics

Symbol	Parameter	Rating	Unit
Θ_{JC}	Thermal resistance of junction to case	16.8	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	50.8	°C/W

5.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance		-	2.2	-	pF
C_{OUT}	Output capacitance		-	2.2	-	pF
C_{BID}	Bi-directional buffer capacitance		-	2.2	-	pF

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding a pad capacitance of about 0.5pF to the package capacitance.

5.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0	-10	±1	10	μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

5.1.5 DC Characteristics of 3.3V with 5V Tolerance I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = 5.5V or 0		±5		μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current	V_{in} = 5.5V or 0		±10		μA

5.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3R3_D	Power supply of on-chip voltage regulator.		3.0	3.3	3.6	V
Tj	Operating junction temperature.		0	25	125	℃
Iload	Driving current.	Normal operation	-	-	240	mA
		Standby mode enabled	-	-	30	mA
V18F	Output voltage of on-chip voltage regulator.	VCC3R3_D = 3.3V	1.71	1.8	1.89	V
Vdrop	Dropout voltage.	△V18F = -1%, Iload = 10mA	-	0.1	0.2	V
$\frac{\triangle V18F}{(\triangle VCC3R3\_D \times V18F)}$	Line regulation.	VCC3R3_D = 3.3V, Iload = 50mA	-	0.2	0.4	%/V
$\frac{\triangle V18F}{(\triangle Iload \times V18F)}$	Load regulation.	VCC3R3_D = 3.3V, 1mA ≦ Iload ≦ 240mA	-	0.02	0.05	%/mA
$\frac{\triangle V18F}{\triangle Tj}$	Temperature coefficient.	VCC3R3_D = 3.3V,-40℃ ≦ Tj ≦ 125℃	-	+/-0.2	+/-0.5	mV/℃
Iq_25℃	Quiescent current at 25 ℃.	VCC3R3_D = 3.3V	-	70	100	μA
		VCC3R3_D = 3.3V	-	100	125	μA
Iq_125℃	Quiescent current at 125 ℃.	VCC3R3_D = 3.3V	-	85	115	μA
		VCC3R3_D = 3.3V	-	125	170	μA
Cout	Output external capacitor.		0.1	1	-	μF
ESR	Allowable effective series resistance of external capacitor.		-	0.5	1	Ω

5.2 Power Consumption

Symbol	Description	Conditions			Current	Unit
		Active HUB ports	Host	Device	Typical	
Isusp	AX88760 only (1.8V)	Suspend (Remote-wakeup disable)			58.5	uA
	AX88760 only (3.3V)				1.2	mA
	AX88760 only (1.8V)	Suspend/Ethernet 100Mbps (Remote-wakeup enable)			75.0	mA
	AX88760 only (3.3V)				10.0	mA
	AX88760 only (1.8V)	Suspend/Ethernet unlink (Remote-wakeup enable)			47.0	mA
	AX88760 only (3.3V)				18.0	mA
IV18	Current Consumption of 1.8V	4 (Ethernet 100Mbps + 3 DS ports)	F	F	78.6	mA
IV33	Current Consumption of 3.3V				99.9	mA
IV18	Current Consumption of 1.8V		H	H	89.3	mA
IV33	Current Consumption of 3.3V				130.3	mA
IV18	Current Consumption of 1.8V		H	F	78.6	mA
IV33	Current Consumption of 3.3V				131.1	mA
IV18	Current Consumption of 1.8V	4 (Ethernet 10Mbps + 3 DS ports)	F	F	20.9	mA
IV33	Current Consumption of 3.3V				122.3	mA
IV18	Current Consumption of 1.8V		H	H	25.4	mA
IV33	Current Consumption of 3.3V				125.8	mA
IV18	Current Consumption of 1.8V		H	F	25.4	mA
IV33	Current Consumption of 3.3V				131.3	mA

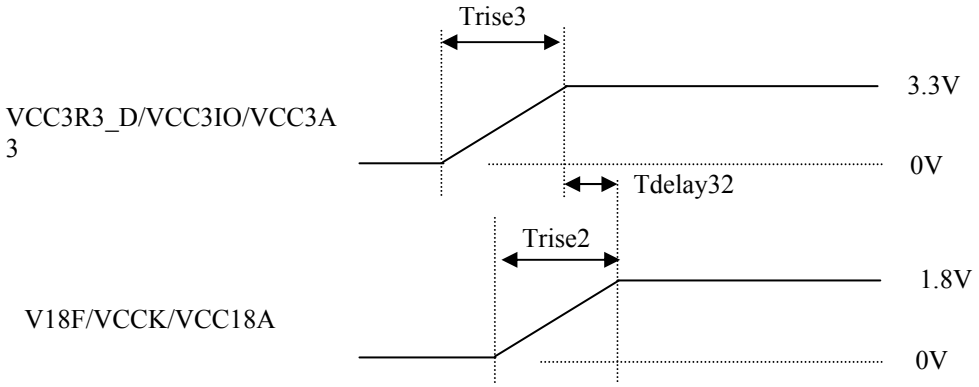
NOTE: The “F” indicates USB Full-speed. The “H” indicates USB High-speed.
NOTE: Magnetic power consumption
100BASE ~ 60mA
10BASE/Unlink ~ 110mA

*Maximum Current Consumption of Demo Board in full operation mode:

Symbol	Description	Conditions			Current			Unit
		Active HUB ports	Host	Device	Min	Typical	Max	
IV18_SYSTEM	Current Consumption of 1.8V	4 (Ethernet 100Mbps + 3 DS ports)	H	F	-	-	100	mA
IV33_SYSTEM	Current Consumption of 3.3V				-	-	230	mA
Total Current	Total current measured on 5V USB VBUS input for bus-powered Hub.				-	-	330	mA

5.3 Power-up Sequence

At power-up, the AX88760 requires the VCC3R3_D/VCC3IO/VCC3A3/VCC33A_H/ VCC33A_PLL power supply to rise to nominal operating voltage within Trise3 and the V18F/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.

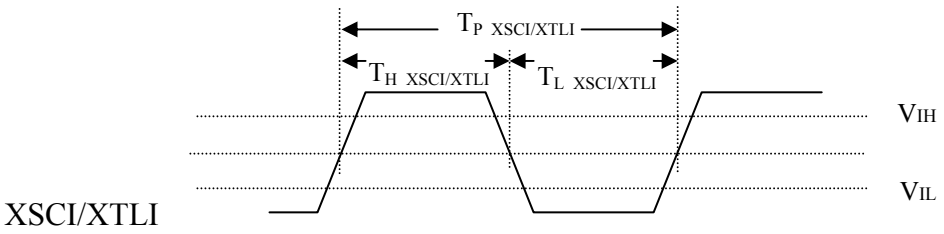


Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	1	-	10	ms
T_{rise2}	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.8V rise time delay		-5	-	5	ms

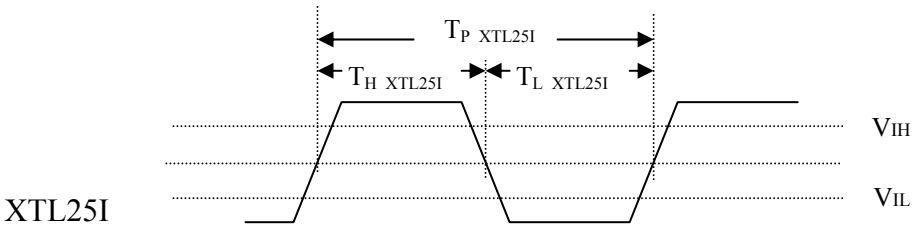
5.4 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on C_L (Output load) =50pF.

5.4.1. Clock Timing

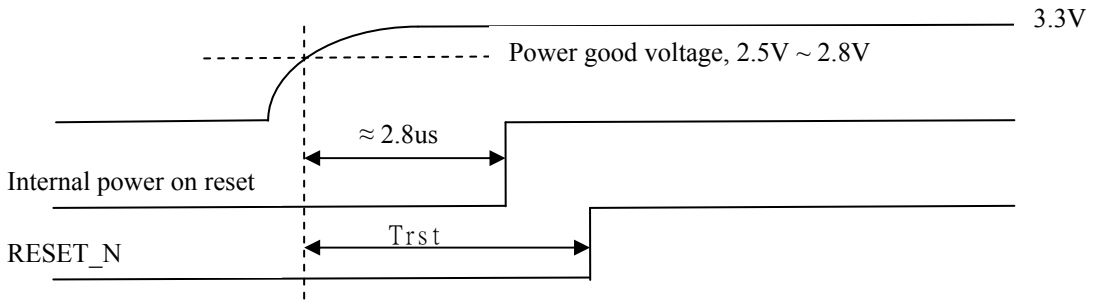


Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{P\_XSCI/XTLI}$	XSCI/XTLI clock cycle time		-	83.33	-	ns
$T_{H\ XSCI/XTLI}$	XSCI/XTLI clock high time		-	41.6	-	ns
$T_{L\ XSCI/XTLI}$	XSCI/XTLI clock low time		-	41.6	-	ns



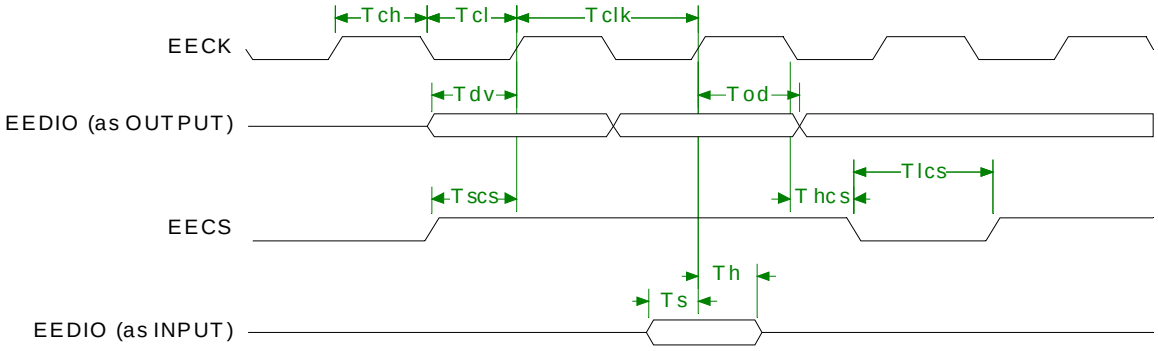
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{P\ XTL25I}$	XTL25I clock cycle time		-	40.0	-	ns
$T_{H\ XTL25I}$	XTL25I clock high time		-	20.0	-	ns
$T_{L\ XTL25I}$	XTL25I clock low time		-	20.0	-	ns

5.4.2. Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	RESET_N release reset from power good	2.8	-	-	us

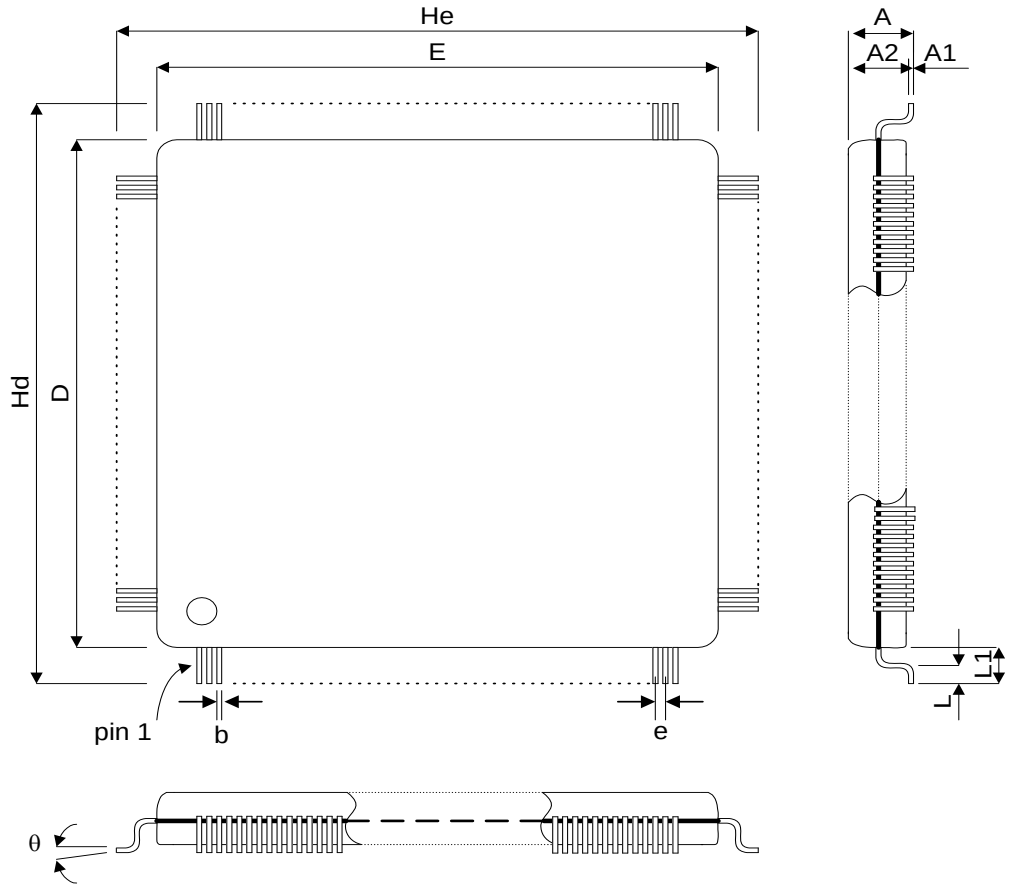
5.4.3. Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

6.0 Package Information

AX88760 100-pin LQFP package



Symbol	Millimeter		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
D		12.00	
E		12.00	
e	-	0.40	-
Hd	-	14.00	-
He	-	14.00	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-
θ	0°	3.5°	7°

7.0 Ordering Information

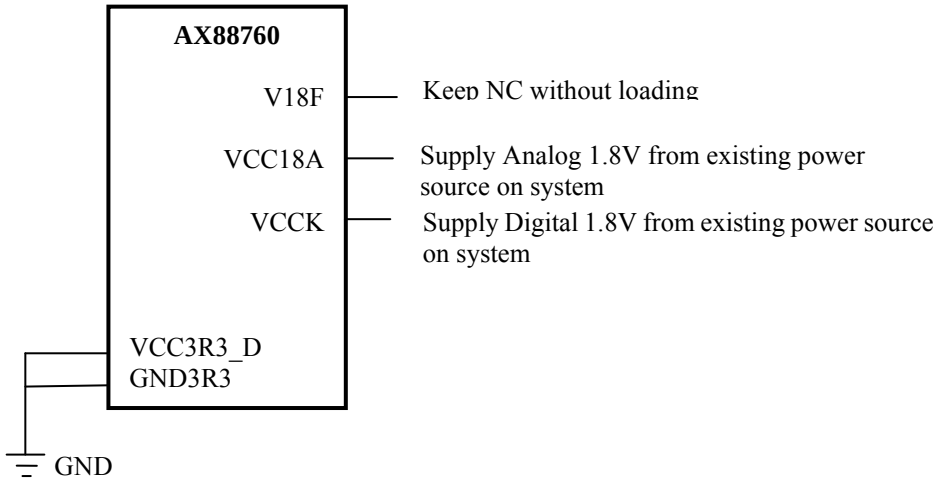
Part Number	Description
AX88760 LF	AX88760: Product Name (100 pin). L: LQFP Package. F: Lead Free.

8.0 Revision History

Revision	Date	Comment
V1.00	2009/10/09	Initial release.
V1.01	2010/07/07	1. Corrected some I/O type descriptions in Section 2.1. 2. Corrected some descriptions in Section 2.2.3. 3. Added more power consumption information in Section 5.2.

Appendix A: Disable AX88760 voltage regulator

The AX88760 integrates an on-chip 3.3V to 1.8V voltage regulator for single-power supply system design. If the system have 1.8V power source already, user may like to disable AX88760 voltage regulator and use the existing 1.8V power source (probably a higher efficiency version). In that case, user can connect VCC3R3_D and GND3R3 to ground, keep V18F open. Please refer to below picture for details.



AX88760 will disable the on-chip voltage regulator when the VCC3R3_D was connected to GND.

Figure 6 : Disable AX88760 Voltage Regulator

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