AX88772C
USB 2.0 to 10/100M Fast Ethernet Controller with Microsoft AOAC Support

Features

Document No: AX88772C/V1.31/04/11/16

- Single chip USB 2.0 to 10/100M Fast Ethernet controller
- Single chip USB 2.0 to RMII, support HomePNA and HomePlug PHY
- Single chip USB 2.0 to Reverse-RMII, supports glueless MAC-to-MAC connections

- **USB Device Interface**
  - Integrates on-chip USB 2.0 transceiver and SIE compliant to USB Spec 1.1 and 2.0
  - Supports USB Full and High Speed modes with Bus-Power or Self-Power capability
  - Supports 4 endpoints on USB interface
  - Supports AutoDetach power saving. Detach from USB host when Ethernet cable is unplugged
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (US Patent Approval)

- **Fast Ethernet Controller**
  - Integrates 10/100Mbps Fast Ethernet MAC/PHY
  - IEEE 802.3 10BASE-T/100BASE-TX compatible
  - IEEE 802.3 100BASE-FX compatible
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Embedded SRAM for RX/TX packet buffering
  - Supports IPv4/ IPv6 packet Checksum Offload Engine(COE) to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP & IPv6 TCP/UDP/ICMPv6 checksum check & generation
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control
  - Supports 2 VLAN ID filtering, received VLAN Tag (4 bytes) can be stripped off or preserved
  - PHY loop-back diagnostic capability
  - Supports multiple unicast MAC destination address filter

- **Support Wake-on-LAN Function**
  - Supports Suspend Mode and Remote Wakeup via Link-change, Magic packet, MS wakeup frame and external wakeup pin
  - Supports Protocol Offload (ARP & NS) for Windows 7 Networking Power Management
  - Optional PHY power down during Suspend Mode
  - Supports 32 MS Wakeup Patterns
  - Supports Wakeup packet indication
  - Supports Receive Filter Wakeup

- **Versatile External Media Interface**
  - Optional RMII interface in MAC mode allows AX88772C to work with HomePNA and HomePlug PHY
  - Optional Reverse-RMII interface in PHY mode allows AX88772C to support glueless MAC-to-MAC connections

- **Advanced Power Management Features**
  - Supports dynamic power management to reduce power dissipation during idle or light traffic
  - Supports very low power Wake-on-LAN (WOL) mode when the system enters suspend mode and waits for network events to wake it up.

- Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors)
- Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- Integrates on-chip voltage regulator and only requires a single 3.3V power supply
- Single 25MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Small form factor with 64-pin LQFP RoHS compliant package
- Operating commercial temperature range 0˚C to 70˚C

ASIX ELECTRONICS CORPORATION
4F, NO.8, Hsin Ann Rd., Hsinchu Science Park, Hsin-Chu City, Taiwan, R.O.C. 300
TEL: 886-3-579-9500 **FAX: 886-3-579-9558**
http://www.asix.com.tw/

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Target Applications

PC/Internet

Consumer Electronics

Figure 1 : Target Applications

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Typical System Block Diagrams

- **Hosted by USB to operate with internal Ethernet PHY only**

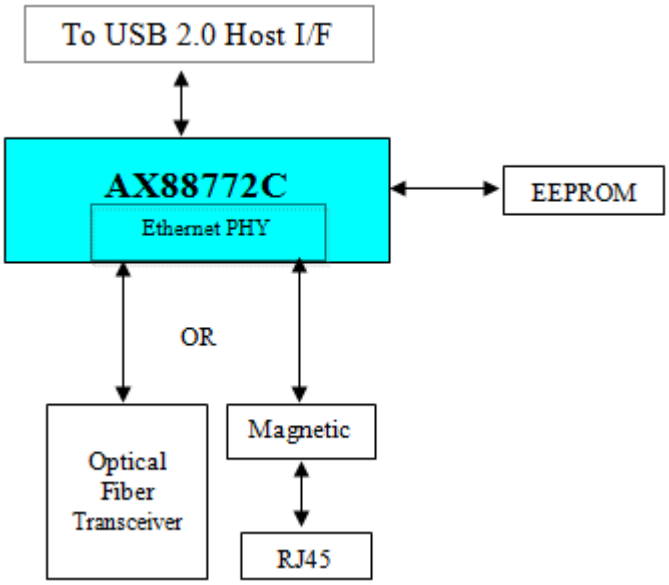

Figure 2 : USB 2.0 to LAN Adaptor (MAC mode)

- **Hosted by USB to operate with either internal Ethernet PHY or RMII (in MAC mode)**

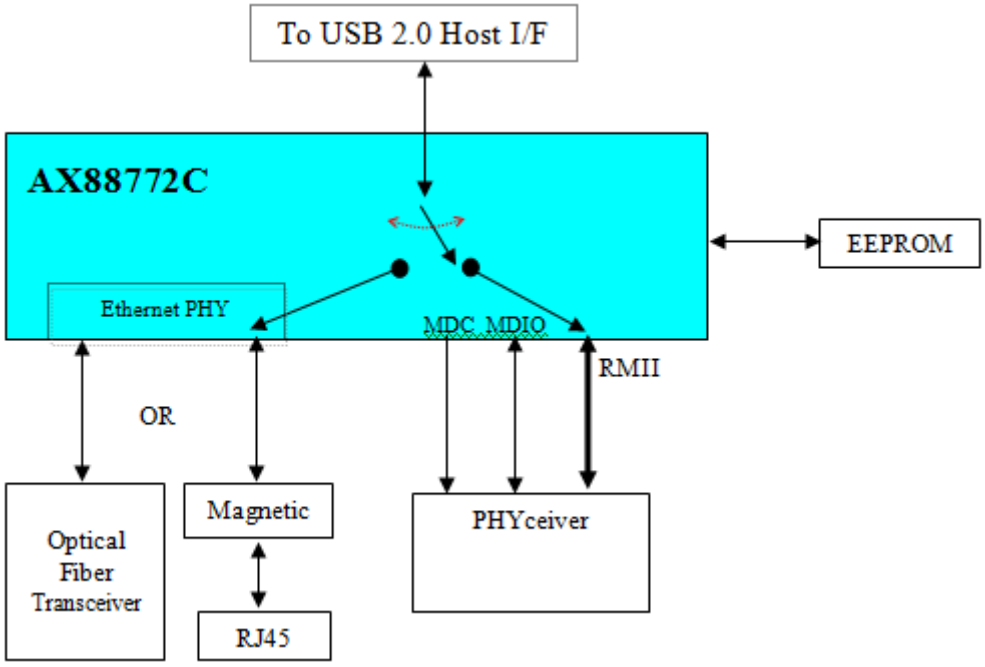

Figure 3 : USB 2.0 to Fast Ethernet and external PHYceiver Combo (MAC mode)

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- **Hosted by USB to operate with either internal Ethernet PHY (in MAC mode) or Reverse-RMII (in PHY mode)**

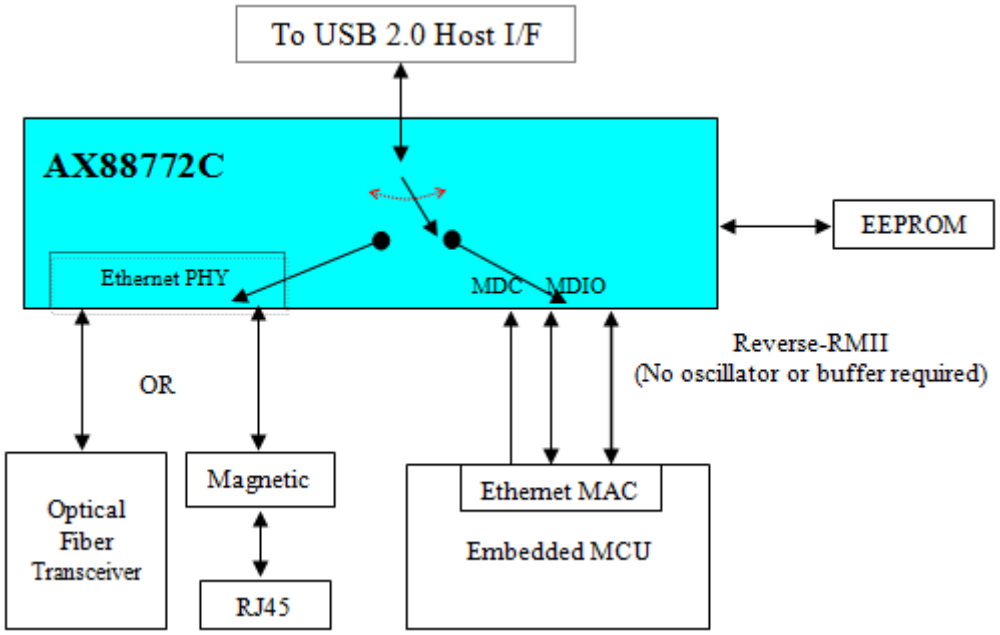

Figure 4 : Bridging Embedded MCU to USB 2.0 Host Interface (PHY mode)

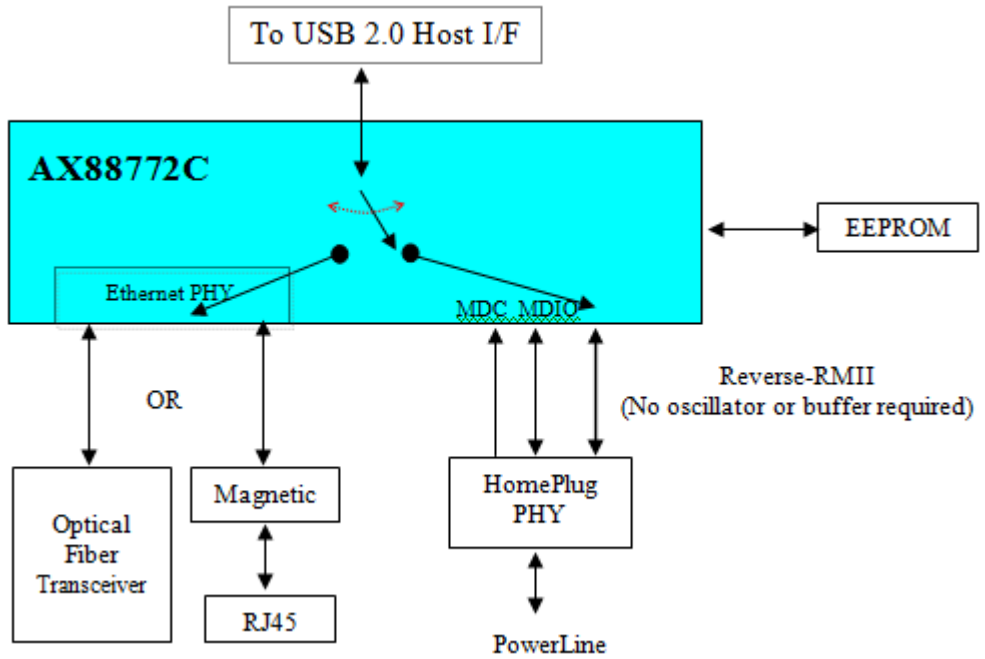

Figure 5 : USB 2.0 to HomePlug Adaptor (PHY mode)

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1 Introduction

1.1 General Description

The AX88772C USB 2.0 to 10/100M Fast Ethernet controller with Microsoft AOAC(Always On Always Connected) support is a high performance and highly integrated ASIC which enables a low cost, small form factor, and simple plug-and-play Fast Ethernet network connection capability for desktops, notebook PCs, Ultrabooks, cradles/port replicators/docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88772C can be used in any embedded system with a USB host microcontroller requiring a twisted pair physical network connection. Featuring a USB interface (compliant with USB specification V2.0 and V1.1) to communicate with a USB Host Controller, the AX88772C also integrates on-chip Ethernet MAC and PHY (IEEE802.3 and IEEE802.3u compatible) and embedded memory. Additionally, the AX88772C needs only a single 25MHz crystal to drive both the USB and Ethernet PHYs.

The AX88772C offers a wide array of features including IPv4/IPv6 checksum offload engine, Protocol Offload(ARP & NS), HP Auto-MDIX, and IEEE 802.3x and back-pressure flow control. The AX88772C also offers multiple power management Wake-on-LAN features, including Magic Packet, Microsoft Wakeup Frame, Link Status Change, 32 Microsoft Wakeup Patterns and Wakeup Packet Indication that allows the AOAC platform to enter a low-power "Connected Standby" state and wake on a desired network pattern.

The AX88772C provides an optional Multi-Function-Bus portion A and B (MFA and MFB) for external PHY or external MAC for different application purposes. The MFA/MFB can be a reduce-media-independent interface (RMII) for implementing HomePlug, HomePNA, etc. functions. The MFA/MFB can also be a Reverse Reduced-MII (Reverse-RMII) for glueless MAC-to-MAC connections to any MCU with Ethernet MAC RMII interface. In addition, the MFA/MFB can be configured as general purpose I/O.

1.2 Block Diagram

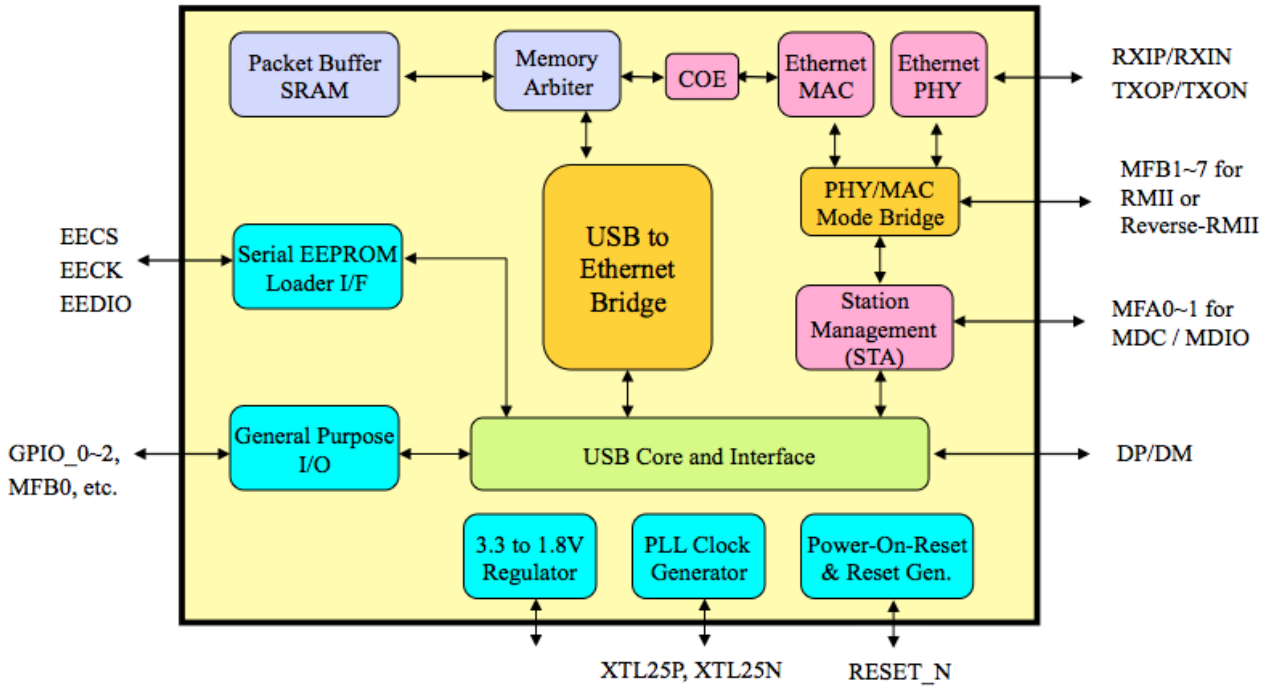

Figure 6 : Block Diagram

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1.3 Pinout Diagram

- 64-pin LQFP package

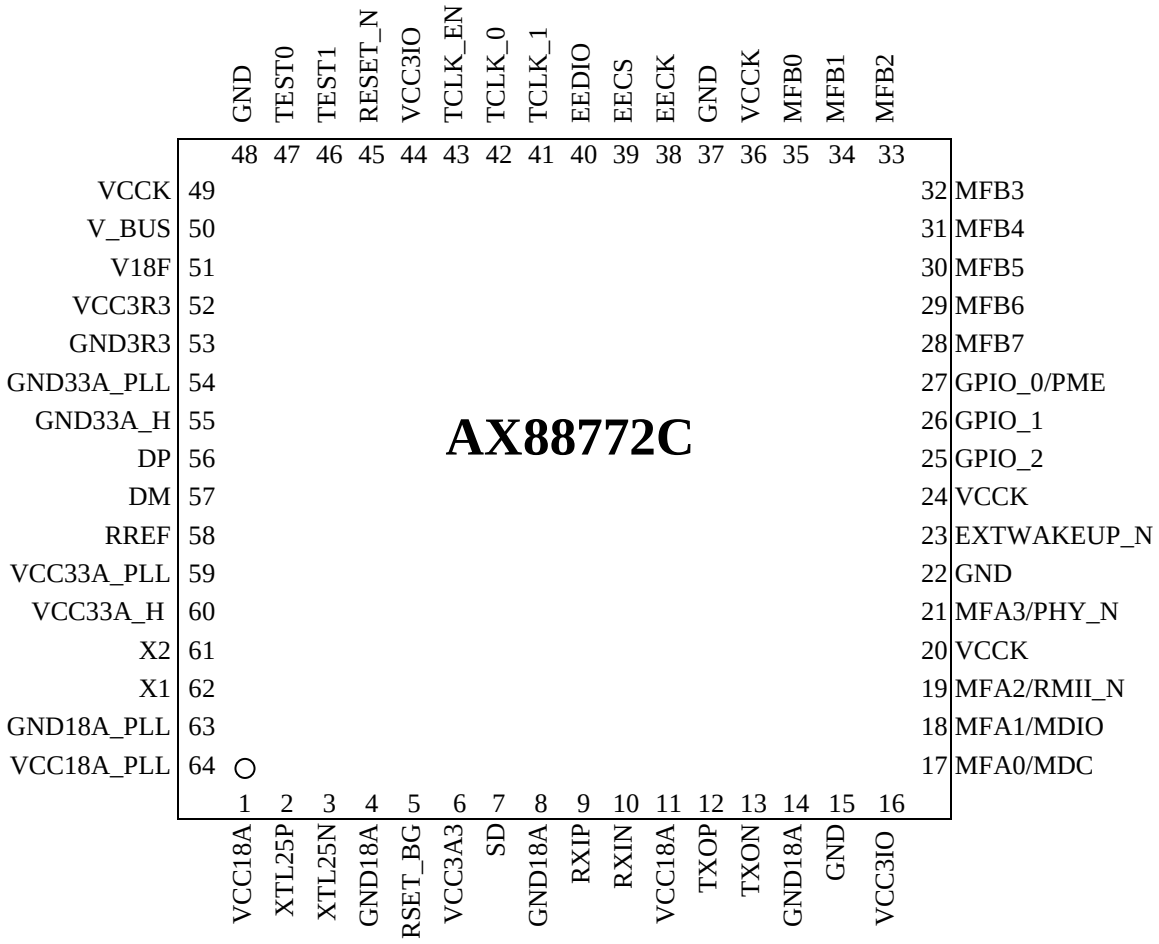

Figure 7 : Pinout Diagram

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2 Signal Description

The following abbreviations apply to the following pin description table.

I18	**Input, 1.8V**	**AI**	**Analog Input**
I3	**Input, 3.3V**	**AO**	**Analog Output**
I5	**Input, 3.3V with 5V tolerant**	**AB**	**Analog Bi-directional I/O**
O3	**Output, 3.3V**	**PU**	**Internal Pull Up (75K)**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**PD**	**Internal Pull Down (75K)**
P	**Power Pin**	**S**	**Schmitt Trigger**
		T	**Tri-stateable**

Note: Every output or bi-directional I/O pin is 8mA driving strength.

2.1 Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	AB	56	USB 2.0 data positive pin.
DM	AB	57	USB 2.0 data negative pin.
V_BUS	I5/PD/S	50	VBUS pin input. Please connect to USB bus power.
RREF	AI	58	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
Serial EEPROM Interface			
EECK	B5/PD/T	38	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	39	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	40	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Ethernet PHY Interface			
XTL25P	I18	2	25MHz ± 0.005% crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25N	O18	3	25MHz crystal or oscillator clock output.
RXIP	AB	9	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	10	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	12	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	AB	13	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
RSET_BG	AO	5	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
Misc. Pins			
RESET_N	I5/PU/S	45	Chip reset input. Active low. This is the external reset source used to reset this chip. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	23	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 25MHz clock to be effective.
GPIO_2	B5/PD	25	General Purpose Input/ Output Pin 2.
GPIO_1	B5/PD	26	General Purpose Input/ Output Pin 1. This pin is default as input pin after power-on reset. This pin is also for Default WOL Ready Mode setting; please refer to section 2.2 Settings.

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GPIO_0/PME	B5/PD	27	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected. Please refer to section 2.2 Settings.
MFB7	B5/PU I5 I5	28	This is a multi-function pin. Please refer to section 2.2 Settings. MFB7: RMII : RXD0 Reverse_RMII : TXD0
MFB6	B5/PU I5 I5	29	This is a multi-function pin. Please refer to section 2.2 Settings. MFB6: RMII : RXD1 Reverse_RMII : TXD1
MFB5/ REF50	B5/PU B5	30	This is a multi-function pin. Please refer to section 2.2 Settings. MFB5: When RMII enable, The REF50 in/out direction is determined by EEPROM Flag [1] setting. Please refer to section 2.2 Settings.
MFB4	B5/PU O3 O3	31	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXD0 Reverse_RMII : RXD0
MFB3	B5/PU O3 O3	32	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXD1 Reverse_RMII : RXD1
MFB2	B5/PU O3 O3	33	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXEN Reverse_RMII : CRSDV
MFB1	B5/PU I5 I5	34	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : CRSDV Reverse_RMII : TXEN
MFB0	B5/PU	35	This is a GPIO pin. Please refer to section 2.2 Settings.
MFA3/ PHY_N	O3 I5/PU	21	It is a multi-function pin. The default is USB Speed indicator. When USB bus is in Full speed, this pin will tri-state continuously. When USB bus is in High speed, this pin drives low continuously. This pin tri-state and drive low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer. MFB1~7 bus is determined by setting of this input pin when MFA2 sets 0: 0: Reverse_RMII (PHY mode). 1: RMII (MAC mode). Please refer to PIN configuration of MFA and MFB in section 2.2 Settings.
MFA2/ RMII_N	O3 I5/PU	19	It is a multi-function pin. The default is Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state. MFB1~7 function is determined by setting of this input pin: 0: Reverse_RMII/RMII . 1: MFB bus as GPIO function. Please refer to PIN configuration of MFA and MFB in section 2.2 Settings.
MFA1/ MDIO	O3 B5/PU	18	It is a multi-function pin. The default is Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode. This pin can perform as MDIO when enabling Reverse_RMII/RMII.

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MFA0/ MDC	O3 O3 I5/PU	17	It is a multi-function pin. The default is Full Duplex and collision detected LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode. When in half duplex mode and the Ethernet PHY detects collision, it will be driven low (or blinking). This pin can perform as MDC when enabling Reverse_RMII/RMII: RMII : Output. Reverse_RMII : Input.
SD	I	7	Fiber signal detected Twisted pair operation: Please connect to GND directly or through a resistor. Fiber operation: Please connect to the fiber transceiver signal detect output pin. Please refer to Section 6.1.7 for the detailed SD signal DC Characteristics spec.
TEST0	I5/S	47	Test pin. For normal operation, user should connect to ground.
TEST1	I5/S	46	Test pin. For normal operation, user should connect to ground.
X1	I3	62	Test pin. For normal operation, user should connect to ground.
X2	O3	61	Test pin. No connection
TCLK_EN	I5/PD/S	43	Test pin. For normal operation, user should keep this pin NC.
TCLK_0	I5/PD	42	Test pin. For normal operation, user should keep this pin NC.
TCLK_1	I5/PD	41	Test pin. For normal operation, user should keep this pin NC.
On-chip Regulator Pins			
VCC3R3	P	52	3.3V Power supply to on-chip 3.3V to 1.8V voltage regulator.
GND3R3	P	53	Ground pin of on-chip 3.3V to 1.8V voltage regulator.
V18F	P	51	1.8V voltage output of on-chip 3.3V to 1.8V voltage regulator.
Power and Ground Pins			
VCCK	P	20, 24, 36, 49	Digital Core Power. 1.8V.
VCC3IO	P	16, 44	Digital I/O Power. 3.3V.
GND	P	15, 22, 37, 48	Digital Ground.
VCC33A_H	P	60	Analog Power for USB transceiver. 3.3V.
GND33A_H	P	55	Analog Ground for USB transceiver.
VCC33A_PLL	P	59	Analog Power for USB PLL. 3.3V.
GND33A_PLL	P	54	Analog Ground for USB PLL.
VCC3A3	P	6	Analog Power for Ethernet PHY bandgap. 3.3V.
VCC18A	P	1, 11	Analog Power for Ethernet PHY and 25MHz crystal oscillator. 1.8V.
GND18A	P	4, 8, 14	Analog Ground for Ethernet PHY and 25MHz crystal oscillator.
VCC18A_PLL	P	64	Analog Power for USB PLL. 1.8V.
GND18A_PLL	P	63	Analog Ground for USB PLL.

Table 1 : Pinout Description

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2.2 Hardware Setting For Operation Mode and Multi-Function Pins

The following hardware settings define the desired function or interface modes of operation for some multi-function pins. The logic level shown on setting pin below is loaded from the chip I/O pins during power on reset based on the setting of the pin's pulled-up (as logic '1') or pulled-down (as logic '0') resister on the schematic.

- Chip Operation Mode setting :

Pin# 19, Pin #21	Operation Modes		Remarks
1x (default)	MAC mode	Internal PHY	The Chip Operation Mode is determined by Pin# 19 (MFA2/RMII_N) and Pin #21 (MFA3/PHY_N) value of AX88772C, which is called hardware setting.
01	MAC mode	RMII	
00	PHY mode	Reverse-RMII	

- EECK pin: USB force to Full Speed mode :

EECK	Description
0	Normal operation (default).
1	USB force to Full Speed mode. External pull-up resistor must be 4.7Kohm.

- GPIO_1 pin: Determines whether this chip will go to Default WOL Ready Mode after power on reset. The WOL stands for Wake-On-LAN.

GPIO_1	Description
0	Normal operation mode (default, see Note 1).
1	Enable Default WOL Ready Mode. Notice that the external pulled-up resistor must be 4.7Kohm. For more details, please refer to APPENDIX A. Default Wake-On-LAN (WOL) Ready Mode

Note 1: This is the default with internal pulled-down resistor and doesn't need an external one.

- EEPROM Flag [12]: Defines the multi-function pin GPIO_0 / PME

GPIO_0 is a general purpose I/O normally controlled by vendor commands. Users can change this pin to operate as a PME (Power Management Event) for remote wake up purpose. Please refer to 4.1.2 Flag of bit 12 (PME_PIN).

- MFA_3 ~ MFA_0 pins: There are 4 multi-function pins for LED display purpose and as GPIO control by vendor command.

PIN Name	Default definition	Vendor Command LED_MUX	Vendor Command VMFAIO	RMII_N enable
MFA3	LED_USB indicater	Sel_LED3	MFAIO_3	-
MFA2	LED_Ethernet_LINK_Active	Sel_LED2	MFAIO_2	-
MFA1	LED_Ethernet_Speed	Sel_LED1	MFAIO_1	MDIO
MFA0	LED_Ethernet_Duplex_Collision	Sel_LED0	MFAIO_0	MDC

Table 2 : MFA_3 ~ MFA_0 pin configuration

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- PIN configuration of MFA and MFB

Pin# 19 MFA2/RMII_N	Pin #21 MFA3/PHY_N	Description		
1: MFB7~MFB0 0: RMII	1: MAC Mode 0: PHY Mode	PIN Name	Function	Pin Type
1	X	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
1	X	MFB1	MFBIO1	Bidirection, controlled by MFBIOEN1
1	X	MFB2	MFBIO2	Bidirection, controlled by MFBIOEN2
1	X	MFB3	MFBIO3	Bidirection, controlled by MFBIOEN3
1	X	MFB4	MFBIO4	Bidirection, controlled by MFBIOEN4
1	X	MFB5	MFBIO5	Bidirection, controlled by MFBIOEN5
1	X	MFB6	MFBIO6	Bidirection, controlled by MFBIOEN6
1	X	MFB7	MFBIO7	Bidirection, controlled by MFBIOEN7
1	X	MFA0	Refer to MFA Configuration	
1	X	MFA1	Refer to MFA Configuration	
1	X	MFA2	Refer to MFA Configuration	
1	X	MFA3	Refer to MFA Configuration	
0	1	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
0	1	MFB1	CRSDV	Input
0	1	MFB2	TXEN	Output
0	1	MFB3	TXD1	Output
0	1	MFB4	TXD0	Output
0	1	MFB5	REF50	Input/Output control by EEPROM flag[1]
0	1	MFB6	RXD1	Input
0	1	MFB7	RXD0	Input
0	1	MFA0	MDC	Output
0	1	MFA1	MDIO	I/O
0	0	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
0	0	MFB1	TXEN	Input
0	0	MFB2	CRSDV	Output
0	0	MFB3	RXD1	Output
0	0	MFB4	RXD0	Output
0	0	MFB5	REF50	Input/Output control by EEPROM flag[1]
0	0	MFB6	TXD1	Input
0	0	MFB7	TXD0	Input
0	0	MFA0	MDC	Input
0	0	MFA1	MDIO	I/O

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3 Function Description

3.1 USB Core and Interface

The USB core and interface contains a USB 2.0 transceiver, serial interface engine (SIE), USB bus protocol handshaking block, USB standard command, vendor command registers, logic for supporting bulk transfer, and an interrupt transfer, etc. The USB interface is used to communicate with a USB host controller and is compliant with USB specification V1.1 and V2.0.

3.2 10/100M Ethernet PHY

The 10/100M Fast Ethernet PHY is compliant with IEEE 802.3 and IEEE 802.3u standards. It contains an on-chip crystal oscillator, PLL-based clock multiplier, and a digital phase-locked loop for data/timing recovery. It provides over-sampling mixed-signal transmit drivers compliant with 10/100BASE-TX transmit wave shaping / slew rate control requirements. It has a robust mixed-signal loop adaptive equalizer for receiving signal recovery. It contains a baseline wander corrective block to compensate data dependent offset due to AC coupling transformers. It supports auto-negotiation and auto-MDIX functions.

3.3 MAC Core

The MAC core supports 802.3 and 802.3u MAC sub-layer functions, such as basic MAC frame receive and transmit, CRC checking and generation, filtering, forwarding, flow-control in full-duplex mode, and collision-detection and handling in half-duplex mode, etc. It provides a reduce-media-independent interface (RMII) for implementing Fast Ethernet and HomePNA functions.

The MAC core interfaces to external RMII/Reverse-RMII interfaces and the embedded 10/100M Ethernet PHY. The selection among the interfaces is done via setting Pin# 19 (MFA2/RMII_N) and Pin #21 (MFA3/PHY_N) of AX88772C package pinout during power on reset (see 2.2) and using the USB vendor command, Software Interface Selection register. Figure 8 shows the data path diagram of 10/100M Ethernet PHY and RMII/Reverse-RMII interfaces to MAC core.

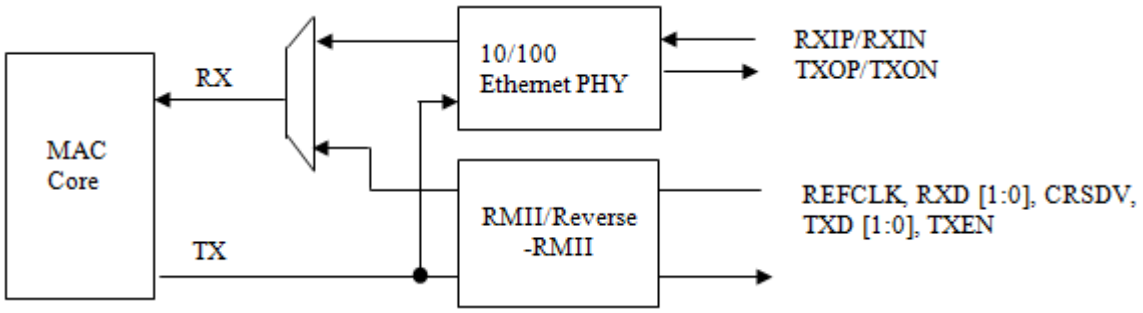

Figure 8 : Internal Data path Diagram of 10/100M Ethernet PHY and RMII/Reverse-RMII Interfaces

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3.4 Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in hardware

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 extention header and routing header type 0 supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet
- Checksum error indication on RX direction for TCP/UDP/ICMP/ICMPv6/IGMP packets with error checksum

3.5 Operation Mode

For simple USB 2.0 to Ethernet applications, user can use the AX88772C, which operates with internal Ethernet PHY.

AX88772C supports following three operation modes: (Ref. 2.2 Hardware Setting For Operation Mode and Multi-Function Pins)

1. MAC mode
2. PHY mode

Below provides a detailed description for the three operation modes:

- In MAC mode, the AX88772C Ethernet block is configured as an Ethernet MAC. From a system application standpoint, AX88772C can be used as a USB 2.0 to LAN Adaptor (see Figure 2) or a USB 2.0 to Fast Ethernet and HomePNA Combo (see Figure 3).

  In MAC mode, the AX88772C internal datapath can work with internal Ethernet PHY or RMII interface by setting Software Interface Selection register. Note that the PHY_ID for the internal Ethernet PHY and external one are defined in below Table 3. Please refer to below Figure 9, Figure 10 for RMII example.

- In PHY mode, the AX88772C Ethernet block is configured as an Ethernet PHY interface. In this case, an external microcontroller with Ethernet MAC can interface with AX88772C as if it were to interface with an Ethernet PHY chip, and AX88772C can act as a USB to Reverse-RMII bridge chip for the microcontroller to provide USB 2.0 device interface for some system applications (see Figure 4).
  Please refer to below Figure 11, Figure 12 for Reverse-RMII example.

STA PHY_ID	MAC mode	PHY mode
Embedded Ethernet PHY PHY_ID [4:0]	10h	10h
External Media Interface PHY_ID [4:0]	{Secondary PHY_ID [4:0]}	{Secondary PHY_ID [4:1], 0}

Note: The value of Secondary PHY_ID [4:0] is defined in EEPROM memory map 4.1.6

Table 3 : PHY_ID Definition Source

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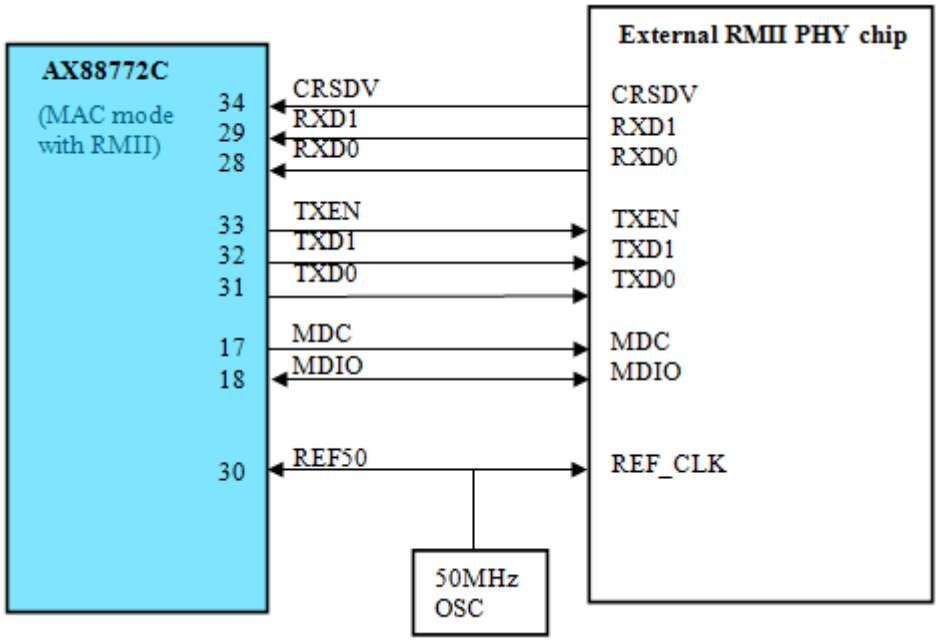

Figure 9 : RMII to External PHY chip with 50MHz OSC

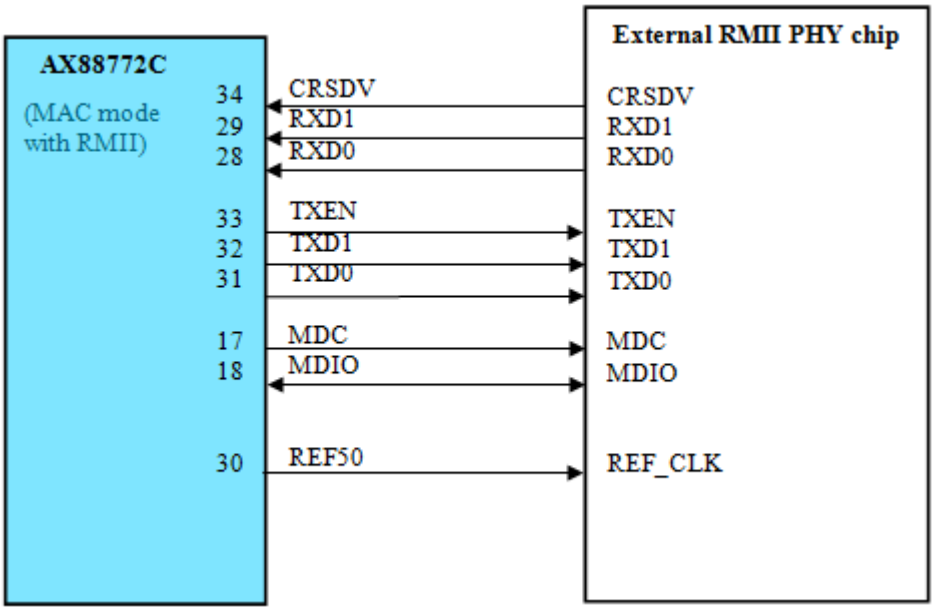

Figure 10 : RMII Interface to External PHY chip

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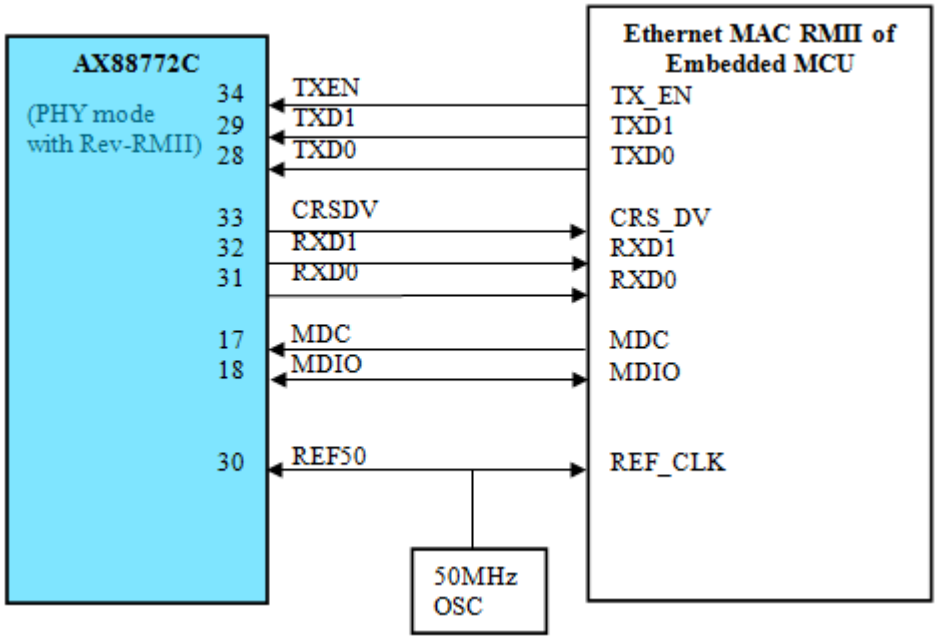

Figure 11 : Reverse-RMII to External MAC Device with 50MHz OSC

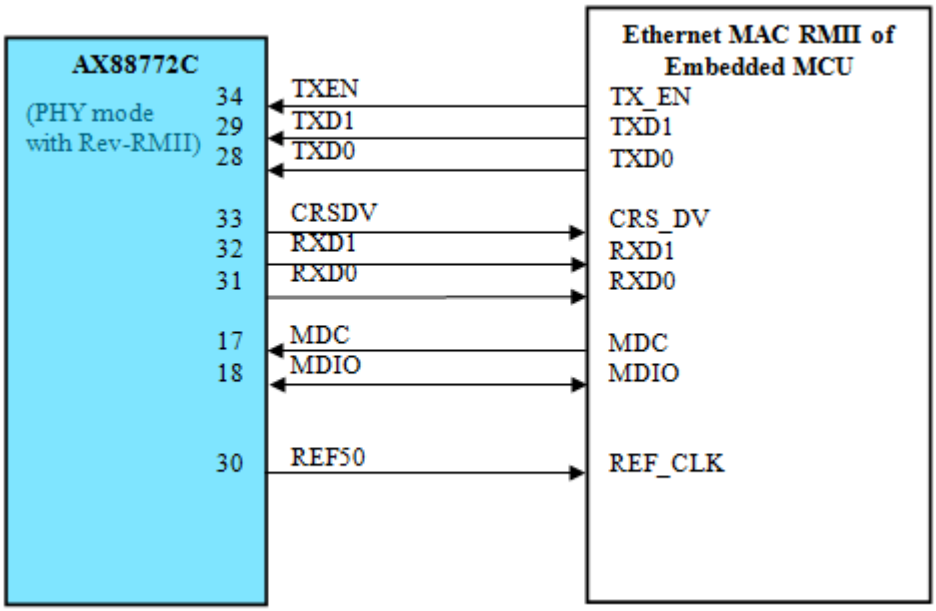

Figure 12 : Reverse-RMII Interface to External MAC Device

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3.6 Station Management (STA)

The Station Management interface provides a simple, two-wire, serial interface to connect to a managed PHY device for the purpose of controlling the PHY and gathering status from the PHY. The Station Management interface allows communicating with multiple PHY devices at the same time by identifying the managed PHY with 5-bit, unique PHY_ID. The PHY ID of the embedded 10/100M Ethernet PHY is being pre-assigned to "1_0000".

The Figure 13 shows the internal control MUX of the Station Management interface when doing read in MAC operation mode, the "mdin" signal will be driven from the embedded 10/100M Ethernet PHY only if PHY ID matches with "1_0000", otherwise, it will always be driven from the external MDIO pin of the ASIC.

The Station Management unit also reports the basic PHY status when operating in PHY mode acting as a PHY role (see 0). For detailed register description, please refer to the Station Management Registers in PHY mode.

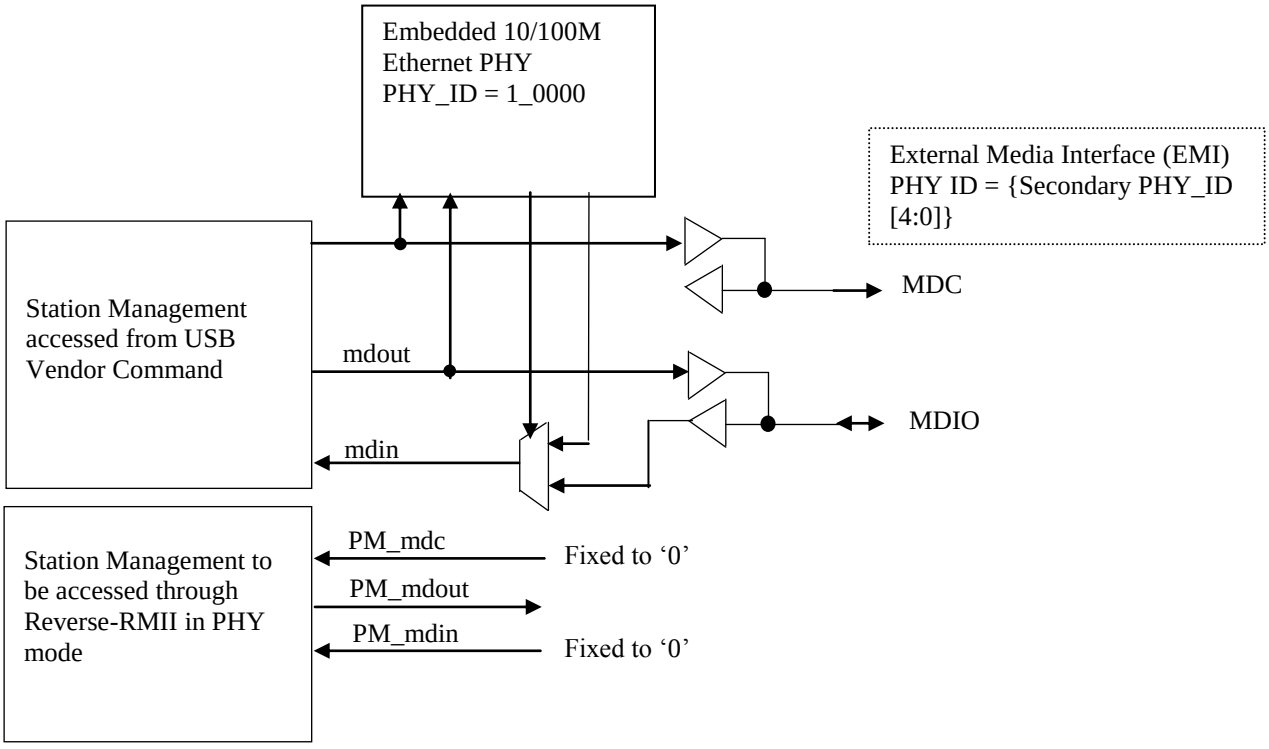

Figure 13 : Internal Control MUX of Station Management Interface in MAC mode

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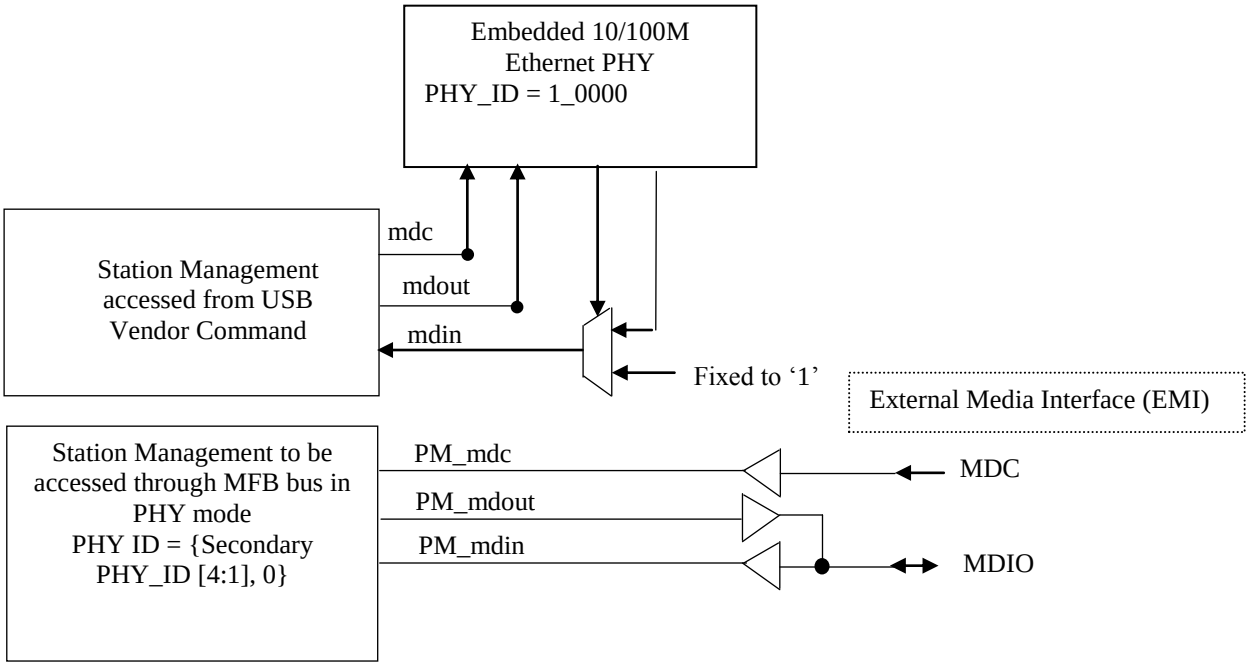

Figure 14 : Internal Control MUX of Station Management Interface in PHY mode

3.7 Memory Arbiter

The memory arbiter block is responsible for storing received MAC frames into on-chip SRAM (packet buffer) and then forwarding it to the USB bus upon request from the USB host via Bulk In transfer. It also monitors the packet buffer usage in full-duplex mode for triggering PAUSE frame (or in half-duplex mode to activate Backpressure jam signal) transmission out on TX direction. The memory arbiter block is also responsible for storing MAC frames received from the USB host via Bulk Out transfer and scheduling transmission out towards Ethernet network.

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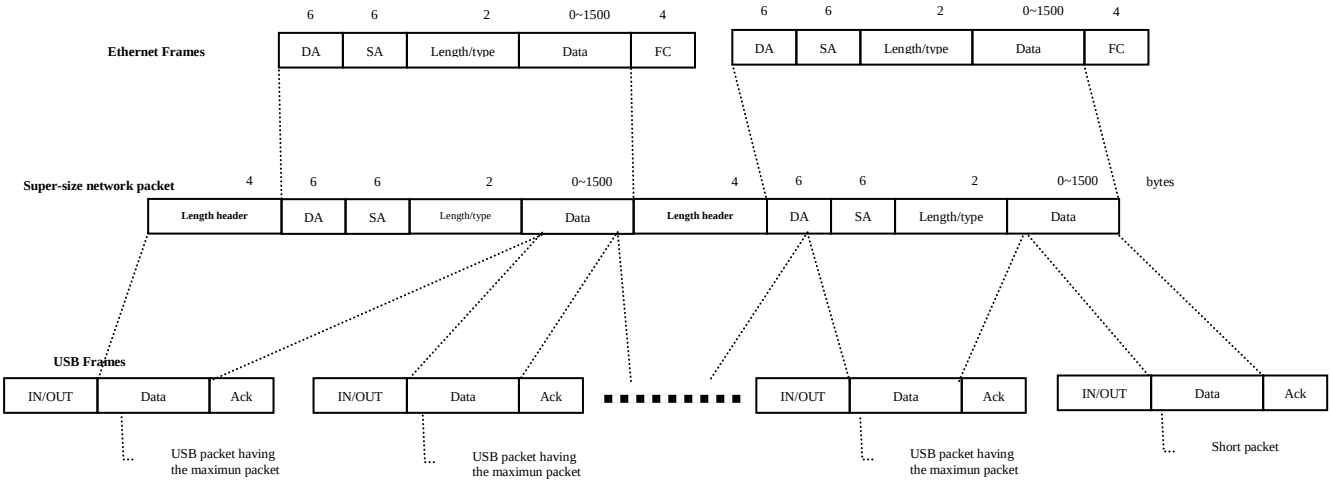
3.8 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (US Patent Approval) to offload software burden and to offer very high packet transfer throughput over USB bus.

3.8.1 Ethernet/USB Frame Format Bridge



3.9 Serial EEPROM Loader

The serial EEPROM loader is responsible for reading configuration data automatically from the external serial EEPROM after power-on reset. If the content of EEPROM offset 0x00 (low byte of first word) is 0x00 or 0xFF, the Serial EEPROM Loader will not auto-load the EEPROM. If the content of EEPROM offset 0x18 (low byte of 18th word) is not equal to (0xFF - SUM [EEPROM offset 07H ~ 0EH]). In that case, the chip internal default value will be used to configure the chip operation setting and to respond to USB commands, etc.

3.10 General Purpose I/O

There are 3 general-purpose I/O pins (named GPIO_0/1/2), 8 multi-function pins group B (named MFB0/1/2/3/4/5/6/7) and 4 multi-function pins group A (named MFA0/1/2/3) provided by this ASIC.

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3.11 Clock Generation

The AX88772C integrates internal oscillator circuits for 25MHz, respectively, which allow the chip to operate cost effectively with just external 25MHz crystals. There are also three PLL circuits integrated in the chip to generate precise clocks.

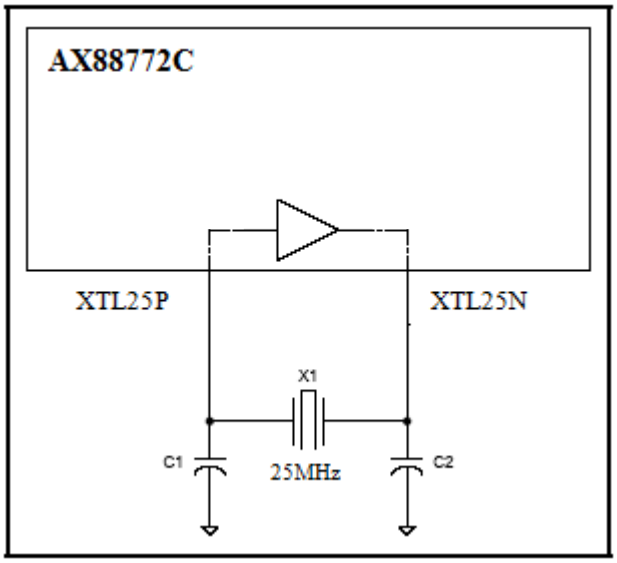
The external 25MHz crystal or oscillator, via pins XTL25P/XTL25N, provides the reference clock to the other two internal PLL circuit to generate a free-run 100MHz clock source for the Reverse-RMII/RMII modes of AX88772C and a 125MHz clock source for the embedded Ethernet PHY use.

The AX88772C can provide REF50 (50MHz output) in Reverse-RMII/RMII modes. This output clock is derived from the internal 100MHz PLL circuit.

The external 25MHz Crystal spec is listed in below table. For more details on crystal timing, please refer to 6.5.1 Clock Timing and AX88772C demo board schematic reference.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±30ppm
Frequency Stability Over Operating Temperature Range		±30ppm
Equivalent Series Resistance	ESR	70 Ohm max.
Load Capacitance	CL	20pF
Operation Temperature Range		0℃ ~ +70℃, Commerical version
Aging		±3ppm/year

Table 4 : The external 25MHz Crystal Units specifications



For the 25MHz oscillator, its feedback resistor isn't integrated into the 25MHz oscillator, so it is necessary to add feedback resistor on external circuit.

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To implement the external circuits of 25MHz crystal please refer to below. One external 1Mohm resistor on 25MHz crystal oscillator is required.

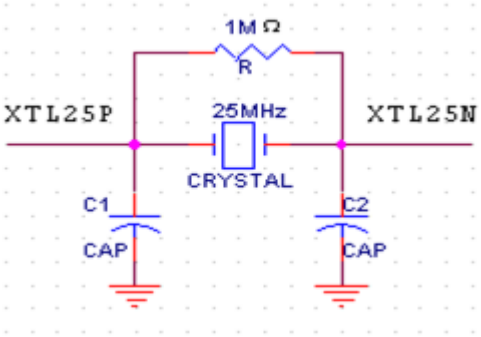

Figure 15 : One external 1M ohm resistor on 25MHz crystal oscillator is necessary

3.12 Reset Generation

The AX88772C integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset system logic after 1.8V core power ramping up to 1.2V (typical threshold). The external hardware reset input pin, RESET_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RESET_N timing, please refer to 6.5.2 Reset Timing.

3.13 Voltage Regulator

The AX88772C contains an internal 3.3V to 1.8V low-dropout-voltage and low-standby-current voltage regulator. The internal regulator provides up to 150mA of driving current for the 1.8V core/analog power of the chip to satisfy the worst-case power consumption scenario. For more details on voltage regulator DC characteristic, please refer to 6.1.6 DC Characteristics of Voltage Regulator.

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4 Serial EEPROM Memory Map

EEPROM OFFSET	HIGH BYTE		LOW BYTE	
00H	0x5A		0x15	
01H	Flag			
02H	Length of High-Speed Device Descriptor (bytes)		EEPROM Offset of High-Speed Device Descriptor	
03H	Length of High-Speed Configuration Descriptor (bytes)		EEPROM Offset of High-Speed Configuration Descriptor	
04H	MAC Address 1		MAC Address 0	
05H	MAC Address 3		MAC Address 2	
06H	MAC Address 5		MAC Address 4	
07H	Language ID High Byte		Language ID Low Byte	
08H	Length of Manufacture String (bytes)		EEPROM Offset of Manufacture String	
09H	Length of Product String (bytes)		EEPROM Offset of Product String	
0AH	Length of Serial Number String (bytes)		EEPROM Offset of Serial Number String	
0BH	Length of Configuration String (bytes)		EEPROM Offset of Configuration String	
0CH	Length of Interface 0 String (bytes)		EEPROM Offset of Interface 0 String	
0DH	Length of Interface 1/0 String (bytes)		EEPROM Offset of Interface 1/0 String	
0EH	Length of Interface 1/1 String (bytes)		EEPROM Offset of Interface 1/1 String	
0FH	EtherPhyMode [2:0]	PHY Register Offset 1 for Interrupt Endpoint	100	PHY Register Offset 2 for Interrupt Endpoint
10H	5'b0	Max Packet Size High Byte[10:8]	Max Packet Size Low Byte[7:0]	
11H	Secondary PHY_Type [7:5] and PHY_ID [4:0]		Primary PHY_Type [7:5] and PHY_ID [4:0]	
12H	Pause Frame Free Buffers High Water Mark		Pause Frame Free Buffers Low Water Mark	
13H	Length of Full-Speed Device Descriptor (bytes)		EEPROM Offset of Full-Speed Device Descriptor	
14H	Length of Full-Speed Configuration Descriptor (bytes)		EEPROM Offset of Full-Speed Configuration Descriptor	
15H~17H	Reserved		Reserved	
18H	Ethernet PHY Power Saving Configuration		EEPROM Checksum	

Table 5 : Serial EEPROM Memory Map

- The value of EEPROM Checksum field, EEPROM offset 0x18 (low byte) = (0xFF - SUM [EEPROM offset 07H ~ 0EH])
- The value of Ethernet PHY Power Saving Configuration field (i.e. high byte of EEPROM offset 0x18) is equal to 2nd byte of Vendor Command 0x20. The AX88772C driver will read this field from high byte of EEPROM offset 0x18 and then writes it to 2nd byte of Vendor Command 0x20 at the end of driver initialization routine and during Suspend mode configuration. This field doesn't affect AX88772C before the driver writes it to Vendor Command 0x20.

Ethernet PHY Power Saving Configuration field

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
WOLLP	0	IPFPS	AutoDetach	IPCOPSC	IPCOPS	IPPSL_1	IPPSL_0

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4.1 Detailed Description

The following sections provide detailed descriptions for some of the fields in serial EEPROM memory map. For other fields not covered here, please refer to the **AX88772C EEPROM User Guide** for more details.

4.1.1 Word Count for Preload (00h)

The number of words to be preloaded by the EEPROM loader = 15h.

4.1.2 Flag (01h)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PME_IND	PME_TYP	PME_POL	PME_PIN	PHY_ISO	1	TDPE	CEM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TACE	RDCE	EPOM	Reserved	1	RWU	REF50_O	SP

SP: Self-Power (for USB standard command Get Status)
1: Self power (default).
0: Bus power.
REF50_O: RMII reference 50MHz clock direction
1: Sets AX88772C provides RMII reference 50MHz clock.
0: Sets AX88772C RMII reference clock source from external 50MHz clock source (default).
RWU: Remote Wakeup support.
1: Indicate that this device supports Remote Wakeup (default).
0: Not support.
EPOM: Embedded PHY copper/fiber Operation Mode
1: Sets embedded PHY in copper mode (default).
0: Sets embedded PHY in fiber mode
RDCE: RX Drop CRC Enable.
1: CRC byte is dropped on received MAC frame forwarding to host (default).
0: CRC byte is not dropped.
TACE: TX Append CRC Enable.
1: CRC byte is generated and appended by the ASIC for every transmitted MAC frame (default).
0: CRC byte is not appended.
CEM: Capture Effective Mode.
1: Capture effective mode enables (default).
0: Disabled.
TDPE: Test Debug Port Enable.
1: Enable test debug port for chip debug purpose.
0: Disable test debug port and the chip operate in normal function mode (default).
PHY_ISO: Set RMII bus to isolate mode when operating in PHY mode.
1: Set RMII bus to isolate mode (default). AX88772C can be in isolate mode when operating in PHY mode with Reverse-RMII. Following output pins are tri-stated in isolate mode.
In Reverse-RMII mode: RXD [1:0] and CRSDV, RXER, except for REF50.
0: Set RMII bus to non-isolate mode.
PME_PIN: PME / GPIO_0
1: Set GPIO_0 pin as PME (default).
0: GPIO_0 pin is controlled by vendor command.
PME_POL: PME pin active Polarity.
1: PME active high.
0: PME active low (default).
PME_TYP: PME I/O Type.
1: PME output is a Push-Pull driver.
0: PME output to function as an open-drain buffer (default).
PME_IND: PME indication.
1: A 1.363ms pulse active when detecting wake-up event.
0: A static signal active when detecting wake-up event (default).

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4.1.3 MAC Address (04~06h)

The MAC Address 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 01-23-45-67-89-ABh, then MAC Address 0 = 01, MAC Address 1 = 23, MAC Address 2 = 45, MAC Address 3 = 67, MAC Address 4 = 89, and MAC Address 5 = AB.

Default values: MAC Address {0, 1, 2, 3, 4, 5} = 0x000E_C687_7201.

4.1.4 PHY Register Offset for Interrupt Endpoint (0Fh)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
EtherPhyMode			PHY Register Offset 1				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100			PHY Register Offset 2				

PHY Register Offset 1: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 5 and 6 of Interrupt Endpoint packet (default = 00101)

PHY Register Offset 2: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 7 and 8 of Interrupt Endpoint packet (default = 00000)

EtherPhyMode: as below table (default = 000),

EtherPhyMode [2:0]	Function
000	Auto-negotiation enable with all capabilities
001	Auto-negotiation with 100BASE-TX FDX / HDX ability
010	Auto-negotiation with 10BASE-TX FDX / HDX ability
011	Reserved
100	Manual selection of 100BASE-TX FDX
101	Manual selection of 100BASE-TX HDX
110	Manual selection of 10BASE-T FDX
111	Manual selection of 10BASE-T HDX

Note:

1. EtherPhyMode is used to set the operation mode of embedded Ethernet PHY directly. For normal operation mode, set them to 000.
2. This value is latched into embedded Ethernet PHY right after it leaves reset. After that, software driver can still make change Ethernet PHY link ability through vendor command PHY Write Register to access embedded Ethernet PHY register.

4.1.5 Max Packet Size High/Low Byte (10h)

Fill the maximum RX/TX MAC frame size supported by this ASIC. The number must be even number in terms of bytes and should be less than or equal to 2048 bytes (default = 0600h).

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4.1.6 Primary/Secondary PHY_Type and PHY_ID (11h)

The 3 bits PHY_Type field for both Primary and Secondary PHY is defined as follows,

000: 10/100M Ethernet PHY or 1M HomePNA PHY.
111: non-supported PHY. For example, the High Byte value of "E0h" means that secondary PHY is not supported.

Default values: Primary {PHY_Type, PHY_ID} = 10h. Secondary {PHY_Type, PHY_ID} = E0h. Note that the PHY_ID of the embedded 10/100M Ethernet PHY is being assigned to "10h".

Secondary PHY_ID always defines The PHY_ID of External Media Interface (EMI) and Secondary PHY_TYPE is not used in that case. Please refer to Table 3 for more information.

4.1.7 Pause Frame Free Buffers High Water and Low Water Mark (12H)

When operating in full-duplex mode, correct setting of this field is very important and can affect the overall packet receive throughput performance a great deal. The High Water Mark is the threshold to trigger sending Pause frame and the Low Water Mark is the threshold to stop sending Pause frame. Note that each free buffer count here represents 128 bytes of packet storage space in SRAM.

These setting values are also used in half-duplex mode to activate Backpressure to send /stop jam signal.

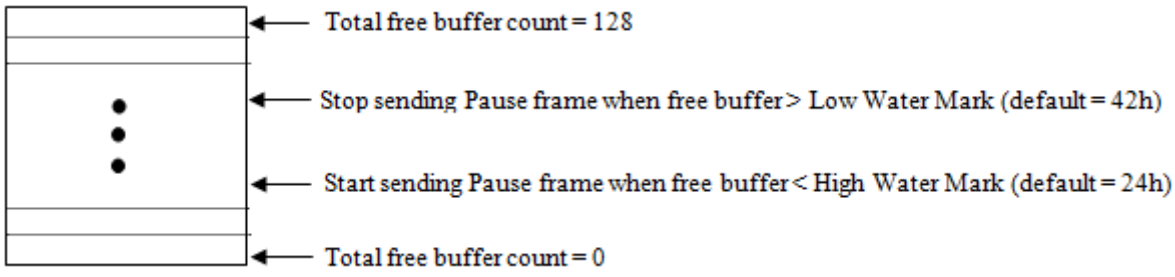

Figure 16 : Water level setting for flow control

4.1.8 Power-Up Steps

After power-on reset, AX88772C will automatically perform the following steps to the Ethernet PHYs via MDC/MDIO lines (only take effect when Chip Operation Mode is in MAC mode with external PHY on RMII interface).

1. Write to PHY_ID of 00h with PHY register offset 00h to power down all PHYs attached to station management interface.
2. Write to Primary PHY_ID with PHY register offset 00h to power down Primary PHY.
3. Write to Secondary PHY_ID with PHY register offset 00h to power down Secondary PHY.

Notice that enabling Default WOL Ready Mode (see 2.2 GPIO_1 Settings) will disable above power-up step (to prevent external Ethernet PHY on RMII interface from entering power-down mode), if external PHY is used.

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4.2 Internal ROM Default Settings

AX88772C supports some default settings inside chip hardware to enable it to communicate with USB host controller during enumeration when the AX88772C EEPROM is blank (prior to being programmed) or the value of EEPROM Checksum field is wrong. The default settings inside chip facilitate users to update the EEPROM content through a Windows PC during R&D validation process or program a blank EEPROM mounted on target system PCB during manufacturing process.

Below table shows AX88772C's internal default settings being used in the case of blank EEPROM or EEPROM with wrong checksum value on board. Each of the address offset contains 16-bit data from left to right representing the low-byte and high-byte, respectively. For example, in offset address 0x01, the 'FD' is low-byte data and the '1D' is high-byte data.

Offset Address	0 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
0x00 0x08	15 **00** 60 22	**FD 1D** 71 12	20 12 19 0E	29 27 3D 04	**00 0E** 3D 04	**C6 87** 3D 04	**72 01** 3D 04	09 04 80 05
0x10 0x18	00 06 **FF 08**	**10 E0** **0E 03**	42 24 **30 00**	40 12 **30 00**	49 27 **30 00**	FF FF **30 00**	00 00 **30 00**	FF FF **31 00**
0x20 0x28	12 01 03 01	00 02 09 02	FF FF 27 00	00 40 01 01	**95 0B** 04 **E0**	**2B 77** **02** 09	**02 00** 04 00	01 02 00 03
0x30 0x38	FF FF 02 00	00 07 07 05	07 05 03 02	81 03 00 02	08 00 00 FF	0B 07 04 03	05 82 30 00	02 00 FF FF
0x40 0x48	12 01 03 01	00 02 09 02	FF FF 27 00	00 08 01 01	**95 0B** 04 **E0**	**2B 77** **02** 09	**02 00** 04 00	01 02 00 03
0x50 0x58	FF FF 00 00	00 07 07 05	07 05 03 02	81 03 40 00	08 00 00 DD	A0 07 FF FF	05 82 AA AA	02 40 BB BB
0x60 0x68	**22 03** **65 00**	**41 00** **63 00**	**53 00** **2E 00**	**49 00** **20 00**	**58 00** **43 00**	**20 00** **6F 00**	**45 00** **72 00**	**6C 00** **70 00**
0x70 0x78	**2E 00** **32 00**	**12 03** **42 00**	**41 00** FF FF	**58 00** FF FF	**38 00** FF FF	**38 00** FF FF	**37 00** FF FF	**37 00** FF FF
0x80~FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF

Table 6 : Internal ROM Memory Map

Note:

1. The default high-byte data of offset 0x00 is 0x00.
2. The default PID/VID is 0x772B/0x0B95.
3. The default "bcdDevice" field (offset 0x26/0x46) is set to 0x0002.
4. The default MAC address is 00-0E-C6-87-72-01, but the real MAC address is 00-00-00-00-00-00 as auto-loaded into the AX88772C MAC Address register. You should manually assign a valid MAC address in the AX88772C driver parameter for normal network operation.
5. The default Manufacture string is "ASIX Elec. Corp.".
6. The default Product string is "AX88772B".
7. The default Serial Number is "000001".
8. The default operation mode is set to Self Power and Remote Wakeup enabled.
9. The default "AutoDetach" function is disabled and set to Cable Off Power Saving Level 0.
10. The default value of EEPROM Checksum field is 0xFF.

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4.2.1 Internal ROM Description

The internal ROM is a fixed value. **User can't modify it.**

Field Definition	Address Offset	Default Values	Description
Vender ID (VID)	0x24 0x44	95 0B	ASIX's VID is 0x0B95
Product ID (PID)	0x25 0x45	2B 77	The PID of AX88772C is 0x772B
MAC Address	0x04 ~0x06	00 0E C6 87 72 01	MAC Address 0 ~ 5
Power Mode/Remote Wakeup/Copper or Fiber Mode	0x01 0x2C 0x4C	FD 1D E0 (high-byte only) E0 (high-byte only)	Self-Power mode, Enable the "remote wakeup" function, Copper Mode (Note 1)
Max Power under High Speed Mode	0x2D	02 (low-byte only)	4mA (Note 2)
Max Power under Full Speed Mode	0x4D	02 (low-byte only)	4mA (Note 2)
Ethernet PHY Type/ID	0x11	10 E0	Primary PHY ID is 0x10 Secondary PHY is not supported
Manufacture String	0x60~0x70	22 03 41 00 53 00 49 00 58 00 20 00 45 00 6C 00 65 00 63 00 2E 00 20 00 43 00 6F 00 72 00 70 00 2E 00	"ASIX Elec. Corp."
Product String	0x71~0x79	12 03 41 00 58 00 38 00 38 00 37 00 37 00 32 00 42 00	"AX88772B"
Serial Number String	0x19~0x1F	0E 03 30 00 30 00 30 00 30 00 30 00 31 00	"000001"
Ethernet PHY Power Saving Configuration	0x18	08 (high-byte only)	Disable "AutoDetach" Set to Cable Off Power Saving Level 0

Table 7 : Internal ROM Description

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Note 1: Power Mode/Remote Wakeup/PME Settings

The offset 0x01 field of AX88772C EEPROM is used to configure the Power mode (i.e. Bus-power or Self-power), Remote Wakeup and PME functions. Please refer to datasheet Section 4 "Serial EEPROM Memory Map" for the detailed description of EEPROM offset 0x01.

The high byte of AX88772C EEPROM offset 0x2C and 0x53 fields are used to configure the "bmAttributes" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus Spec Rev 2.0 for the detailed description of the "bmAttributes" field of Standard Configuration Descriptor.

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
7	*bmAttributes*	1	Bitmap	Configuration characteristics D7: Reserved (set to one) D6: Self-powered D5: Remote Wakeup D4...0: Reserved (reset to zero) D7 is reserved and must be set to one for historical reasons. A device configuration that uses power from the bus and a local source reports a non-zero value in *bMaxPower* to indicate the amount of bus power required and sets D6. The actual power source at runtime may be determined using the GetStatus(DEVICE) request (see Section 9.4.5). If a device configuration supports remote wakeup, D5 is set to one.

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Note 2: Max Power Setting

The low byte of AX88772C EEPROM offset 0x2D and 0x54 fields are used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus Spec Rev 2.0 for the detailed description of the "bMaxPower" field of Standard Configuration Descriptor. These fields are used to define the Maximum power consumption of the USB device drawn from the USB bus in this specific configuration when the device is fully operational. Expressed in 2mA units (for example, 0x64 indicates for 200mA).

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
8	*bMaxPower*	1	mA	Maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. The USB System Software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

4.2.2 External EEPROM Description

User can assign the specific VID/PID, Serial Number, Manufacture String, Product String, etc. user defined fields by external EEPROM. Please refer to **AX88772C EEPROM User Guide** document for more details about how to configure AX88772C EEPROM content.

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5 USB Configuration Structure

5.1 USB Configuration

The AX88772C supports 1 Configuration only.

5.2 USB Interface

The AX88772C supports 1 interface.

5.3 USB Endpoints

The AX88772C supports following 4 endpoints:

- Endpoint 0: Control endpoint. It is used for configuring the device.
- Endpoint 1: Interrupt endpoint. It is used for reporting status.
- Endpoint 2: Bulk In endpoint. It is used for receiving Ethernet Packet.
- Endpoint 3: Bulk Out endpoint. It is used for transmitting Ethernet Packet.

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6 Electrical Specifications

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
VCCK	Digital core power supply	- 0.3 to 2.16	V
VCC18A	Analog Power. 1.8V	- 0.3 to 2.16	V
VCC3IO	Power supply of 3.3V I/O	- 0.3 to 4	V
VCC3R3	Power supply of on-chip voltage regulator	- 0.3 to 4	V
VCC3A3	Analog Power 3.3V for Ethernet PHY bandgap	- 0.3 to 3.8	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	- 0.3 to 4	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	- 0.3 to 4	V
V_{IN18}	Input voltage of 1.8V I/O	- 0.3 to 2.16	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.3 to 4.0	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.3 to 5.8	V
T_{STG}	Storage temperature	- 65 to 150	℃
I_{IN}	DC input current	50	mA
I_{OUT}	Output short circuit current	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

6.1.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCC3R3	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	2.97	3.3	3.63	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	2.97	3.3	3.63	V
VCC3A3	Analog power supply for bandgap	2.97	3.3	3.63	V
T_j	Junction operating temperature	0	25	125	℃
T_a	Commerical ambient operating temperature in still air	0	-	70	℃

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6.1.3 Leakage Current and Capacitance

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{IN}	True 3.3V I/O input leakage current	Vin=3.3V or 0V	-	<±1	-	µA
	3.3V with 5V tolerance I/O input leakage current	Vin=5V or 0V	-	<±1	-	µA
C_{IN}	Input capacitance	3.3V I/O cells	-	2.3	-	pF
		3.3V with 5V tolerance I/O cells	-	4	-	pF
C_{OUT}	Output capacitance		-	2.2	-	pF
C_{BID}	Bi-directional buffer capacitance		-	2.2	-	pF

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding a pad capacitance of about 0.5pF to the package capacitance.

6.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.15	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.65	2.0	V
Vol	Output low voltage	|Iol| = 2 mA ~ 16 mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 2 mA ~ 16 mA	2.4	-	-	V
Rpu	Input pull-up resistance	PU = VCC3IO, PD = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	PU = 0V, PD = VCC3IO	40	75	190	KΩ

6.1.5 DC Characteristics of 3.3V with 5V Tolerance I/O Pins

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.15	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.65	2.0	V
Vol	Output low voltage	|Iol| = 2 mA ~ 16 mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 2 mA ~ 16 mA	2.4	-	-	V
Vopu[1]	Output pull-up voltage for 5V tolerance I/O cells	PU = VCC3IO, PD = 0V, E = 0, |Ipu| =1 μ A	VCC3IO-0.9	-	-	V
Rpu	Input pull-up resistance	PU = VCC3IO, PD = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	PU = 0V, PD = VCC3IO	40	75	190	KΩ

[1] This parameter indicates that the pull-up resistor for the 5V tolerance I/O cells cannot reach the VCC3IO DC level even without the DC loading current.

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6.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3R3	Power supply of on-chip voltage regulator.		3.0	3.3	3.6	V
Tj	Operating junction temperature.		0	25	125	℃
Iload	Driving current.	Normal operation	-	-	150	mA
V18F	Output voltage of on-chip voltage regulator.	VCC3R3 = 3.3V	1.71	1.8	1.89	V
Vdrop	Dropout voltage.	△V18F = -1%, Iload = 10mA	-	-	0.2	V
$\frac{\triangle V18F}{(\triangle VCC3R3 \times V18F)}$	Line regulation.	VCC3R3 = 3.3V, Iload = 10mA	-	0.2	0.4	%/V
$\frac{\triangle V18F}{(\triangle Iload \times V18F)}$	Load regulation.	VCC3R3 = 3.3V, 1mA ≦ Iload ≦ 150mA	-	0.02	0.05	%/mA
$\frac{\triangle V18F}{\triangle Tj}$	Temperature coefficient.	VCC3R3 = 3.3V,0℃ ≦ Tj ≦ 125℃	-	0.4	-	mV/℃
Iq_25℃	Quiescent current at 25 ℃	VCC3R3 = 3.3V, Iload = 0mA, Tj = 25 ℃	-	66	96	μA
Iq_125℃	Quiescent current at 125 ℃	VCC3R3 = 3.3V, Iload = 0mA, Tj = 125 ℃	-	85	115	μA
Cout	Output external capacitor.		3.3	-	-	μF
ESR	Allowable effective series resistance of external capacitor.		0.5	-	-	Ω

6.1.7 DC Characteristics of Fiber Interface

Fiber Transmitter Specification						
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Vol	Output low voltage		1.2	1.57	1.95	V
Voh	Output high voltage		2.0	2.4	2.7	V
|Vod|	Differential output voltage		0.54	0.83	1.15	V
Vol(od)	Output low voltage (overdrive)		1.1	1.5	1.85	V
Voh(od)	Output high voltage (overdrive)		2.2	2.5	2.8	V
|Vod|(od)	Differential output voltage (overdrive)		0.65	1.02	1.4	V
Fiber Receiver Specification						
Vicm	Input commond-mode voltage range		1.67	2.0	2.33	V
|Vidth|	Input differential threshold voltage		50	-	-	mV

Fiber SD (Signal Detect) Input Voltage Specification	
SD input voltage (Visd)	**Operation mode**
Visd < 0.2V	Copper mode
1.0V < Visd < 1.8V	Fiber mode No signal detected
Visd > 2.2V	Fiber mode Signal detected

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6.2 Thermal Characteristics

Description	Symbol	Rating	Units
Thermal resistance of junction to case	Θ_{JC}	16.7	℃/W
Thermal resistance of junction to ambient	Θ_{JA}	52.2	℃/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P},\ \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature T_A: ambient or environment temperature
T_C: the top center of compound surface temperature P: input power (watts)

6.3 Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 100Mbps full duplex mode and USB High speed mode	-	75.5	-	mA
IVCC33	Current Consumption of 3.3V		-	32.0	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 100Mbps full duplex mode and USB Full speed mode	-	70.6	-	mA
IVCC33	Current Consumption of 3.3V		-	26.1	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 10Mbps full duplex mode and USB High speed mode	-	20.5	-	mA
IVCC33	Current Consumption of 3.3V		-	30.5	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 10Mbps full duplex mode and USB Full speed mode	-	15.7	-	mA
IVCC33	Current Consumption of 3.3V		-	25.7	-	mA
IVCC18	Current Consumption of 1.8V	Ethernet unlink (Disable AutoDetach)	-	15.5	-	mA
IVCC33	Current Consumption of 3.3V		-	19.0	-	mA
IVCC18	Current Consumption of 1.8V	Ethernet unlink (Enable AutoDetach)	-	2.3	-	mA
IVCC33	Current Consumption of 3.3V		-	4.5	-	mA
IVCC18	Current Consumption of 1.8V	Suspend and enable Remote WakeUp and disable WOLLP (WOL Low Power)	-	62.7	-	mA
IVCC33	Current Consumption of 3.3V		-	12.7	-	mA
IVCC18	Current Consumption of 1.8V	Suspend and enable Remote WakeUp and enable WOLLP (WOL Low Power)	-	7.5	-	mA
IVCC33	Current Consumption of 3.3V		-	9.9	-	mA
IVCC18	Current Consumption of 1.8V	Suspend and disable Remote WakeUp	-	20	-	µA
IVCC33	Current Consumption of 3.3V		-	165	-	µA
IVCC18	Current Consumption of 1.8V	Operating at Rev-RMII PHY mode, Ethernet 100Mbps full duplex mode and USB High speed mode (Embedded PHY is powered down)	-	21.5	-	mA
IVCC33	Current Consumption of 3.3V		-	33.3	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Rev-RMII PHY mode, Ethernet 100Mbps full duplex mode and USB Full speed mode (Embedded PHY is powered down)	-	16.0	-	mA
IVCC33	Current Consumption of 3.3V		-	27.4	-	mA
I_{DEVICE}	Power consumption of AX88772C full loading (chip only)	1.8V	-	75.5	-	mA
		3.3V	-	32.0	-	mA
I_{SYSTEM}	Power consumption of AX88772C full loading (demo board)	Total of 3.3V (Including VCC3R3 regulator supplies 1.8V to VCCK and VCC18A)	-	168	-	mA

Table 8 : Power consumption

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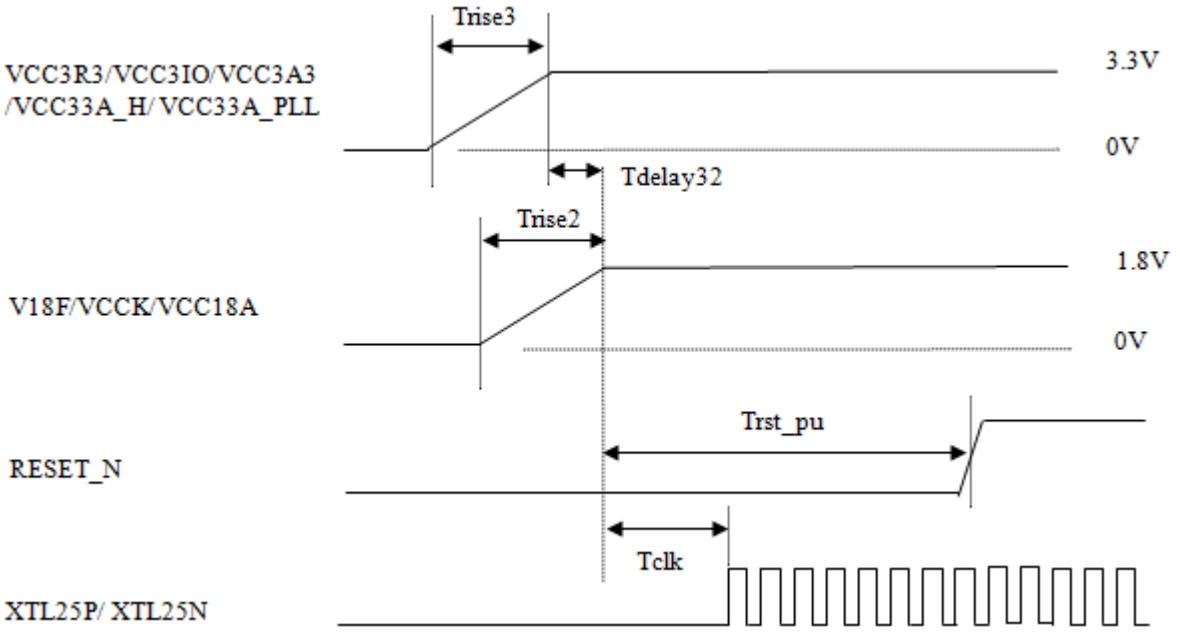
6.4 Power-up Sequence

At power-up, the AX88772C requires the VCC3R3/VCC3IO/VCC3A3/VCC33A_H/ VCC33A_PLL power supply to rise to nominal operating voltage within Trise3 and the V18F/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.



Symbol	Description	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	0.4	-	10	ms
T_{rise2}	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.8V rise time delay		-5	-	5	ms
T_{clk}	25MHz crystal oscillator start-up time	From VCC18A = 1.8V to first clock transition of XTALIN or XTALOUT	-	1	-	ms
T_{rst_pu}	RSTn low level interval time from power-up	From VCCK/VCC18A = 1.8V and VCC3IO = 3.3V to RSTn going high	T_{clk} + Trst *1	-	-	ms

*1 : Please refer to 1.09.16.5.2 Reset Timing for the details about the Trst.

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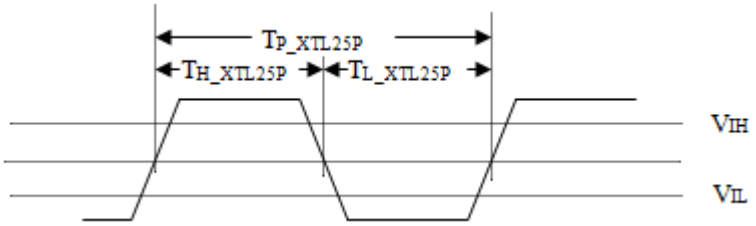
6.5 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on C_L (Output load) =50pF.

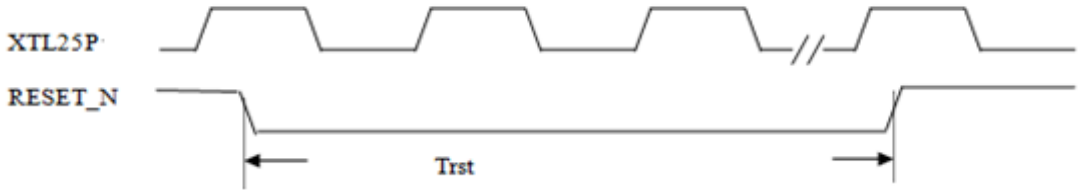
6.5.1 Clock Timing

XTL25P



Symbol	Description	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTL25P clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTL25P clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTL25P clock low time		-	20.0	-	ns

6.5.2 Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTL25P is running	125	-	250000	XTL25P clock cycle (Note)

Note: If the system applications require using hardware reset pin, RESET_N, to reset AX88772C during device initialization or normal operation after VBUS pin is asserted, the above timing spec (Min=5 μs, Max=10ms) of RESET_N should be met.

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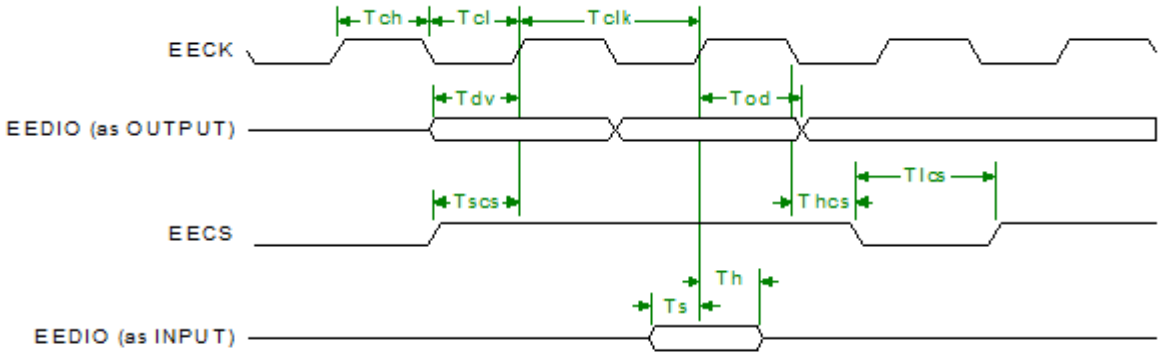
6.5.3 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

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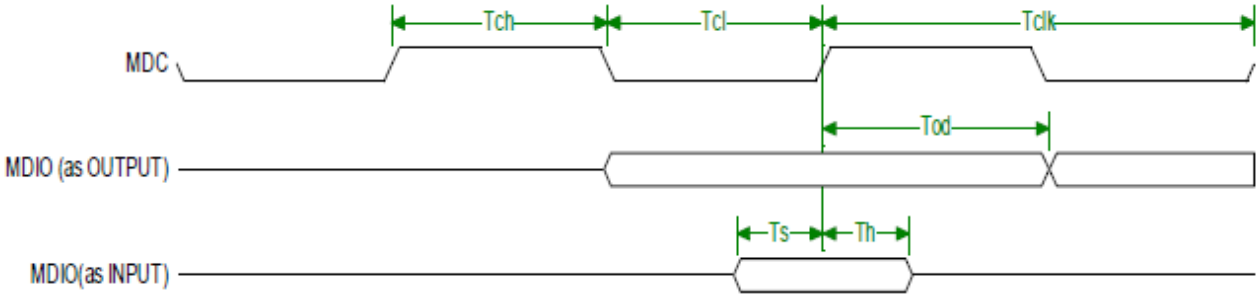
6.5.4 Station Management Timing



MAC mode with RMII: MDC=Output

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	640	-	ns
Tch	MDC clock high time	-	320	-	ns
Tcl	MDC clock low time	-	320	-	ns
Tod	MDC clock rising edge to MDIO output delay	0.5	-	-	Tclk
Ts	MDIO data input setup time	125	-	-	ns
Th	MDIO data input hold time	0	-	-	ns

PHY mode (Reverse-RMII): MDC=Input

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	320	-	ns
Tch	MDC clock high time	-	160	-	ns
Tcl	MDC clock low time	-	160	-	ns
Tod	MDC clock rising edge to MDIO output delay	0	-	300	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	10	-	-	ns

Note: MDC is Pin#17, MDIO is Pin#18.

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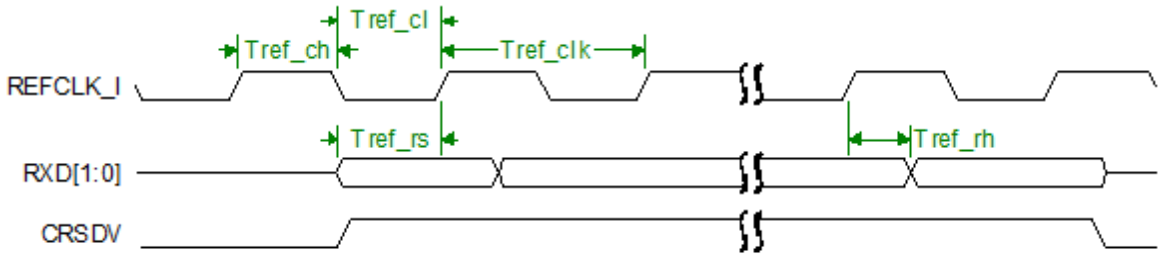
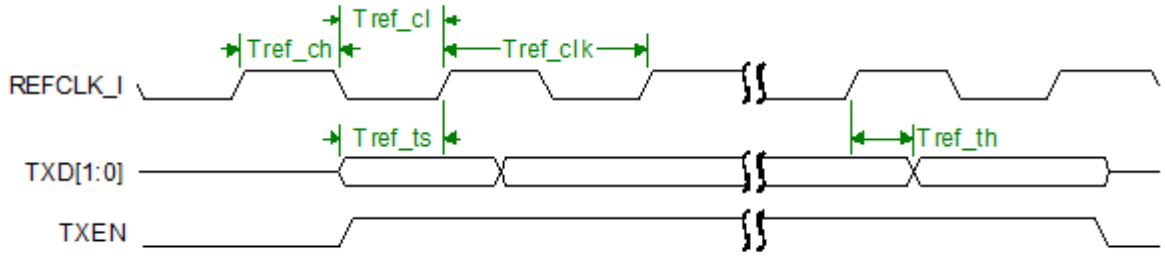
6.5.5 RMII / Reverse-RMII Timing



Symbol	Description	Min	Typ	Max	Unit
Tref_clk	Clock cycle time	-	20.0	-	ns
Tref_ch	Clock high time	-	10.0	-	ns
Tref_cl	Clock low time	-	10.0	-	ns
Tref_rs	RXD [1:0], CRSDV setup to rising REFCLK_I	4.0	-	-	ns
Tref_rh	RXD [1:0], CRSDV hold (delay time) from rising REFCLK_I	2.0	-	-	ns



Symbol	Description	Min	Typ	Max	Unit
Tref_ts	TXD [1:0], TXEN setup to rising REFCLK_I	4.0	-	-	ns
Tref_th	TXD [1:0], TXEN hold from rising REFCLK_I	2.0	-	-	ns

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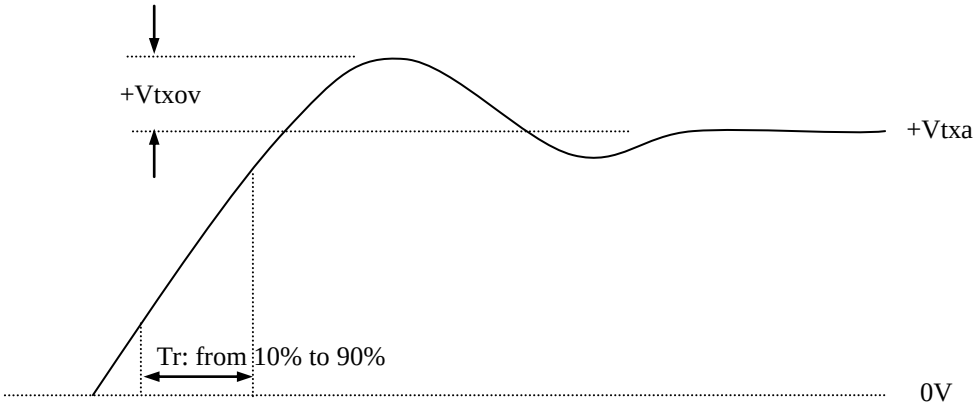
6.5.6 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

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6.5.7 USB Transceiver Interface Timing

VCC33A_H/ VCC33A_PLL= 3.0 ~ 3.6 V.

Static Characteristic for Analog I/O Pins (DP/DM):

Symbol	Description	Conditions	Min	Typ	Max	Unit
USB 2.0 Transceiver (HS)						
Input Levels (Differential Receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$ Measured at the connection as an application circuit.	300	-	-	mV
V_{HSCM}	High speed data signaling common mode voltage range		-50	-	500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected	-	-	100	mV
		No squelch detected	200	-	-	mV
Output levels (differential)						
V_{HSOI}	High speed idle level output voltage		-10	-	10	mV
V_{HSOL}	High speed low level output voltage		-10	-	10	mV
V_{HSOH}	High speed high level output voltage		-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage		700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage		-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	45	49.5	Ohm
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0	-	3.6	V
USB 1.1 Transceiver (FS/LS)						
Input Levels (Differential Receiver)						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$	0.2	-	-	V
V_{CM}	Differential common mode voltage		0.8	-	2.5	V
Input Levels (Single-Ended Receiver)						
V_{SE}	Single ended receiver threshold		0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage		0	-	0.3	V
V_{OH}	High-level output voltage		2.8	-	3.6	V

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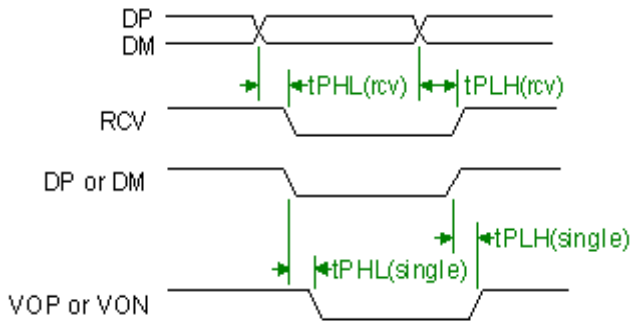
Dynamic Characteristic for Analog I/O Pins (DP/DM):

Symbol	Description	Conditions	Min	Typ	Max	Unit
Driver Characteristic						
High-Speed Mode						
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Full-Speed Mode						
t_{FR}	Rise time of DP/DM	C_L=50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L=50pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3	-	2.0	V
Driver Timing						
High-Speed Mode						
	Driver waveform requirement	See eye pattern of template 1	Follow template 1 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
	VI, FSE 0, OE to DP, DN Propagation delay	For detailed description of VI, FSE 0 and OE, please refer to USB rev 1.1specification.	-	-	15	ns
Receiver Timing						
High-Speed Mode						
	Data source jitter and receiver jitter tolerance	See eye pattern of template 4	Follow template 4 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
$t_{PLH(rcv)}$ $t_{PHL\ (rcv)}$	Receiver propagation delay (DP; DM to RCV)	For detailed description of RCV, please refer to USB rev 1.1specification.	-	-	15 (Note)	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)	-	-	-	15 (Note)	ns

Note: Full-Speed Timing diagram



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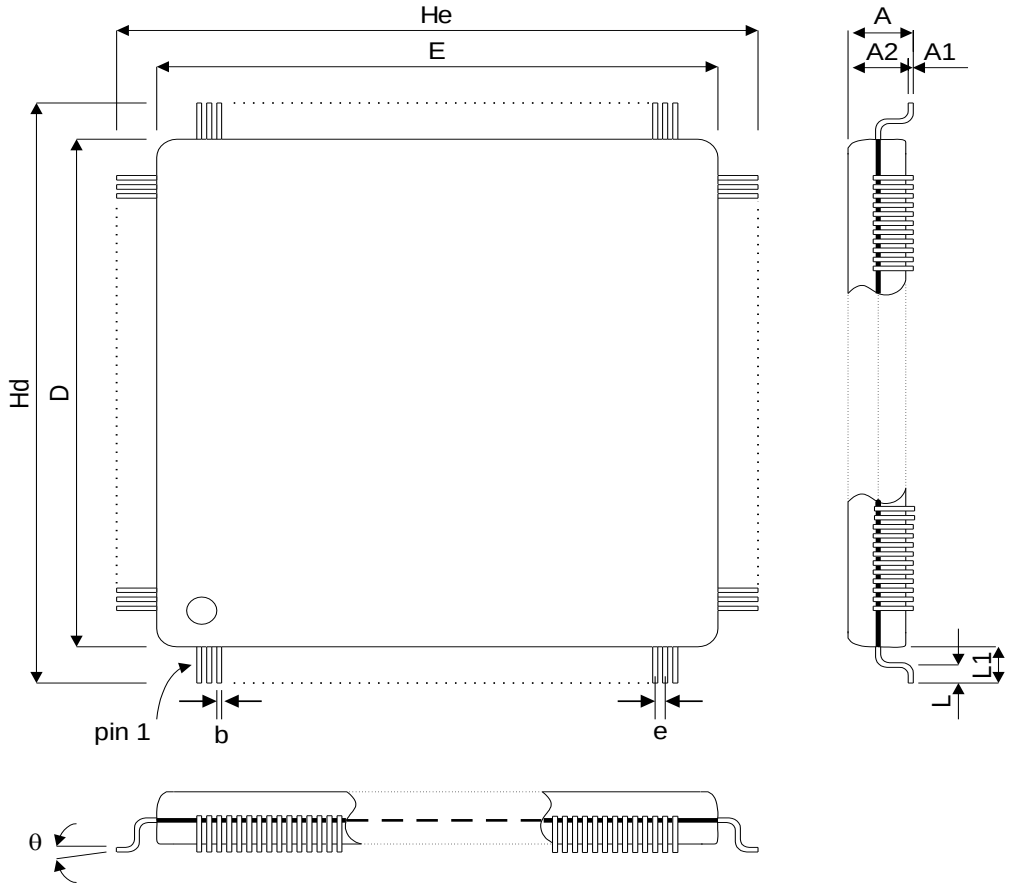
7 Package Information

7.1 AX88772C 64-pin LQFP package



Symbol	Millimeter		
	Min	Typ	Max
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A	-	-	1.60
b	0.13	0.18	0.23
D		7.00 BSC	
E		7.00 BSC	
e		0.40 BSC	
Hd		9.00 BSC	
He		9.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

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8 Ordering Information

Part Number	Description
AX88772CLF	64 PIN, LQFP Package, Commerical grade 0℃ to +70 ℃ (Green, Lead-Free)

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9 Revision History

Revision	Date	Comment
V0.10	2013/02/22	Preliminary release.
V0.20	2013/03/01	1. Modified the title string. 2. Modified some descriptions in Section 1.1, 2.1. 3. Updated the block diagram in Section 1.2. 4. Added the “DC Characteristics of Fiber Interface” information in Section 9.1.7.
V1.00	2013/05/03	1. Corrected a typo in the Title string. 2. Changed the “Node ID” wording to “MAC Address” in Section 4. 3. Modified some descriptions in Section 5. 4. Removed Section 6, 7, 8. 5. Added the Rev-RMII PHY power consumption in Section 6.3.
V1.01	2013/05/08	1. Modified the description in Title string. 2. Modified some descriptions in Section 1.1.
V1.10	2013/05/15	1. Modified some descriptions in the Features page and Section 3.11, 6.1.2, 6.1.6, 8.
V1.20	2014/05/14	1. Modified some descriptions in Section 7.
V1.30	2016/02/26	1. Modified some information in Section 6.1.
V1.31	2016/04/11	1. Modified some descriptions in Section 6.1.

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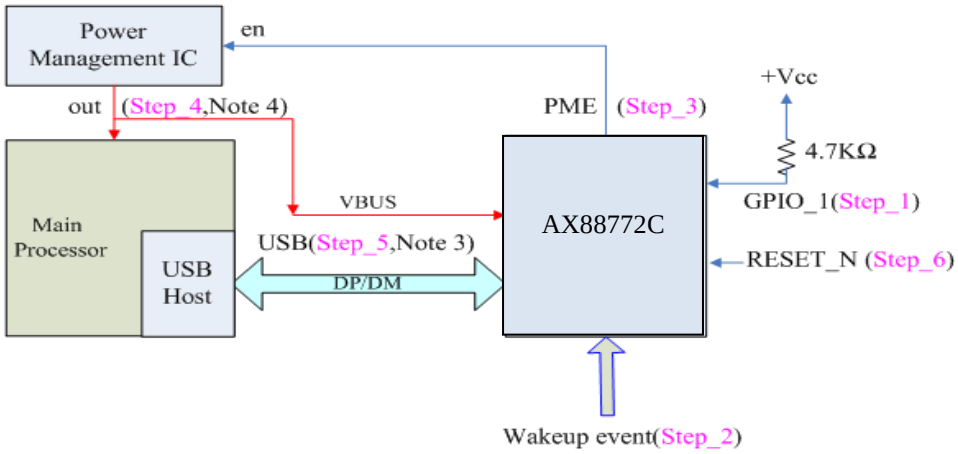
APPENDIX A. Default Wake-On-LAN (WOL) Ready Mode

This Default WOL Ready Mode application is different from normal operation where AX88772C Suspend/Resume state usually has to be configured by software driver during normal system operation. This application applies to a system that needs to use a predefined remote wakeup event to turn on the power supply of the system processor and its peripheral circuits without having any system software running in the beginning. This is quite useful when a system has been powered down already and a user needs to power on the system from a remote location.

The AX88772C can be configured to support Default WOL Ready Mode, where no system driver is required to configure its WOL related settings after power on reset. A system design usually partitions its power supply into two or more groups and the AX88772C is supplied with an independent power separated from the system processor. The power supply of AX88772C is usually available as soon as power plug is connected. The power supply of system processor remains off initially when power plug is connected and is controlled by AX88772C's PME pin, which can be activated whenever AX88772C detects a predefined wakeup event such as valid Magic Packet reception, Secondary PHY link-up, or the EXTWAKEUP_N pin trigger. To conserve power consumption, initially the USB host controller communicating with AX88772C can also be unpowered as the system processor.

The PME pin of AX88772C can control the power management IC to power up the system processor along with the USB host controller, which will perform USB transactions with AX88772C after both have been initialized. The pin polarity of PME is configured as high active when enabling Default WOL Ready Mode (see following **A.1** Note 2). Note that the AX88772C must be in self-power (via setting EEPROM Flag [0]) mode for this function.

A.1 Procedure to Enable Default WOL Ready Mode



To enable Default WOL Ready Mode, a user needs to configure GPIO_0 pin definition as PME (via setting EEPROM Flag [12]) and have GPIO_1 pulled-up with a 4.7Kohm resistor. After power on reset, AX88772C will disable most functions including USB transceiver (see Note 3) but enable Magic Packet detector logic and internal Ethernet PHY and its auto-negotiation function to be ready to receive Magic Packet. In PHY mode for AX88772C, Secondary PHY link-up can be a wakeup event (see Note 1).

When a valid Magic Packet is received, AX88772C will assert the PME pin to indicate to system processor the wakeup event. The PME pin, when being configured as static level output signal (via setting EEPROM Flag [15], see Note 2), can be used to control the power management IC to enable system power supply. After asserting the PME pin, AX88772C will also exit from the Default WOL Ready Mode and revert back to normal operation mode to start normal USB device detection, handshaking, and enumeration.

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The PME pin, when being configured as static level output signal, maintains its signal level until RESET_N is asserted again. If asserting RESET_N to AX88772C with GPIO_1 pulled-up, the Default WOL Ready Mode will be re-entered. Otherwise (GPIO_1 being pulled-down), the normal operation mode (non-Default WOL Ready Mode) will be entered and the normal USB device detection, handshaking and enumeration process should take place right after RESET_N negation.

Note 1: For complete truth table of wakeup events supported, please refer to below **Remote Wakeup Truth Table** on the "GPIO_1 = 1" setting.
Note 2: Please refer to 4.1.2 Flag. The bit [15:12] of Flag (PME_IND, PME_TYP, PME_POL, PME_PIN) = 0111.
Note 3: When the Default WOL Ready Mode is enabled, the DP/DM pins of AX88772C will be in tri-state.
Note 4: It is recommended that VBUS pin be connected to system power group directly. This way the V_BUS will become logic high when power management IC enables the system power supply.

Waken Up by	Setting						Wakeup Event						Device wakes up
	RWU bit of Flag byte in EEPROM	Set_Feature standard command	RWWF	RWMP	RWLC	GPIO_1 (*)	Host sends resume signal	Receiving a Wakeup Frame	Receiving a Magic Packet	Link status change detected On Primary PHY	Link status change detected On Secondary PHY	EXTWAKEUP_N pin	
USB Host	X	X	X	X	X	0	J → K						Yes
Device	0	0	X	X	X	0		X	X	X	X	X	No
Device	1	1	1	0	0	0		Yes					Yes
Device	1	1	0	1	0	0			Yes				Yes
Device	1	1	0	0	1	0				Yes			Yes
Device	1	1	0	0	1	0					Yes		Yes
Device	1	1	X	X	X	0						Low-pulse	Yes
Device	X	0	0	0	0	1			Yes		Yes	Low-pulse	Yes

*: About Default WOL Ready Mode, please refer to section 2.2 GPIO_1 Settings.

Table 9 : Remote Wakeup Truth Table

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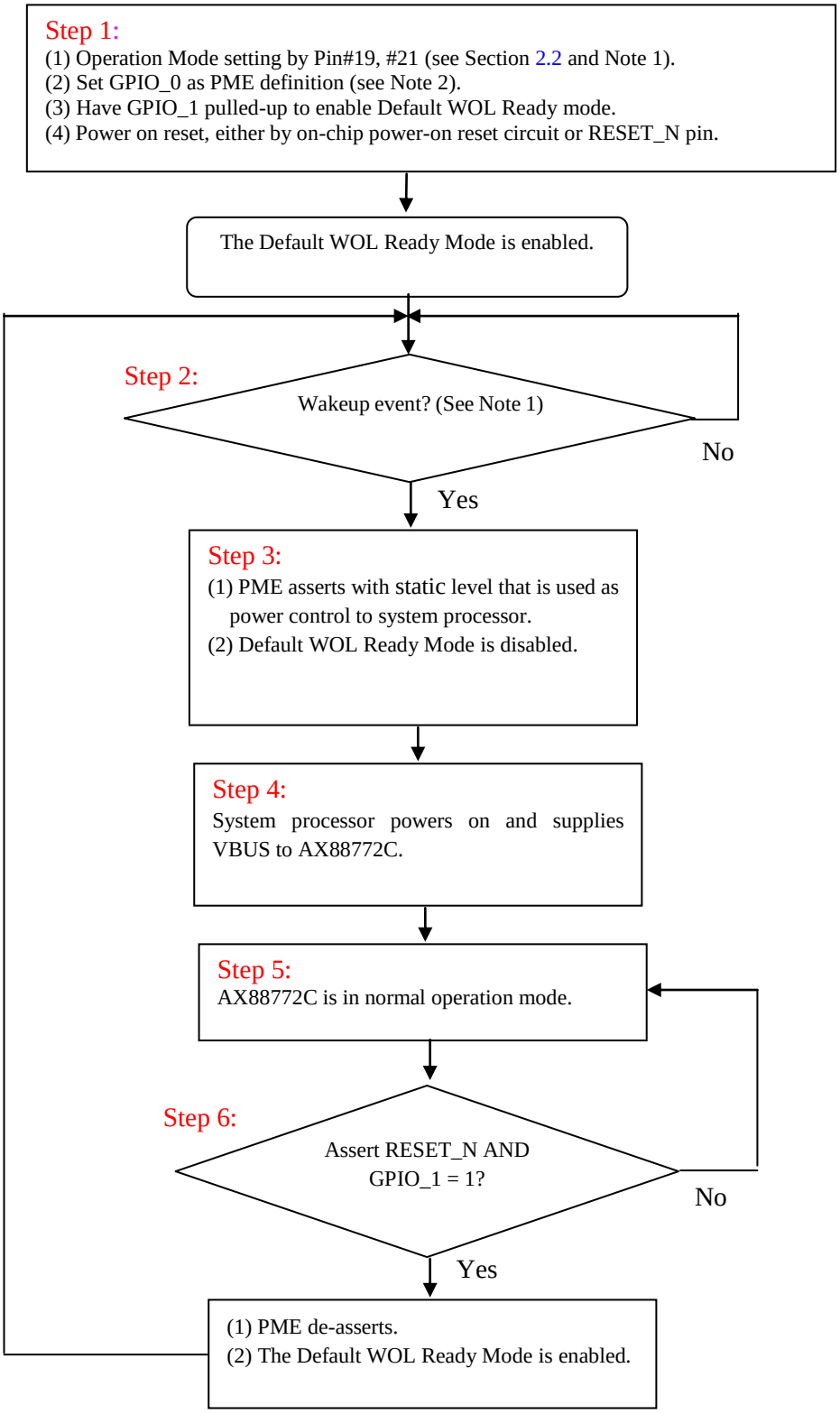
A.2 Flow Chart of Default WOL Ready Mode



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APPENDIX B. Ethernet PHY Power and Reset Control

This section indicates some information about AX88772C Ethernet PHY Power and Reset control.

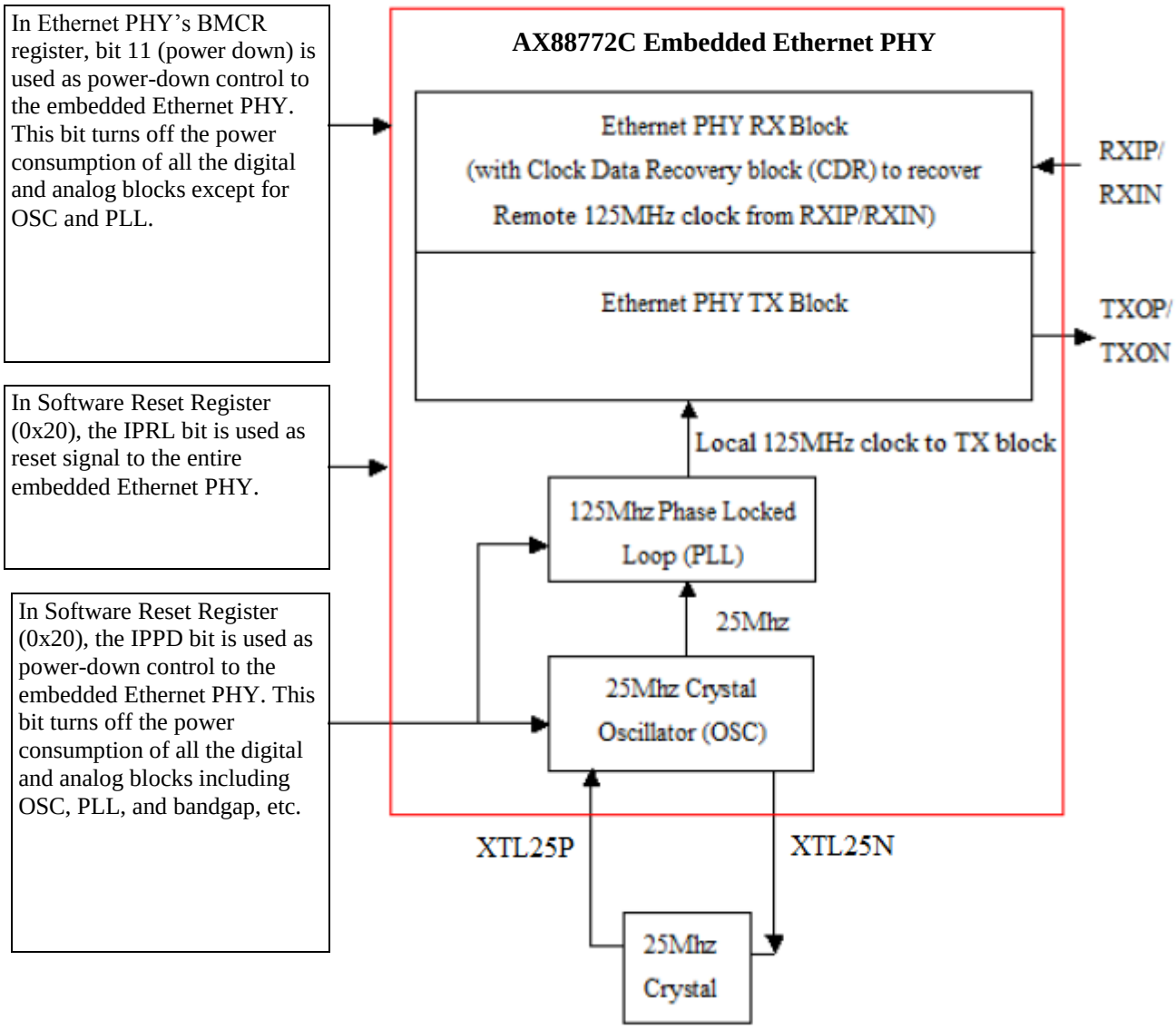

Figure 17 : Ethernet PHY Oscillator/PLL Block Diagram

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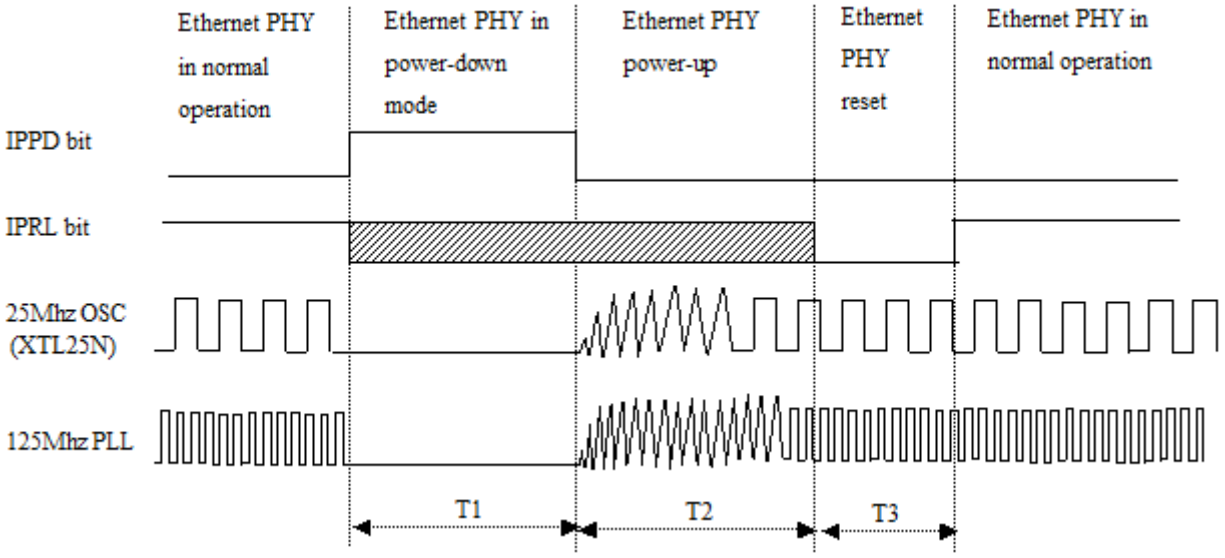
The following power-up and reset signal timing issued to the Ethernet PHY of AX88772C must be met in order to initialize the Ethernet PHY properly and reliably every time after it has been put into power-down mode previously.



Symbol	Description	Min	Typ	Max
T1	Ethernet PHY in power-down mode where the internal 25MHz OSC, 125MHz PLL and analog bandgap of AX88772C are completely turned off for max. power saving. This is the lowest power consumption mode of the Ethernet PHY. Note: Alternatively, user can use the Ethernet PHY's BMCR register bit 11, "power down", to set the Ethernet PHY into power-down mode. When the BMCR bit 11 power-down is used, the 25MHz OSC and 125MHz PLL will remain toggled but the analog bandgap will be turned off. The power consumption of BMCR bit 11 power-down mode is about 15mA more than the Software Reset Register (0x20) IPPD bit power-down mode.	500ns	-	-
T2	From Ethernet PHY power-up to 25MHz OSC and 125MHz PLL stable time. Note: If the IPRL is low during T2, it should be kept at low for more than T2 time so that the Ethernet PHY can be reset properly right after the power-up. In other words, the successful and reliable reset to the Ethernet PHY can only be accomplished with a stable running 25MHz OSC and 125MHz PLL clocks.	600ms	-	-
T3	Mandatory Ethernet PHY reset time after it has just been powered up from the previous power-down mode (after >T2 time). Also, software can issue reset to the Ethernet PHY during its non-power-down mode, but the minimum reset duration defined here must be met.	500ns	-	-

Figure 18 : Ethernet PHY Power-up & Reset Timing Diagram

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4F, No.8, Hsin Ann Rd., Hsinchu Science Park,
Hsinchu, Taiwan, R.O.C.

TEL: +886-3-5799500
FAX: +886-3-5799558

Email: support@asix.com.tw
Web: http://www.asix.com.tw