Document No: AX88782_783/V1.05/04/27/12

Features

- **High Performance Non-PCI Interface**
  - Configurable 8/16/32-bit SRAM-like host interface, easily interfaces with most common embedded MCUs (AX88782: 8/16-bit, AX88783: 8/16/32-bit)
  - Supports PPPoE/IPv4 IP/TCP/UDP/ICMP/ IGMP checksum offload to relieve CPU loading
  - Supports burst-mode access, minimizing CPU overhead
- **Fast Ethernet MAC + PHY**
  - IEEE 802.3 10Base-T/100Base-TX compatible
  - Supports Full Duplex operation with IEEE 802.3x flow control and Half Duplex with backpressure
  - 10/100M PHY supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Supports Wake-on-LAN by Microsoft Wakeup Frame, Magic Packet and link status change detection
- **Switching Fabric**
  - Performs non-blocking wire-speed forwarding and filtering
  - Embeds 32KB SRAM for packet buffering
  - Supports broadcast storm filtering
  - Supports per queue and per port ingress and egress programmable rate limit control
  - Integrates two-way Address-Lookup engine and table for 1K MAC addresses
  - Supports Routing Table/IGMP/VLAN Table access through CPU read/write operation
  - Supports 802.1D Spanning Tree Protocol and 802.1w Rapid Spanning Tree Protocol
- **QoS**
  - Supports Quality-of-Service for Port-Based, 802.1p VLAN and IPv4 TOS/IPv6 COS packets with four priority queues
  - Supports RFC2475 DiffServ-based
- **VLAN**
  - Supports up to 3 VLAN groups for port-based VLAN and 16 VLAN entries for 802.1Q tag-based VLAN functions
  - Supports the Double tagging 802.1Q-in-802.1Q Function for WAN access
- **Security**
  - Supports ingress port security mode, incoming packets with unknown source MAC address could be dropped
  - Supports eight Security MAC Registrations
  - Supports 802.1X port-based Authorization
- **Multicast**
  - Supports GMRP/GVRP/GARP packet snooping
  - Support IPv4 IGMP and IPv6 ICMP/MLD (Multicast Listener Discovery) Snooping
  - Supports up to 1K Multicast Group (shared with L2 MAC table)
  - Supports eight IGMP Multicast IP address snooping
- **Monitoring**
  - Supports RMON group 1, 2, 3 and 9 counter (RFC1213)
  - Supports Ethernet-like MIB counter (RFC 1643)
  - Supports Bridge MIB counter (RFC 1493)
  - Egress/Ingress Port Mirroring
  - Sniffer functions:
    - Source/Destination Port
    - DA/SA
    - VLAN ID
    - Ethernet Packet Type
    - IPv4/IPv6 Protocol
    - IPv4/IPv6 TCP/UDP Port Number
- **Optional Interfaces Supported:**
  - Optional serial EEPROM
  - MII or Reverse-MII (AX88783 only)
  - RMII or Reverse-RMII (AX88783 only)
  - Optional GPIO/GPI/GPO (AX88783 only)
- Single 3.3V power supply with options for 1.8V, 2.5V and 3.3V I/O voltage support
- Integrated an on-chip voltage regulator requiring only a single power supply of 3.3V
- Integrates an on-chip oscillator and PLL requiring only a 25MHz crystal to operate
- Integrates on-chip power-on reset circuit
- Small form factor: 80-pin E-PAD LQFP (AX88782) or 128-pin E-PAD LQFP (AX88783) RoHS compliant package
- Operating temperature range: 0˚C to 70˚C

Product Description

The AX88782/AX88783 is a non-PCI 2-port 10/100M Ethernet controller with an integrated 3-port switching fabric, three 10/100M MACs, two 10/100M PHYs, and an 8/16/32-bit SRAM-like host interface. This controller is targeted at embedded system applications that need to support two Ethernet ports, typically one for a LAN port and one for a WAN port. The AX88782/AX88783 supports simple a SRAM-like host interface, routine packet checksum calculation, and burst-mode access which make it easy to provide high performance 2-port Ethernet connectivity solutions for any embedded MCU. The built-in switching fabric supports non-blocking wire-speed forwarding and provides four priority

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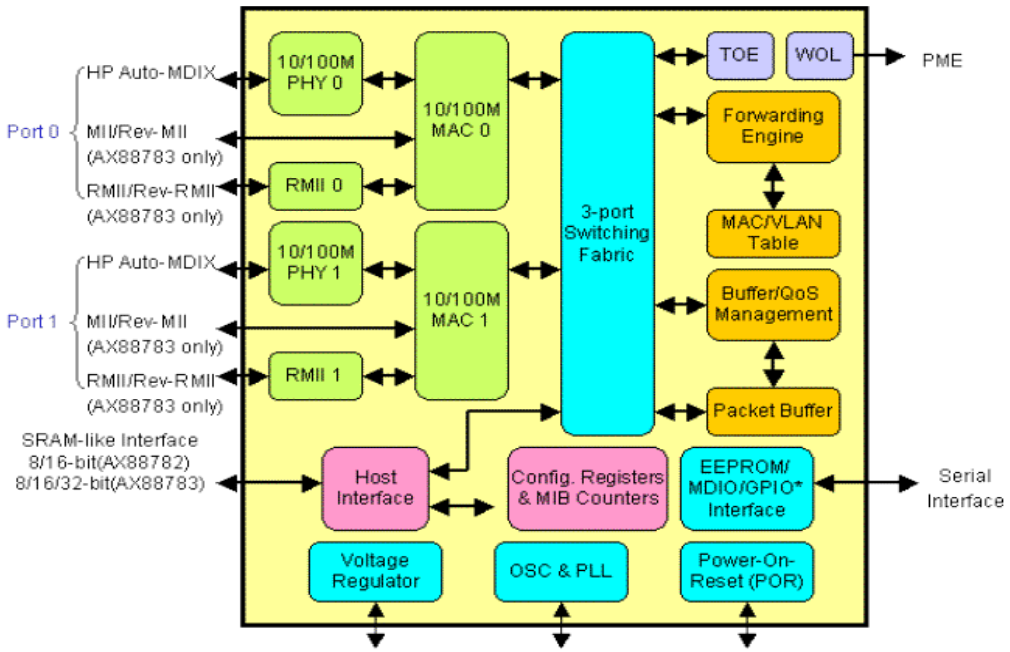
queues for advanced QoS functions including Port-Based, 802.1p VLAN, IPv4 TOS/IPv6 COS for voice, video, audio and data traffic classification. The AX88782/AX88783 combines the benefits of high integration and flexibility which makes it an ideal single-chip solution for designing high performance, QoS-aware, cost effective and small form factor 2-port Ethernet function for any embedded system application.

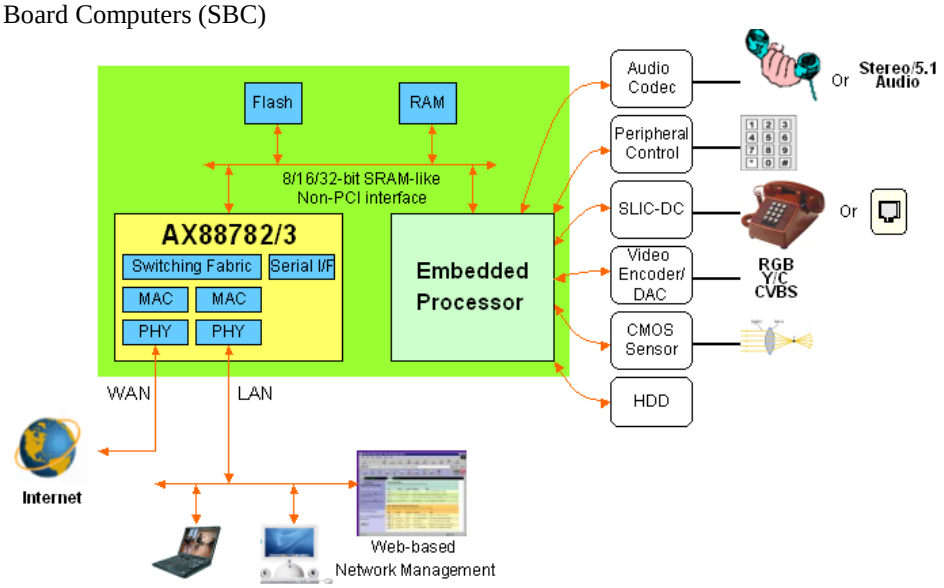
Block Diagram



*Optional GPIO Interface only for AX88783

Target Applications

- VoIP Phone, VoIP ATA Adapter
- IP Camera for Remote Surveillance
- Next Generation IP-STB and IPTV
- Industrial Controller and Networked Sensor
- Port Redundancy and Port Monitoring
- Single Board Computers (SBC)



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1.0 Overview

1.1 General Description

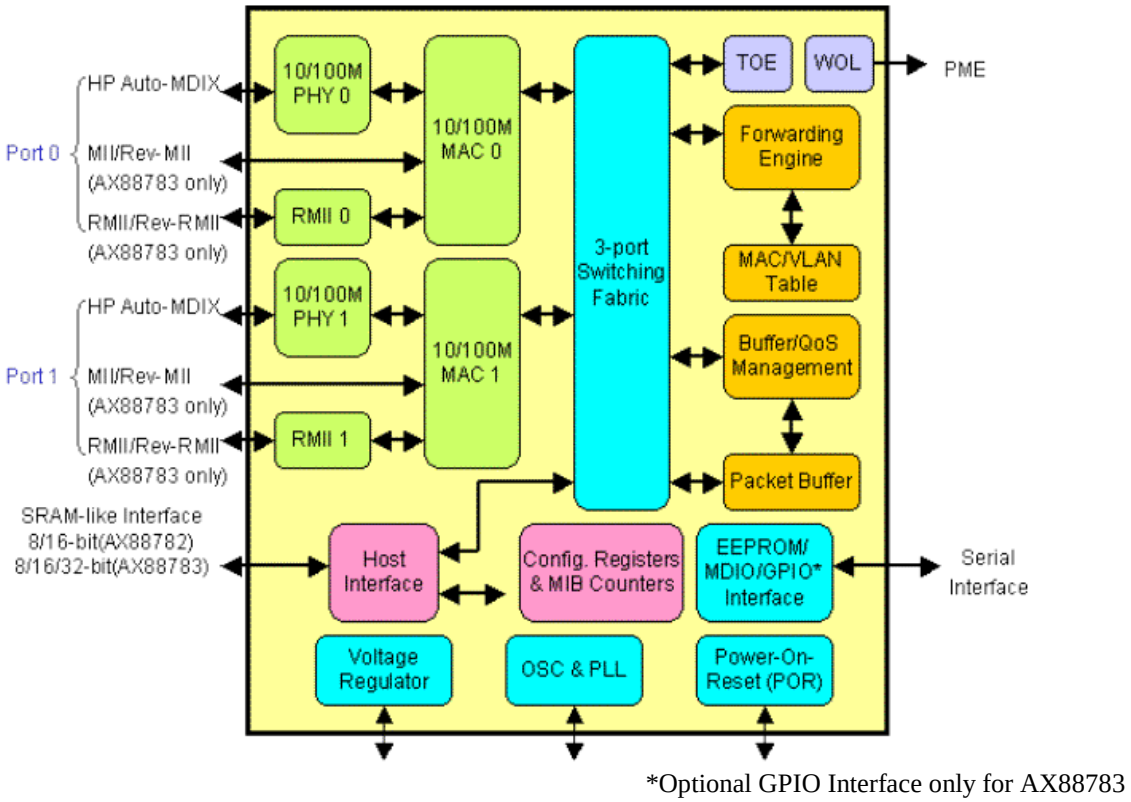
The AX88782/AX88783 is a non-PCI 2-port 10/100M Ethernet controller with an integrated 3-port switching fabric, three 10/100M MACs, two 10/100M PHYs, and the 8/16/32-bit SRAM-like host interface targeted for embedded system applications that need support of two Ethernet ports, typically one for LAN port and one for WAN port.

The AX88782/AX887833 supports the simple SRAM-like host interface, the routine packet checksum calculation, and the burst read and write access through host port which make it easy to provide 2-port Ethernet connectivity solutions for any embedded MCU with reasonable performance. The built-in switching fabric supports non-blocking wire-speed forwarding and provides four priority queues for advanced QoS functions including Port-Based, 802.1P VLAN, IPv4 TOS/IPv6 COS for voice, video, audio and data traffic classification. The AX88782/AX88783 combines the benefits of high integration and flexibility which makes it a ideal single-chip solution for designing high performance, QoS-aware, cost effective and small form factor 2-port Ethernet function for any embedded system applications.

The AX88782/AX88783 supports non-blocking wire speed forwarding rate and no Head-of-Line (HOL) blocking issue. The AX88782/AX88783 provides two flow-control mechanisms to avoid loss of data: an optional jamming-based backpressure flow control in the half-duplex operation and IEEE 802.3x in the full-duplex mode.

To support Quality of Service (QoS), each output port has four priority queues and their assignment can be based on the 802.1P priority field, TOS/COS/DiffServ field or Port-Pair setting. Each output port retrieves the Ethernet frames from the shared buffer based on queuing and sends them to the transmitting (Tx) FIFO.

1.2 Block Diagram



*Optional GPIO Interface only for AX88783

Fig 1 The AX88782/AX88783 Block Diagram

1.3 Pinout Diagram

1.3.1 AX88782: Port 0/Port 1 PHY Mode

Port 0: Built-in PHY
Port 1: Built-in PHY
Port 2: 8 / 16 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode

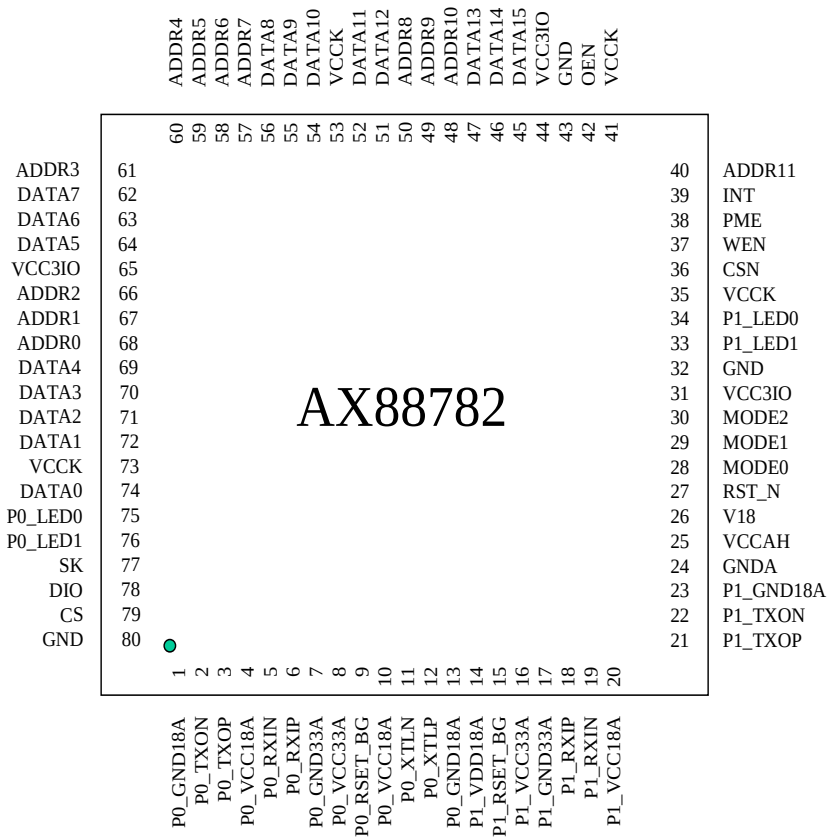


Fig 2 The AX88782 Default Pinout Diagram

1.3.2 AX88783 : Port 0/Port 1 PHY Mode

Port 0: Built-in PHY
Port 1: Built-in PHY
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

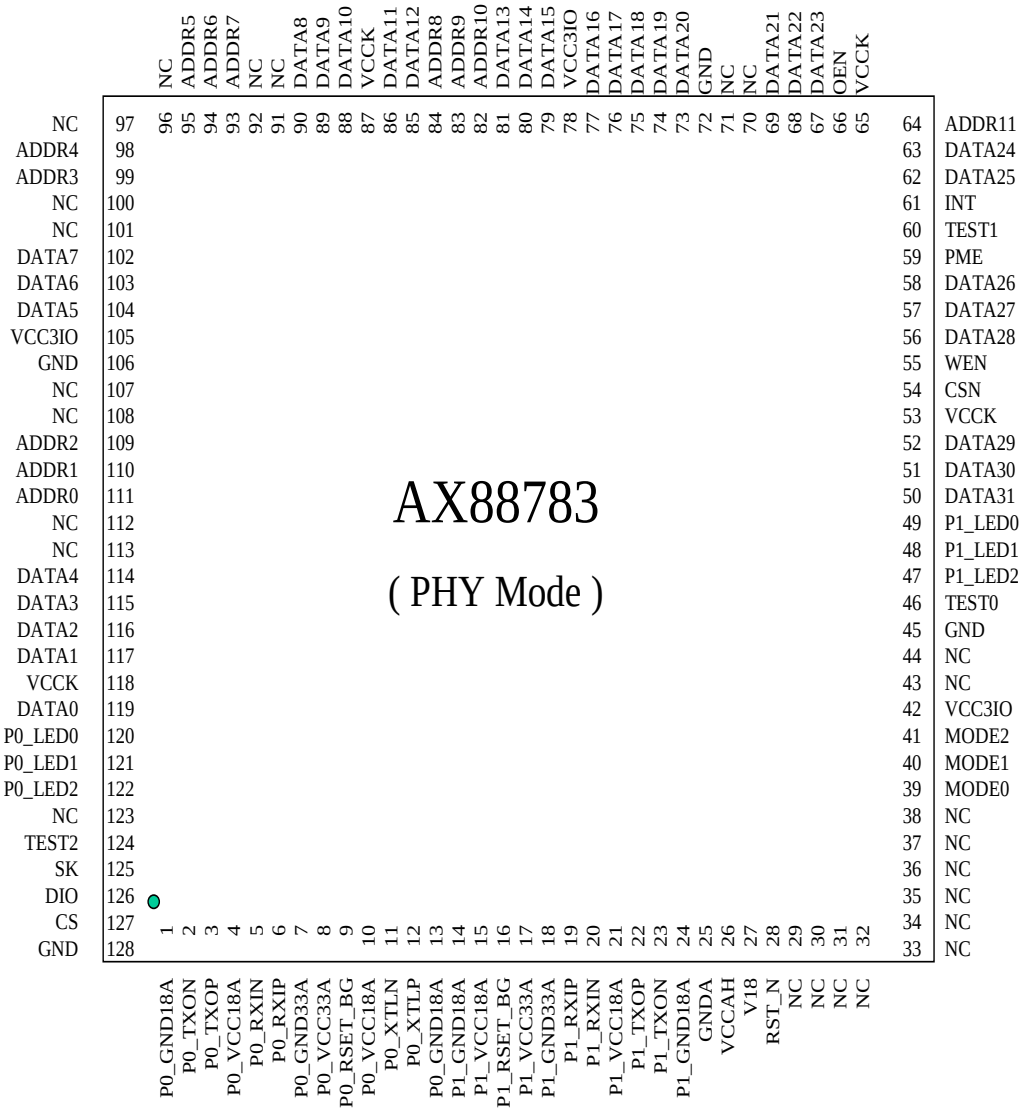


Fig 3 The AX88783 PHY Mode Pinout Diagram

1.3.3 AX88783 : Port 0/Port 1 MII Mode

Port 0 : MII Interface
Port 1 : MII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

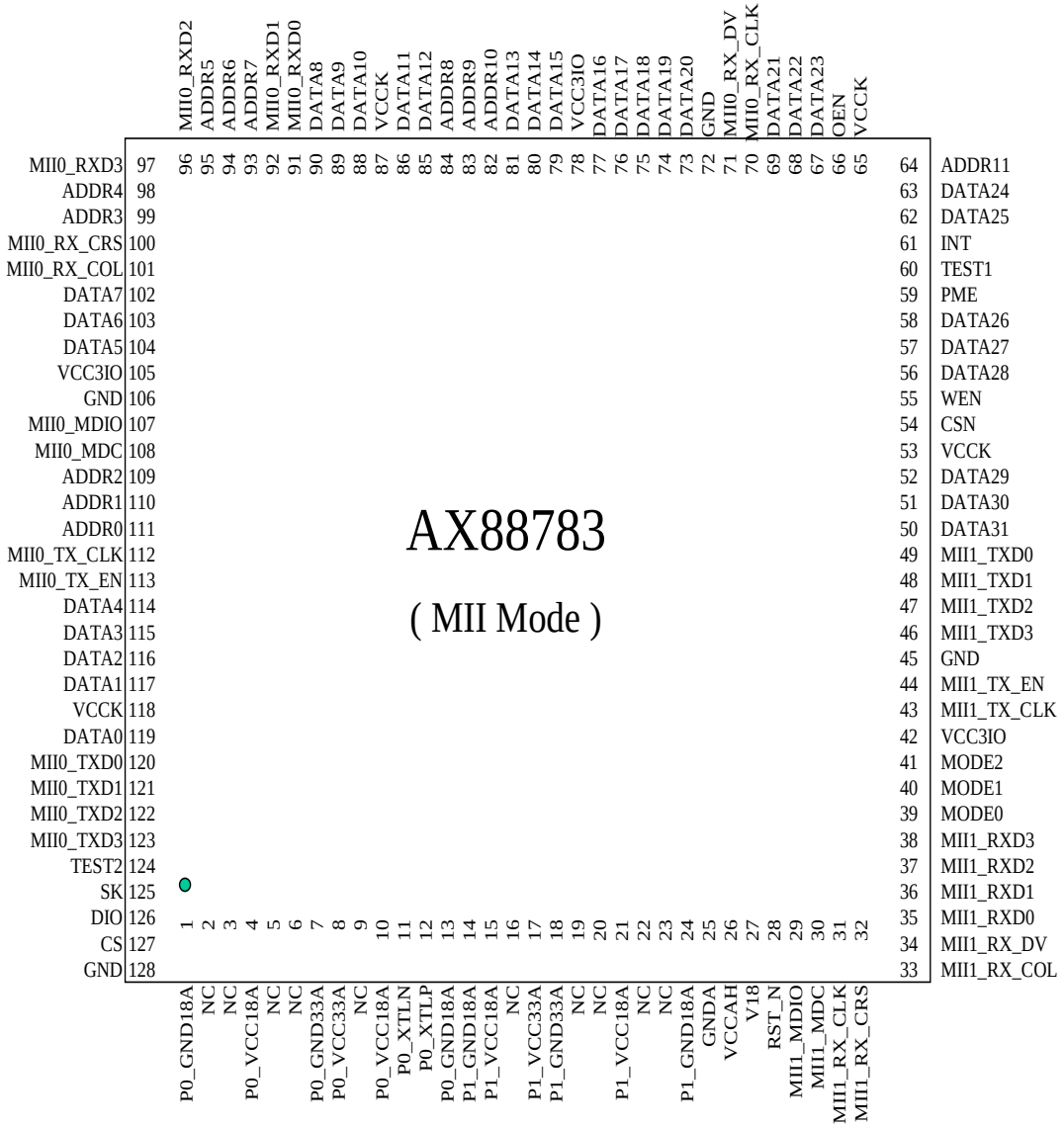


Fig 4 The AX88783 Port0/Port1 in MII Mode

1.3.4 AX88783: Port 0/Port 1 Reverse MII Mode

Port 0 : Reverse MII Interface
Port 1 : Reverse MII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

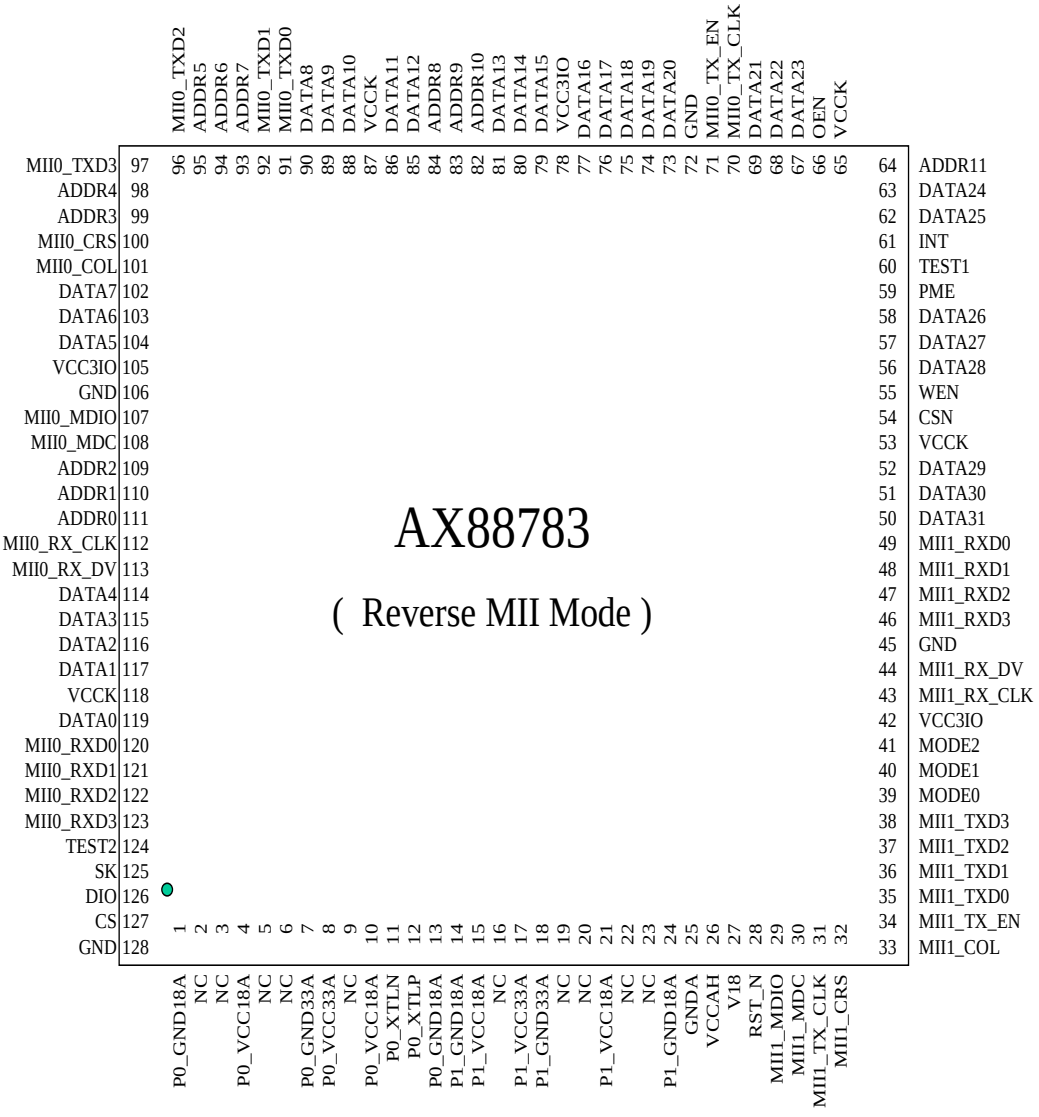


Fig 5 The AX88783 Port0/Port1 in Reverse MII Mode

1.3.5 AX88783: Port 0/Port 1 RMII Mode

Port 0 : RMII Interface
Port 1 : RMII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

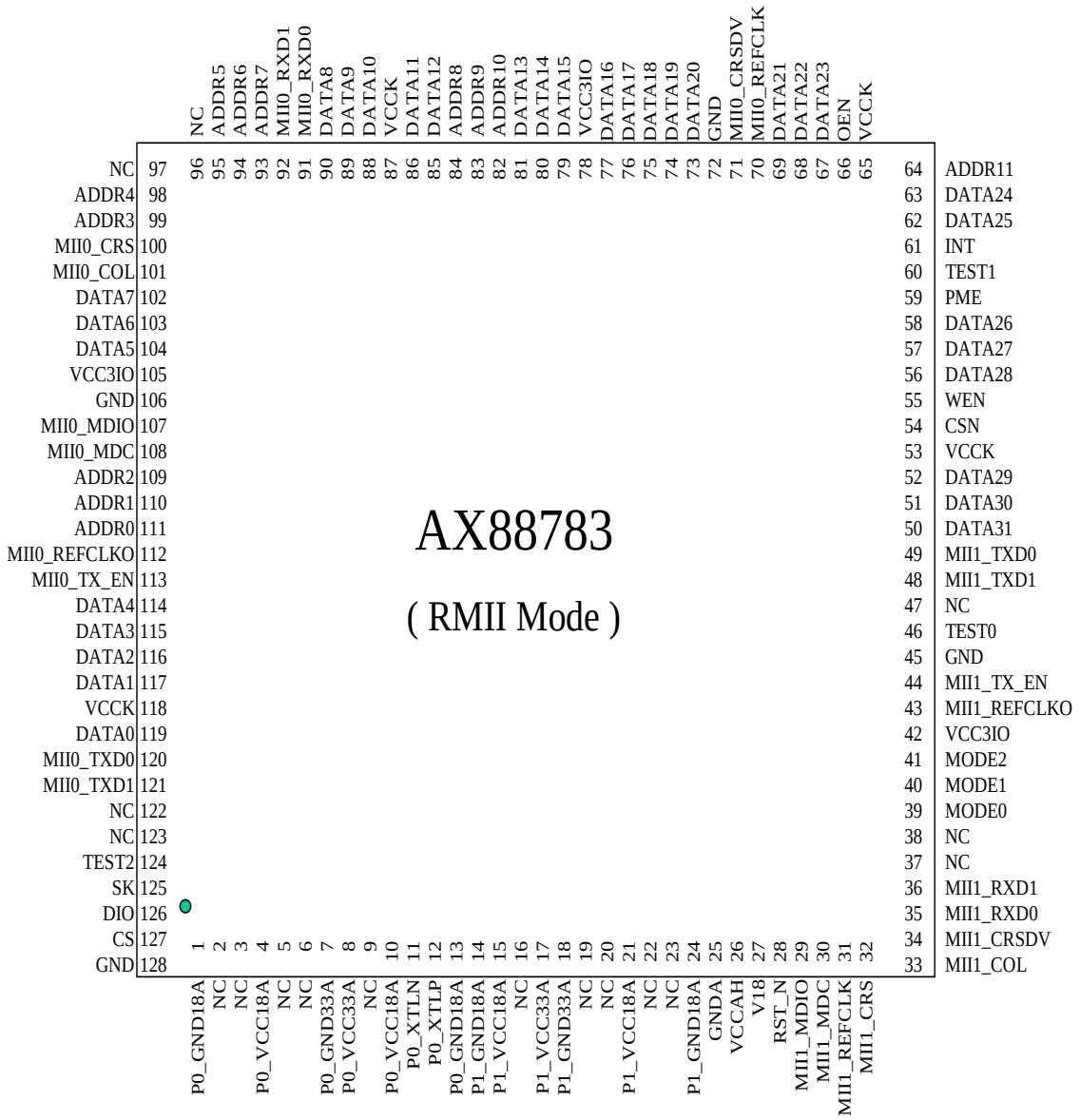


Fig 6 The AX88783 Port0/Port1 in RMII Mode

1.3.6 AX88783: Port 0/Port 1 Reverse RMII Mode

Port 0 : Reverse RMII Interface
Port 1 : Reverse RMII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

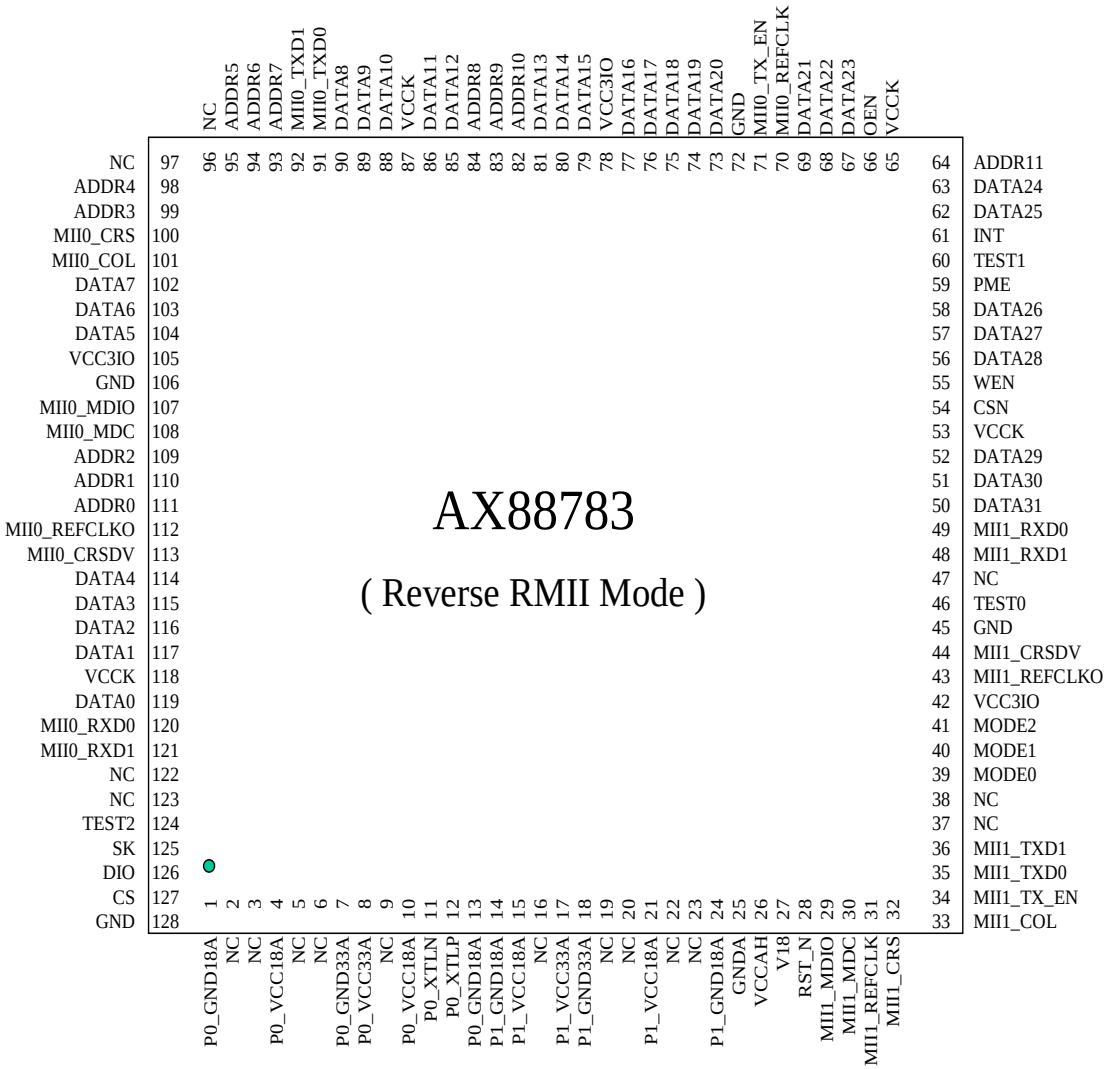


Fig 7 The AX88783 Port0/Port1 in Reverse RMII Mode

Note: The AX88783 also supports following mix-mode operations. Please refer to corresponding pin-out diagrams above. The AX88782 only support PHY mode with either 8 or 16-bit SRAM-like CPU interface.

Port 0	Port 1	Port 2
Built-in PHY	Built-in PHY	8-Bit Interface
MII Interface	MII Interface	16-Bit Interface
Reverse MII Interface	Reverse MII Interface	32-Bit Interface
RMII Interface	RMII Interface	
Reverse RMII Interface	Reverse RMII Interface	

2.0 Pin Descriptions

I/O Definition: The following terms describe the AX88782/AX88783 pin-out. The following abbreviations are used in following Tables.

I18	**Input 1.8V**	**PU**	**Pull Up**
I3	**Input 3.3V**	**PD**	**Pull Down**
O18	**Output 1.8V**	**P**	**Power Pin**
O3	**Output 3.3V**	**NC**	**No Connect**
B18	**Bi-directional 1.8V**	**OD**	**Open Drain**
B3	**Bi-directional 3.3V**	**T**	**Tri-state**
AB	**Analog Bi-directional**	**8mA**	**8 mA drive strength**
A	**Analog**	**16mA**	**16 mA drive strength**

2.1 Port 0 Interface

2.1.1 PHY Mode

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
P0_TXOP, P0_TXON	AB	3 2	3 2	Transmit Differential Data Pair for PHY0. The differential data is transmitted to the media on the TXOP/TXON signal pair in MDI mode or received differential data input positive pin in MDIX mode.
P0_RXIP, P0_RXIN	AB	6 5	6 5	Receive Differential Data Pair for PHY0. The differential data is received from the media on the RXIP/RXIN signal pair in MDI mode or transmitted differential data output negative pin in MDIX mode.
P0_XTLN,	I18	11	11	25Mhz ± 50 PPM crystal or oscillator clock input. A 25 MHz parallel-resonant crystal may be connected between these pins to stabilize the internal oscillator. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
P0_XTLP	O18	12	12	25MHz Crystal Feedback Output. This output is used in crystal connection only. It must be left open when P0_XTLN is driven with an external 25MHz oscillator.
P0_RSET_BG	AO	9	9	Off-chip resistor. Connect 12.1Kohm ± 1% resistor to ground.
P0_LED0	B3/8mA	75	120	Port 0 PHY LED 0 signal output. Please configure LCR [7:0] to select LED output function.
P0_LED1	B3/8mA	76	121	Port 0 PHY LED 1 signal output. Please configure LCR [15:8] to select LED output function.
P0_LED2	O3/8mA	N/A*	122	Port 0 PHY LED 2 signal output. Please configure LCR [23:16] to select LED output function.
P0_VCC18A	P/A	4, 10	4, 10	1.8V power supply for internal PHY Analog circuit
P0_VCC33A	P/A	8	8	3.3V power supply for internal PHY Analog circuit.
P0_GND18A	P/A	1, 13	1, 13	1.8V Ground for internal PHY Analog circuit
P0_GND33A	P/A	7	7	3.3V Ground for internal PHY Analog circuit.

* The AX88782 Only supports P0_LED0 and P0_LED1 LED output function.

2.1.2 MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_RX_CLK	I3	70	Port 0 Receive clock input
MII0_RX_COL	I3	101	Port 0 Receive collision signal. Collision signal is driven high by PHY when the collision is detected.
MII0_RX_CRS	I3	100	Port 0 Receive carrier sense. Carrier sense signal is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
MII0_RX_DV	I3	71	Port 0 Receive data valid. MII0_RX_DV is asserted high when valid data is present on receive data bus [3:0].
MII0_RXD0	I3	91	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD1	I3	92	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD2	I3	96	Port 0 Receive data bit 2 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD3	I3	97	Port 0 Receive data bit 3 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_TX_CLK	I3	112	Port 0 Transmit clock input
MII0_TX_EN	O3/8mA	113	Port 0 Transmit data enable. MII0_TX_EN is asserted high to indicate a valid transmit data bus [3:0]
MII0_TXD0	O3/8mA	120	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD1	O3/8mA	121	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD2	O3/8mA	122	Port 0 Transmit data bit 2 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD3	O3/8mA	123	Port 0 Transmit data bit 3 synchronously with respect to the rising edge of MII0_TX_CLK. Note: Pull-Down with a 4.7K ohm resistor to ground
MII0_MDIO	B3/8mA	107	MII management Data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	O3/8mA	108	MII management clock output to PHY. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. The frequency of MII0_MDC is 1MHz.

2.1.3 Reverse MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_TX_CLK	O3/8mA	70	Port 0 Transmit clock output
MII0_CRS	I3	100	Port 0 Carrier Sense. Please connect this signal to MII0_TX_EN enable signal.
MII0_COL	I3	101	Pull-Down with a 4.7KOhm resistor to ground. (Reverse MII mode only support full duplex mode)
MII0_TX_EN	I3	71	Port 0 Transmit data valid. MII0_TX_EN is asserted high when valid data is present on transmit data bus [3:0].
MII0_TXD0	I3	91	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD1	I3	92	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD2	I3	96	Port 0 Transmit data bit 2 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD3	I3	97	Port 0 Transmit data bit 3 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_RX_CLK	O3/8mA	112	Port 0 Transmit clock output
MII0_RX_DV	O3/8mA	113	Port 0 Receive data enable. MII0_RX_DV is asserted high to indicate a valid receive data bus [3:0]
MII0_RXD0	O3	120	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD1	O3	121	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD2	O3	122	Port 0 Receive data bit 2 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD3	O3/8mA	123	Port 0 Receive data bit 3 synchronously with respect to the rising edge of MII0_RX_CLK. Note: Pull-Down with a 4.7K ohm resistor to ground
MII0_MDIO	B3/8mA	107	MII management Data. Serial data input/output transferred from/to the external connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	I3	108	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. Note: P0SMR0 Slave MDIO Register need to be programmed.

2.1.4 RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_REFCLK	I3	70	Port 0 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII0_CRSDV	I3	71	Port 0 Receive data valid synchronously with respect to the rising edge of MII0_REFCLK. MII0_CRSDV is asserted high when valid data is present on receive data bus [1:0].
MII0_RXD0	I3	91	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_RXD1	I3	92	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_REFCLKO	O3/8mA	112	Port 0 50MHz reference clock output if ICR [12] is set to one.
MII0_TX_EN	O3/8mA	113	Port 0 Transmit data enable synchronously with respect to the rising edge of MII0_REFCLK. MII0_TX_EN is asserted high to indicate a valid transmit data bus [1:0]
MII0_TXD0	O3/8mA	120	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_TXD1	O3/8mA	121	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_MDIO	B3/8mA	107	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	O3/8mA	108	MII management clock output to PHY. All data transferred on MDIO are synchronized to the rising edge of this clock. The frequency of MII0_MDC is 1MHz.
MII0_CRS	I3	100	Pull-Down with a 4.7K ohm resistor to ground
MII0_COL	I3	101	Pull-Down with a 4.7K ohm resistor to ground

2.1.5 Reverse RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_REFCLK	I3	70	Port 0 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII0_TX_EN	I3	71	Port 0 Transmit data valid synchronously with respect to the rising edge of MII0_REFCLK. MII0_TX_EN is asserted high when valid data is present on transmit data bus [1:0].
MII0_TXD0	I3	91	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_TXD1	I3	92	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_REFCLKO	O3/8mA	112	Port 0 50 MHz Reference clock output if ICR [12] is set to one.
MII0_CRSDV	O3/8mA	113	Port 0 Receive data enable synchronously with respect to the rising edge of MII0_REFCLK. MII0_CRSDV is asserted high to indicate a valid receive data bus [1:0]
MII0_RXD0	O3/8mA	120	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_RXD1	O3/8mA	121	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_MDIO	B3/8mA	107	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	I3	108	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. Note: P0SMR0 Slave MDIO Register need to be programmed.
MII0_CRS	I3	100	Pull-Down with a 4.7K ohm resistor to ground
MII0_COL	I3	101	Pull-Down with a 4.7K ohm resistor to ground

2.1.6 GPIO Mode (AX88783)

Signal Name	I/O	AX88783 Pin No.	Description
GPIO0	B3	101	Generous Purpose IO Pin #0
GPIO1	B3	100	Generous Purpose IO Pin #1
GPIO2	B3	112	Generous Purpose IO Pin #2
GPIO3	B3	70	Generous Purpose IO Pin #3
GPIO4	B3	107	Generous Purpose IO Pin #4
GPIO5	B3	108	Generous Purpose IO Pin #5
GPI0	I3	91	Generous Purpose Input Pin #0
GPI1	I3	92	Generous Purpose Input Pin #1
GPI2	I3	96	Generous Purpose Input Pin #2
GPI3	I3	97	Generous Purpose Input Pin #3
GPI4	I3	71	Generous Purpose Input Pin #4
GPO	O3	113	Generous Purpose Output Pin

2.1.7 Port 0 Multi-Function Pin Summary

AX88783 Pin #	MII Mode	Reverse MII Mode	RMII Mode	Reverse RMII Mode	PHY Mode	GPIO Mode
70	MII0_RX_CLK	MII0_TX_CLK	MII0_REFCLK	MII0_REFCLK	NC	GPIO3
101	MII0_RX_COL	Pull-Down	Pull-Down	Pull-Down	NC	GPIO0
100	MII0_RX_CRS	MII0_CRS	Pull-Down	Pull-Down	NC	GPIO1
71	MII0_RX_DV	MII0_TX_EN	MII0_CRSDV	MII0_TX_EN	NC	GPI4
91	MII0_RXD0	MII0_TXD0	MII0_RXD0	MII0_TXD0	NC	GPI0
92	MII0_RXD1	MII0_TXD1	MII0_RXD1	MII0_TXD1	NC	GPI1
96	MII0_RXD2	MII0_TXD2	NC	NC	NC	GPI2
97	MII0_RXD3	MII0_TXD3	NC	NC	NC	GPI3
112	MII0_TX_CLK	MII0_RX_CLK	MII0_REFCLKO	MII0_REFCLKO	NC	GPIO2
113	MII0_TX_EN	MII0_RX_DV	MII0_TX_EN	MII0_CRSDV	NC	GPO
120	MII0_TXD0	MII0_RXD0	MII0_TXD0	MII0_RXD0	P0_LED0	
121	MII0_TXD1	MII0_RXD1	MII0_TXD1	MII0_RXD1	P0_LED1	
122	MII0_TXD2	MII0_RXD2	NC	NC	P0_LED2	
123	MII0_TXD3	MII0_RXD3	NC	NC	NC	
107	MII0_MDIO	MII0_MDIO	MII0_MDIO	MII0_MDIO	NC	GPIO4
108	MII0_MDC	MII0_MDC	MII0_MDC	MII0_MDC	NC	GPIO5

Note1: The AX88782 can only support PHY Mode
Note2: GPIO mode and PHY mode can active at the same time without any conflict.

2.2 Port 1 Interface

2.2.1 PHY Mode

Signal Name	I/O	Pin No. AX88782	Pin No. AX88783	Description
P1_TXOP, P1_TXON	AB AB	21 22	22 23	Transmit Differential Data Pair for PHY0. The differential data is transmitted to the media on the TXOP/TXON signal pair in MDI mode or received differential data input positive pin in MDIX mode.
P1_RXIP, P1_RXIN	AB AB	18 19	19 20	Receive Differential Data Pair for PHY0. The differential data is received from the media on the RXIP/RXIN signal pair in MDI mode or transmitted differential data input positive pin in MDIX mode.
P1_RSET_BG	AO	15	16	Off-chip resistor. Connect 12.1Kohm ± 1% resistor to ground.
P1_LED0	B3/8mA	34	49	Port 1 PHY LED 0 signal output. Please configure LCR [7:0] to select LED output function.
P1_LED1	B3/8mA	33	48	Port 1 PHY LED 1 signal output. Please configure LCR [15:8] to select LED output function.
P1_LED2	O3/8mA	N/A	47	Port 1 PHY LED 2 signal output. Please configure LCR [23:16] to select LED output function.
P1_VCC18A	P/A	14, 20	15, 21	1.8V power supply for internal PHY Analog circuit
P1_VCC33A	P/A	16	17	3.3V power supply for internal PHY Analog circuit.
P1_GND18A	P/A	23	14, 24	1.8V Ground for internal PHY Analog circuit
P1_GND33A	P/A	17	18	3.3V Ground for internal PHY Analog circuit.

2.2.2 MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_RX_CLK	I3	31	Port 1 Receive clock input
MII1_RX_COL	I3	33	Port 1 Receive collision signal. Collision signal is driven high by PHY when the collision is detected.
MII1_RX_CRS	I3	32	Port 1 Receive carrier sense. Carrier sense signal is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
MII1_RX_DV	I3	34	Port 1 Receive data valid. MII1_RX_DV is asserted high when valid data is present on receive data bus [3:0].
MII1_RXD0	I3	35	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD1	I3	36	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD2	I3	37	Port 1 Receive data bit 2 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD3	I3	38	Port 1 Receive data bit 3 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_TX_CLK	I3	43	Port 1 Transmit clock input
MII1_TX_EN	O3/8mA	44	Port 1 Transmit data enable. MII1_TX_EN is asserted high to indicate a valid transmit data bus [3:0]
MII1_TXD0	O3/8mA	49	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD1	O3/8mA	48	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD2	O3/8mA	47	Port 1 Transmit data bit 2 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD3	O3/8mA/PD	46	Port 1 Transmit data bit 3 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec. NOTE: If both Port 0 and Port 1 are set to MII Mode then please tie MDIO to MII0_MDIO and ignore this pin.
MII1_MDC	O3/8mA	30	MII management clock output to PHY. All data transferred on MII1_MDIO are synchronized to the rising edge of this clock. The frequency of MII1_MDC is 1MHz. NOTE: If both Port 0 and Port 1 are set to MII Mode then please tie MDC to MII0_MDC and ignore this pin.

2.2.3 Reverse MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_TX_CLK	O3/8mA	31	Port 1 Transmit clock output
MII1_CRS	I3	32	Port 1 Carrier Sense. Please connect this signal to MII1_TX_EN enable signal.
MII1_COL	I3	33	Pull-Down with a 4.7KOhm resistor to ground. Reverse MII mode only support full duplex.
MII1_TX_EN	I3	34	Port 1 Transmit data valid. MII1_TX_EN is asserted high when valid data is present on transmit data bus [3:0].
MII1_TXD0	I3	35	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD1	I3	36	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD2	I3	37	Port 1 Transmit data bit 2 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD3	I3	38	Port 1 Transmit data bit 3 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_RX_CLK	O3/8mA	43	Port 1 Receive clock output
MII1_RX_DV	O3/8mA	44	Port 1 Receive data enable. MII1_RX_DV is asserted high to indicate a valid receive data bus [3:0]
MII1_RXD0	O3/8mA	49	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD1	O3/8mA	48	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD2	O3/8mA	47	Port 1 Receive data bit 2 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD3	O3/8mA	46	Port 1 Receive data bit 3 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	I3	30	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock. Note: P1SMR0 Slave MDIO Register need to be programmed

2.2.4 RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_REFCLK	I3	31	Port 1 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII1_CRSDV	I3	34	Port 1 Receive data valid synchronously with respect to the rising edge of MII1_REFCLK. MII1_CRSDV is asserted high when valid data is present on receive data bus [1:0].
MII1_RXD0	I3	35	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_RXD1	I3	36	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_REFCLKO	O3/8mA	43	Port 1 50MHz clock output if ICR [13] is set to one.
MII1_TX_EN	O3/8mA	44	Port 1 Transmit data enable synchronously with respect to the rising edge of MII1_REFCLK. MII1_TX_EN is asserted high to indicate a valid transmit data bus [1:0]
MII1_TXD0	O3/8mA	49	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_TXD1	O3/8mA	48	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	O3/8mA	30	MII management clock output to PHY. All data transferred on MDIO are synchronized to the rising edge of this clock. The frequency of MDC is 1MHz.
MII1_CRS	I3	32	Pull-Down with a 4.7K ohm resistor to ground
MII1_COL	I3	33	Pull-Down with a 4.7K ohm resistor to ground

2.2.5 Reverse RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_REFCLK	I3	31	Port 1 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII1_TX_EN	I3	34	Port 1 Transmit data valid synchronously with respect to the rising edge of MII1_REFCLK. MII1_TX_EN is asserted high when valid data is present on transmit data bus [1:0].
MII1_TXD0	I3	35	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_TXD1	I3	36	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_REFCLKO	O3/8mA	43	Port 1 50MHz reference clock output if ICR [13] is set to one.
MII1_CRSDV	O3/8mA	44	Port 1 Receive data enable synchronously with respect to the rising edge of MII1_REFCLK. MII1_CRSDV is asserted high to indicate a valid receive data bus [1:0]
MII1_RXD0	O3/8mA	49	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_RXD1	O3/8mA	48	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	I3	30	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock. Note: P1SMR0 Slave MDIO Register need to be programmed
MII1_CRS	I3	32	Pull-Down with a 4.7K ohm resistor to ground
MII1_COL	I3	33	Pull-Down with a 4.7K ohm resistor to ground

2.2.6 Port 1 Multi-Function Pin Summary

AX88783 Pin #	MII Mode	Reverse MII Mode	RMII Mode	Reverse RMII Mode	PHY Mode
31	MII1_RX_CLK	MII1_TX_CLK	MII1_REFCLK	MII1_REFCLK	NC
33	MII1_RX_COL	Pull-Down	Pull-Down	Pull-Down	NC
32	MII1_RX_CRS	MII1_CRS	Pull-Down	Pull-Down	NC
34	MII1_RX_DV	MII1_TX_EN	MII1_CRSDV	MII1_TX_EN	NC
35	MII1_RXD0	MII1_TXD0	MII1_RXD0	MII1_TXD0	NC
36	MII1_RXD1	MII1_TXD1	MII1_RXD1	MII1_TXD1	NC
37	MII1_RXD2	MII1_TXD2	NC	NC	NC
38	MII1_RXD3	MII1_TXD3	NC	NC	NC
43	MII1_TX_CLK	MII1_RX_CLK	MII1_REFCLKO	MII1_REFCLKO	NC
44	MII1_TX_EN	MII1_RX_DV	MII1_TX_EN	MII1_CRSDV	NC
49	MII1_TXD0	MII1_RXD0	MII1_TXD0	MII1_RXD0	P1_LED0
48	MII1_TXD1	MII1_RXD1	MII1_TXD1	MII1_RXD1	P1_LED1
47	MII1_TXD2	MII1_RXD2	NC	NC	P1_LED2
46	MII1_TXD3	MII1_RXD3	NC	NC	NC
29	MII1_MDIO	MII1_MDIO	MII1_MDIO	MII1_MDIO	NC
30	MII1_MDC	MII1_MDC	MII1_MDC	MII1_MDC	NC

2.3 Port 2 SRAM-like Interface

2.3.1 8/16 Bit CPU Interface for the AX88782

Signal Name	I/O	Pin No.	Description
CSN	I3	36	Chip Select, active low.
WEN	I3	37	Write Enable, active low.
OEN	I3	42	Read Enable active low.
INT	O3/T	39	Interrupt output to external CPU. Interrupt polarity can be programmed by setting GMCR register bit [27].
ADDR0	I3	68	CPU Address bus bit [0]
ADDR1	I3	67	CPU Address bus bit [1]
ADDR2	I3	66	CPU Address bus bit [2]
ADDR3	I3	61	CPU Address bus bit [3].
ADDR4	I3	60	CPU Address bus bit [4].
ADDR5	I3	59	CPU Address bus bit [5].
ADDR6	I3	58	CPU Address bus bit [6]
ADDR7	I3	57	CPU Address bus bit [7]
ADDR8	I3	50	CPU Address bus bit [8]
ADDR9	I3	49	CPU Address bus bit [9]
ADDR10	I3	48	CPU Address bus bit [10]
ADDR11	I3	40	CPU Address bus bit [11]
DATA0	B3	74	CPU Data bus bit [0]
DATA1	B3	72	CPU Data bus bit [1]
DATA2	B3	71	CPU Data bus bit [2]
DATA3	B3	70	CPU Data bus bit [3]
DATA4	B3	69	CPU Data bus bit [4]
DATA5	B3	64	CPU Data bus bit [5]
DATA6	B3	63	CPU Data bus bit [6]
DATA7	B3	62	CPU Data bus bit [7]
DATA8	B3	56	CPU Data bus bit [8]
DATA9	B3	55	CPU Data bus bit [9]
DATA10	B3	54	CPU Data bus bit [10]
DATA11	B3	52	CPU Data bus bit [11]
DATA12	B3	51	CPU Data bus bit [12] Please Pull-Down with a 4.7K ohm resistor to ground when MODE2, MODE1 and MODE0 is configured to 8-bit bus mode.
DATA13	B3	47	CPU Data bus bit [13]
DATA14	B3	46	CPU Data bus bit [14]
DATA15	B3	45	CPU Data bus bit [15]

2.3.2 8/16/32 Bit CPU Interface for the AX88783

Signal Name	I/O	Pin No.	Description
CSN	I3	54	Chip Select, active low.
WEN	I3	55	Write Enable, active low.
OEN	I3	66	Read Enable active low.
INT	O3/T	61	Interrupt output to external CPU. Interrupt polarity is programmed by setting GMCR register bit [27].
ADDR0	I3	111	CPU Address bus bit [0]
ADDR1	I3	110	CPU Address bus bit [1]
ADDR2	I3	109	CPU Address bus bit [2]
ADDR3	I3	99	CPU Address bus bit [3].
ADDR4	I3	98	CPU Address bus bit [4].
ADDR5	I3	95	CPU Address bus bit [5].
ADDR6	I3	94	CPU Address bus bit [6]
ADDR7	I3	93	CPU Address bus bit [7]
ADDR8	I3	84	CPU Address bus bit [8]
ADDR9	I3	83	CPU Address bus bit [9]
ADDR10	I3	82	CPU Address bus bit [10]
ADDR11	I3	64	CPU Address bus bit [11]
DATA0	B3	119	CPU Data bus bit [0]
DATA1	B3	117	CPU Data bus bit [1]
DATA2	B3	116	CPU Data bus bit [2]
DATA3	B3	115	CPU Data bus bit [3]
DATA4	B3	114	CPU Data bus bit [4]
DATA5	B3	104	CPU Data bus bit [5]
DATA6	B3	103	CPU Data bus bit [6]
DATA7	B3	102	CPU Data bus bit [7]
DATA8	B3	90	CPU Data bus bit [8]
DATA9	B3	89	CPU Data bus bit [9]
DATA10	B3	88	CPU Data bus bit [10]
DATA11	B3	86	CPU Data bus bit [11]
DATA12	B3	85	CPU Data bus bit [12] Please Pull-Down with a 4.7K ohm resistor to ground when MODE2, MODE1 and MODE0 is configured to 8-bit bus mode.
DATA13	B3	81	CPU Data bus bit [13]
DATA14	B3	80	CPU Data bus bit [14]
DATA15	B3	79	CPU Data bus bit [15]
DATA16	B3	77	CPU Data bus bit [16]
DATA17	B3	76	CPU Data bus bit [17]
DATA18	B3	75	CPU Data bus bit [18]
DATA19	B3	74	CPU Data bus bit [19]
DATA20	B3	73	CPU Data bus bit [20]
DATA21	B3	69	CPU Data bus bit [21]
DATA22	B3	68	CPU Data bus bit [22]
DATA23	B3	67	CPU Data bus bit [23]
DATA24	B3	63	CPU Data bus bit [24]
DATA25	B3	62	CPU Data bus bit [25]
DATA26	B3	58	CPU Data bus bit [26]
DATA27	B3	57	CPU Data bus bit [27]
DATA28	B3	56	CPU Data bus bit [28]
DATA29	B3	52	CPU Data bus bit [29]
DATA30	B3	51	CPU Data bus bit [30]
DATA31	B3	50	CPU Data bus bit [31]

2.4 EEROM Interface

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
CS	B3/8mA/ PD	79	127	EEPROM chip select signal PU: Pull-Up with a 4.7K ohm resistor to VCC PD: Pull-Down with a 4.7K ohm resistor to ground **EEPROM size / SK / CS** N/A (default) PD PD 1K(93C46) PD PU 2K(93C56) PU PD 4K(93C66) PU PU
DIO	B3/8mA/ T	78	126	EEPROM bi-direction data signal. This pin should connect to EEPROM's DO and DI pin.
SK	B3/8mA/ PD	77	125	EEPROM clock (1MHz)

2.5 Miscellaneous IO Pin Function

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
MODE2, MODE1, MODE0	I3 I3 I3	30 29 28	41 40 39	Chip Bus Mode Select MODE2 / MODE1 / MODE0 / Chip Mode PD / PD / PD / 8-Bit CPU Bus Mode PD / PD / PU / 16-Bit CPU Bus Mode PD / PU / PD / 32-Bit CPU Bus Mode PU: Pull-Up with a 4.7K ohm resistor to VCC PD: Pull-Down with a 4.7K ohm resistor to ground
TEST0	I3		46	Pull-Down with a 4.7K ohm resistor to ground when the Port 1 is in the PHY, RMII or reverse RMII mode
TEST1	I3		60	Pull-Down with a 4.7K ohm resistor to ground
TEST2	I3		124	Pull-Down with a 4.7K ohm resistor to ground
RST_N	I3	27	28	Chip Reset pin. Active low.
PME	O3	38	59	Power Management Event. This pin is used to indicate that a power management event has occurred.
VCCAH	P	25	26	Internal Regulator 3.3 Volt DC power input
V18	P	26	27	Internal Regulator 1.8 Volt DC power output.
GNDA	P	24	25	Internal Regulator analog ground pin
VCCK	P	35,41,53,73	53,65,87,118	1.8 Volt. DC Power Supply for core logic
VCC3IO	P	31,44,65	42,78,105	Support 1.8V, 2.5V or 3.3 multi voltage DC Power Supply for IO pad
GND	P	32,43,80	45,72, 106,128	Ground

3.0 Functional Description

3.1 Overview

In essence, the AX88782/AX88783 device is a highly integrated Layer 2 switch. It supports two 10/100M ports with on-chip PHYs. It also supports integrated switching logic and packet storage memory. The AX88782/AX88783 is capable of store-and-forwarding packets at wire speed on all ports regardless of packet size. It is a low cost solution for two or three ports Ethernet switch design. After a power on reset, the AX88782/AX88783 provides an 8/16/32 SRAM-like bus interface, which can direct access internal configuration registers through CPU read/write operation. The AX88782/AX88783 can easily be configured to support QoS, IEEE 802.3x flow control threshold setting, broadcast storm control and other functions.

The packet-forwarding engine inside the AX88782/AX88783 uses the packet header information (e.g., DA, SA, VLAN, QoS etc.) extracted and decoded by the packet decoder. It processes this header information and uses the result (list of destination port numbers, VLAN identifier etc.) to do following process:

- Layer 2 Switching
- Head-Of-Line Blocking Prevention
- QoS, including port-based, 802.1P priority tags, IPv4 TOS/IPv6 COS/Diff-Serv packets with four priority queues
- Broadcast Storm Prevention
- Security Operation, include 802.1x, VLAN filtering, and MAC address Restriction.
- Egress/Ingress Bandwidth Control
- Port Mirroring/Sniffer Function
- Filtering/Forwarding Control Frame
- VLANs, including port-based and tag-based IEEE 802.1Q VLANs.
- Two Built-in 10/100M Ethernet PHY IP power down control and configuration
- IPv4 IGMP and IPv6 ICMP/MLD (Multicast Listener Discovery) snooping
- IEEE 802.1D Spanning Tree
- Double-tagging (1Q-in-1Q) processing
- RMON Counters for network management
- PPPoE/IPv4/TCP/UDP/ICMP/IGMP checksum offload
- Microsoft Wake-Up Frame Detection, Magic Packet Detection, Link Status Change Detection
- Power Management

3.2 Clock

The AX88782/AX88783 only needs one external 25 MHz crystal or oscillator, via pins P0_XTLP/P0_XTLN, to provide the reference clock to the internal PHY0's PLL circuit, generate a free-run 100Mhz clock source for the AX88782/AX88783 internal usage and provide a 25Mhz clock source for the 2nd embedded Ethernet PHY usage. The AX88782/88783 provides RX and TX clocks (25Mhz output) in Reverse MII mode or 50Mhz reference output in Reverse RMII mode. These output clocks are derived from the internal 100Mhz PLL circuit. The external 25Mhz crystal spec is listed in below table.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance(@25℃)		±30ppm
Operation Temperature Range		0℃ ~ +70℃
Aging		±3ppm/year

The External 25MHz Crystal Specifications

For the 25MHz oscillator, its feedback resistor isn't integrated into the 25MHz oscillator, so it is necessary to add 1Mohm feedback resistor on external circuit.

3.3 Built-in Power-On-Reset

The AX88782/AX88783 integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset system logic after 1.8V core power ramping up to 1.2V (typical threshold). The external hardware reset input pin, RST_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. The user can read CIRR [16] ChipInitDone bit to check if the initialization of the chip is finished after reset back to high.

3.4 Built-in Voltage Regulator

The AX88782/AX88783 integrates an internal 3.3V to 1.8V low-dropout-voltage and low-standby-current voltage regulator. The internal regulator provides up to 300mA of driving current for the 1.8V core/analog power of the chip to satisfy the worst-case power consumption scenario. The internal regulator can operate in stand-by mode to consume less current when the required driving current is less than 30mA. The stand-by mode register is located in PCR [31]. For more details on voltage regulator DC characteristic, please refer to section 6.3.2.

Note: The AX88782/AX88783's built-in 3.3V to 1.8V Voltage Regulator can be disabled easily by connecting the V18 pin to the external 1.8V power source and connect a 0 Ohm resistor between VCCAH and V18 pins. To disable the built-in voltage regulator might reduce the AX88782/AX88783 operating temperature about 5°C if heat is the key concern in your design.

3.5 Two Built-in 10/100M Base-TX Fast Ethernet DSP-Based PHY

There are two 10/100M Base-TX Fast Ethernet DSP-Based PHY built in the AX88782/AX88783. The basic feature is fully compliant with 100 BASE-TX and 10 BASE-T PMD level standard (802.3u, FDDI-TP-PMD and 802.3).

- Supports MDI/MDIX auto crossover function (Auto-MDIX)
- Supports parallel and serial control interface
- Supports MII interface
- DSP-based highly integrated embedded Ethernet twisted-pair symbol transceiver solution
- DSP-based adaptive line equalizer for superior immunity to noise and inter-symbol interface
- Full compliance with 100 BASE-TX and 10 BASE-T PMD level standards (IEEE 802.3u, FDDI-TP-PMD and IEEE 802.3)
- DSP-controlled symbol timing recovery circuit
- Baseline wander corrective circuits compensates data dependent offset due to AC coupling transformer
- Multifunction LED output
- Full-duplex and Half-Duplex

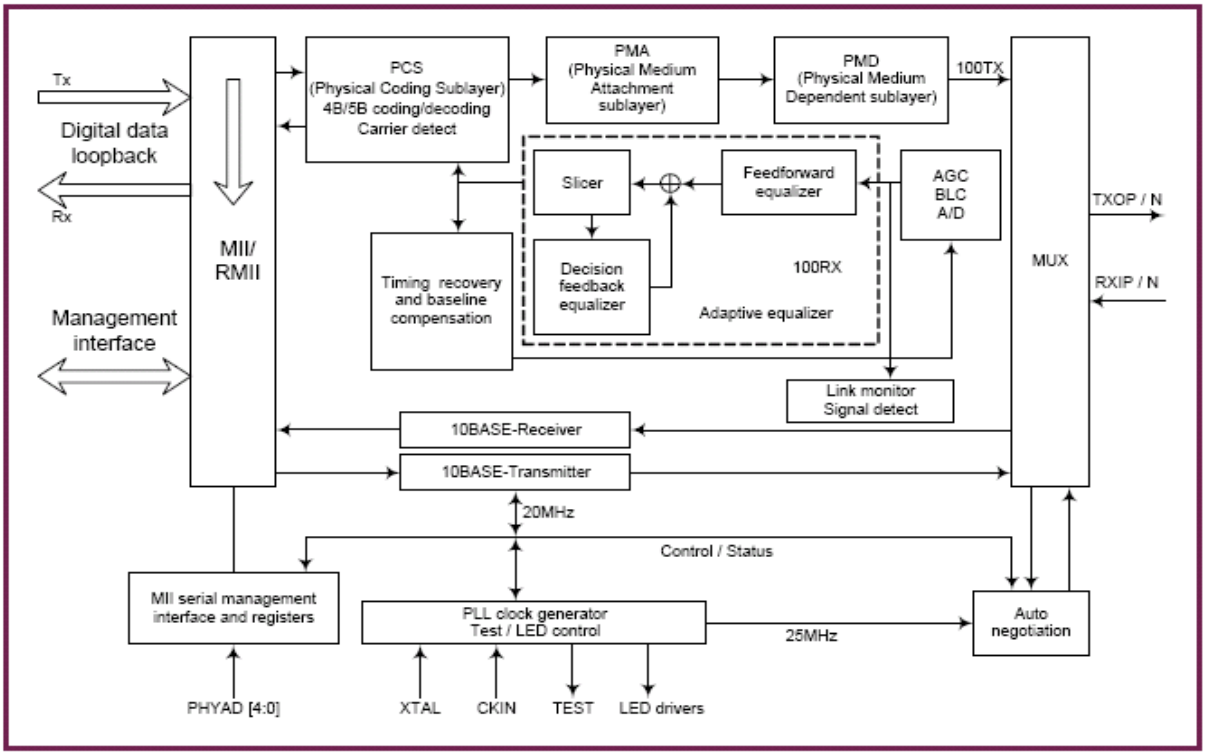


Fig 8 Built-in 10/100M Base-TX Ethernet PHY architecture

Adaptive Equalizer
The cable's amplitude and phase distortions will cause inter-symbol interface (ISI), which make clock and data recovery impossible. This design eliminates these distortions by automatically adjusting the weights of the feedback equalizer and feed-forward equalizer to match the inverse of cable impulse response.

Baseline Compensation
The transmitter sends DC and AC signals as a pair. Both the receiving side and transmitting side have a transformer that blocks the DC signals. When the AC signal loses its DC component, the AC signal becomes distorted. This design provides a circuit that restores the DC component to its corresponding AC signal and delivers them as a complete signal to the receiver.

Link Monitor/Signal Detect
When the receiver receives a signal, the receiver will detect the signal's level. If the signal level is above 400mV in 100BASE-TX mode, the receiver will send a Signal Detector (SD) signal to the MII. If the level is below 400mV, the SD signal will then be de-asserted in 722us.

Carrier Detect
The Physical Coding Sub-layer (PCS) checks Physical Medium Attachment (PMA) data to see if the packets meet IEEE 802.3-defined preamble (J/K/packets in 100BASE-TX) standards. If the packets are correct, the PCS sub-layer will start to process the data and send it to MII.

4B/5B Coding
The Physical Coding Sub-layer (PCS) converts received/transmitted data according to IEEE 802.3-defined coding standards, such as 4B/5B and scrambling/de-scrambling.

MII Serial Management Interface
The MII serial management interface (SMI) is the IEEE 802.3-defined serial coding control interface. Every register in this design can be read or write accessed through this interface.

Auto-Negotiation
The 10/100M Base PHY can automatically negotiate its operating modes with other PHY devices over twisted pair cable connections. Clause 28 of the IEEE 802.3u defines the auto negotiation mechanism.

Opmode [2]	Opmode [1]	Opmode [0]	Description
0	0	0	Auto-negotiation enable with all capabilities
0	0	1	Auto-negotiation enable with 100 BASE-TX FDX/HDX ability
0	1	0	Auto-negotiation enable with 10 BASE-T FDX/HDX ability
0	1	1	Reserved
1	0	0	Manual selection of 100 BASE-TX FDX
1	0	1	Manual selection of 100 BASE-TX HDX
1	1	0	Manual selection of 10 BASE-T FDX
1	1	1	Manual selection of 10 BASE-T HDX

Table 1 PHY Operation Mode Setting by PCR OPMODE [2:0]

Power-up Control Flow and Power-down Operation
In the power-down state, the PCR register power-down bit must be driven to high; in all other states the power-down bit must be driven to low. During the reset period, the PCR Phyreset bit must be driven to low for about 500 ns and then driven to high; In normal condition PCR Phyreset bit is driven to high. For Band-gap, PLL, and crystal PAD stable issue, the power-on state must be longer than 60 ms.

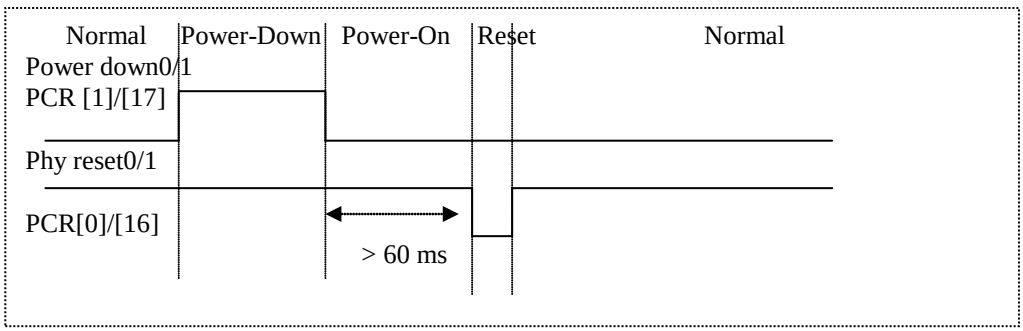


Fig 9 Power-up and Power-down Operation

Power-down mode through MDIO interface

Set PHY BMCR bit 11 to high to enter the power-down mode. At this time, PLL, band-gap, and XTLP (Crystal) are alive, and the other clocks and blocks within PHY module are off. This operation can go through MDIO interface or using register write process on MDIO register. It is recommended power-down the PHY0 through MDIO to keep the core clock alive so the switch operation and the register read/write control can still working. .

PHY Loop-back Function Support

The loop-back function can be enabled by programmed BMCR register bit [14] loop back enable bit through MDIO interface or through the AX88782/AX88783 PCR loop back bit. If this bit is set to one, then the entire data stream received from MII TX interface will be forward to MII RX and returned back to switch core engine.

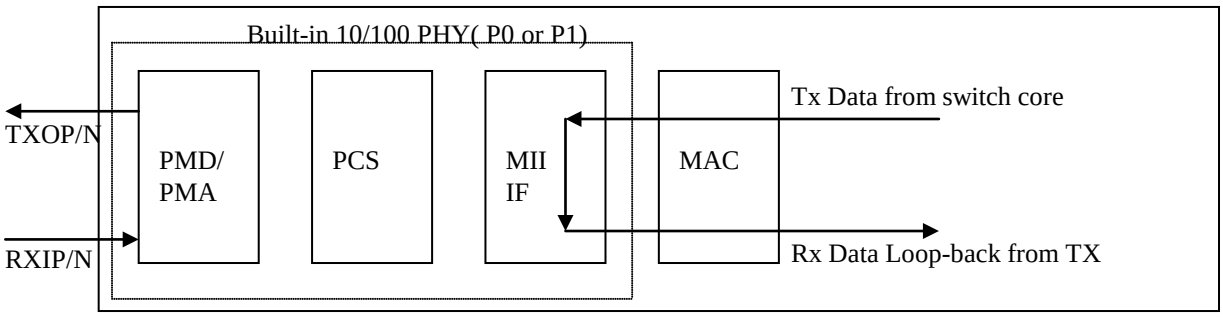


Fig 10 Loop-back data path when internal loop back function is enabled

Programmable LED Output Function

The AX88782/AX88783 is able to support a user programmable LED output function. There are six LED signal outputs from PHY: speed, full-duplex, collision, RX activity, TX activity and link status. The user can assign any of these function outputs to the LED pins by programmed LCR register. The AX88782 only supports two LED pin outs and the AX88783 supports three LED pin outs.

Access PHY Registers

The AX88782/AX88783 supports direct control of the internal PHY through software configuration registers. The user can program PCR to control internal PHY0 and PHY1 operations including PHY ID, Operation Mode, Loop-back, Power-down Mode and software reset functions. The user can also access internal PHY register through MDIO interface or program PPMR and MRCR CPU read/write register. The AX88782/AX88783 converts these read/write setting into MDIO access command indirectly.

Power-Saving Function

The AX88782/AX88783 supports power-saving function on both internal PHY. When PCR [15] power-saving bit is set to zero, the hardware logic will enable auto-detect function and reset the unused logic block within the PHY module. If PCR [15] power-saving bit is set to one then software takes the control and program the PCR [13] to enable the power-saving on PHY0 and PCR [29] for PHY1.When the power-saving function is enable, the TX module will constantly send out idle pulse and waiting to be link up again if the cable is plug in again.

3.6 Basic MAC Function

Full Duplex 802.3x Flow Control
In full duplex mode, the AX88782/AX88783 supports the standard flow control mechanism defined in respect to IEEE 802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When space of the packet buffer is less than the initialization setting threshold value, the AX88782/AX88783 will send out a PAUSE-ON packet with pause time equal to "0xFFF" to stop the remote node transmission. Then, the AX88782/AX88783 will send out a PAUSE-OFF packet with pause time equal to zero to inform the remote node to retransmit packet if it has enough space to receive packets. When the AX88782/AX88783 receives a PAUSE-ON packet from remote node, the AX88782/AX88783 will finish the current transmit process and wait for PAUSE-OFF packet to re-start transmit process.

Half Duplex Back Pressure Control
In half duplex mode, the AX88782/AX88783 provides a backpressure control mechanism to avoid dropping packets during network congestion. When the packet buffer size is less than the threshold value, the AX88782/AX88783 will send a JAM pattern from the low threshold value port if it senses an incoming packet, thus forcing a collision to make the remote node transmission back off and will effectively avoid dropping packets. And the AX88782/AX88783 will not send out a JAM packet until it has enough space to receive one packet. In GMCR, if bit [23] ContinueSendJam bit is set to one then the AX88782/AX88783 will never stop backpressure (Only for 10Mps).

Broadcast Storming Prevention
The AX88782/AX88783 can enable broadcast storm filtering control by MaxStorm [1:0](defined in GMCR [15:14]). This allows limitation of the number of broadcast packets into the switch, and can be implemented on a per port basis. The threshold of number of broadcast packets is set to 64/48/32. When enabled (i.e., MaxStorm [1:0] is not 00), each port will drop broadcast packets (Destination MAC ID is ff ff ff ff ff ff) after receiving 64/48/32 continuous broadcast packets. The counter will be reset to 0 every 1 second or when receiving any non-broadcast packets (Destination MAC ID is not ff ff ff ff ff ff).

When disabled (i.e., MaxStorm [1:0] is 00), or the number of non-unicast packets received at the port is not over the programmed threshold, the switch will forward the packet to all the ports (except the receiving port) within the VLANs specified at the receiving port.

Head-Of-Line Blocking Prevention
The AX88782/AX88783 incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. The AX88782/AX88783 will first check the destination address of the incoming packet when the flow control function is disabled. If the destination port is congested, then the AX88782/AX88783 will discard this packet to avoid blocking the next packet in line.

RX Packet filtering and TX CRC Regeneration
The AX88782/AX88783 discards Ethernet frame packet size less than 64 bytes and can be programmed to accept Ethernet frame size up to MPL [10:0] in GMCR (default value is 1522). Receive MAC will drop error packets, CRC error packets, and pause packets. Transmit MAC can re-calculate new CRC if GMCR [26] is set to one.

Late Collision and Back-Off control
If a transmit packet experiences collision after 512 bit time of transmission, it's called late collision and the packet will be dropped. The AX88782/AX88783 has an option in GMCR [13] NoAbort to for MAC never abort when exceed maximum collision limit if it is set to one and used only in half-duplex mode. GMCR [21] SuperMac bit can reduce back-off count and collision when in half-duplex mode and set to one.

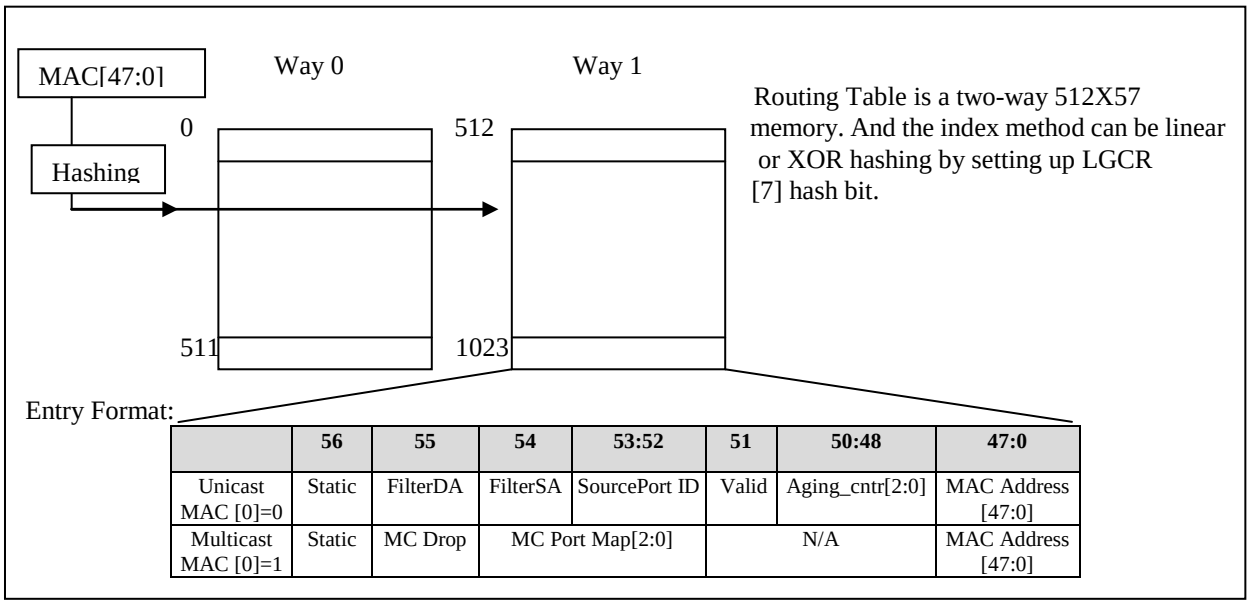
3.7 Basic Switch Function

Address Lookup Memory
The switch engine makes use of internal SRAMs to store the routing address tables used. The internal tables are:

- 1024-Entry MAC address table
- 16-Entry VLAN tag table (full range 4K VLAN ID support)
- 16-Entry Multicast Filter Table to limit multicast traffic to Port 2 (Host port)
- 8-Entry IGMP table

Routing-Table Format
The MAC address table is used for L2 forwarding, source address learning and read/write specified entries by the user. Its format is list below.

Routing Table Entry	Description
MAC Address [47:0]	Ethernet MAC address [47:0] (Unicast or Multicast)
Aging_cntr [2:0]	Routing table aging timer. The timer will automatically clear Valid bit when time out reach.
Valid	The forwarding information in this entry is valid if this bit is set to one.
SourcePort ID [1:0]	Source port number of this MAC address: 00 : Port 0, 01 : Port 1 or 10 : Port 2.
FilterSA	Incoming packet will be dropped if received packet's SA MAC matches with this MAC address and this bit is set to be 1.
FilterDA	Incoming packet will be dropped if received packet's DA MAC matches with this MAC address and this bit is set to be 1.
Static	When set to one, The information of this entry will be frozen and will not be replace with any new learned SA.
MC Drop	Drop received multicast packet if received multicast packet's DA MAC matches with this MAC address and the Static bit is set to one.
MC Port Map [2:0]	Define Multicast Group Port Map. {Port2, Port 1, Port 0} If received multicast packet's DA MAC matches with this MAC address and Static bit is set to one, the switch will forward this multicast packet to the same group defined in this field.



	56	55	54	53:52	51	50:48	47:0
Unicast MAC [0]=0	Static	FilterDA	FilterSA	SourcePort ID	Valid	Aging_cntr[2:0]	MAC Address [47:0]
Multicast MAC [0]=1	Static	MC Drop	MC Port Map[2:0]		N/A		MAC Address [47:0]

Fig 11 Routing Table Format

Routing Table Read/Write

The switch supports 1K MAC routing table entries for switching. Two-way dynamic address learning is performed when a good unicast packet is completely received. Total 1K routing table entries can be indirectly read or write through the LRCR0 and LRCR1 registers.

1. Setup MAC address
2. Setup source port, page and filtering information for unicast MAC and MC Drop, MC port map for multicast MAC
3. Set static bit for multicast MAC or unicast MAC that don't want to be aging out
4. Set Write_RT or Read_RT bit if write/read operation is performed.
5. Clear Write_RT or Read_RT bit once finish the command

The user can flush the routing table by enabling Flush_RT bit within LRCR1.

Example: Write an Entry into the Routing Table

1. Setting up LRCR0 and LRCR1 register MAC information include MAC_addr [47:0], source port ID, filtering control and static bit value.
2. Enable write process by setting the Write_RT bit to one.
3. Write 0 to the Write_RT bit to clear write process.

MAC Address Learning and Aging

The AX88782/AX88783 is able to automatically learning new MAC address and update source port, time stamp, and valid information whenever receive good frame with unknown source MAC address. The AX88782/AX88783 provides an option to learn once or stop learning by configuring LLCR. The routing table also has a programmable aging out timer in LLCR [24:16]. Default value is 0x1FF.and each step is about 1.34 second.

Only the learned address entries are scheduled in the aging module. Address aging function is supported for topology changes such as an address moving from one port to the other. That is, one station does not transmit any packet for a period of time. When this happens, the belonging MAC address will be aged out (removed) from the address table. The aging out time can be programmed automatically through the EEPROM or CPU write configuration, its default value is about 687 seconds. And aging function can enable or disable by the user. Normally, disabling aging function is for security purpose. Aging timer is located in LLCR [24:16].

VLAN Table

The VLAN tag table is used to determine the multiple outgoing ports for L2 broadcast packets and to tag the VLAN identity onto each incoming untagged frame. There are 16 VLAN table entries located in the VER0 ~ VER15. Its format is list in the following table.

VLAN Table Entry	Description
Forward_map [2:0]	Forwarding information for this VLAN ID.(1: Forward 0:Filter) [0]: Port 0 [1]: Port 1 [2]: Port 2
Tag_map [2:0]	Output tag or un-tag information for this VLAN ID.(1: Tag, 0: Untag) [0]: Port 0 [1]: Port 1 [2]: Port 2
VLAN ID [11:0]	Full range VLAN ID can be programmed here. Note: 0x000 and 0xFFF is reserved for management purpose.
Valid	Valid bit for this VLAN ID and mapping information.

17	16:6	5:3	2:0
Valid	VLAN ID [11:0]	Tag_map [2:0]	Forward_map [2:0]

Fig 12 VLAN Table Format

If the 802.1Q function is enabled, the switch engine will look-up this table and forward tag or un-tag packet to the corresponding output ports. Once the 802.1Q is enabled then the user should not turn on port-based VLAN function on LGCR [20].

IGMP Table

There are eight multicast IP entries in this table from IER0 to IER7. Its format is list below:

IGMP Table Entry	Description
IP [27:0]	Lower 28 bits of IP address. Assume IP address bit [31:28] is 1110 (i.e., multicast IP address).
Port_map [2:0]	Port mapping information
Valid	Valid bit

31	30:28	27:0
Valid	Port_map [2:0]	IP [27:0]

Fig 13 IGMP Table Format

When the IGMP snooping function is enabled, the switch engine will look-up this table and copy the packet to the corresponding ports if the receiving packet is a multicast IP packet (IP [31:28]=1110), IP [27:0] is found in this table and the valid bit is set to one.

Host Port Multicast Filter Table

There are 16 Multicast Filter entries in this table from P2MFR0 to P2MFR15. If any one of the valid bits within the table is set to one then any multicast packets forwarding to the host port whose DA MAC address is not match with the valid entry's HMAC field will be dropped on Host Port (Port 2). The multicast MAC entry in this table only contains last 23 MAC address bits (from bit [24] to bit [47]), which means only the last 23 bits will be compared. If none of the valid is set then no multicast packet will be filtered.

The forwarding engine only sends multicast packets to the host port when all four of the following conditions are valid:

1. The incoming packet's DA MAC last 23 bits matches up with one of the 16 entry's HMAC field [22:0],
2. DA MAC is a multicast packet
3. Source port information matches with the From Port 0 bit or the From Port 1 bit
4. Valid bit is set to one

Any multicast packet that supposed to forward to the host port (port 2) not meet all these four conditions will be dropped if any of these entry has valid bit set to one.

NOTE: Assume the expected MAC address is 01-23-45-67-89-AB then the HMAC [22:0] should be 67-89-AB.

Multicast Table Entry	Description
HMAC [22:0]	Last 23 bits MAC address {MAC[30:24],MAC[39:32],MAC[47:40]}
From Port 0	This multicast packet is received from Port 0
From Port 1	This multicast packet is received from Port 1
Valid	Valid bit

25	24	23	22:0
Valid	From Port 1	From Port 0	MAC [22:0]

Fig 14 Host Port Multicast Filter Table Format

Packet Filtering and L2 Forwarding Process

The switch uses a simple store-and-forward algorithm as a packet switching method. After receiving incoming packets, the switch will store the packet to the embedded 32K byte packet buffer memory first. The forwarding engine will look up the VLAN table, the Spanning Tree Status Table, the Address-Lookup Table (Routing Table), the Multicast Filtering Table, the IGMP Table and decide the forwarding ports. Only the good receiving packets will be forward. Conditions of good packets are below:

1. CRC is correct.
2. 64 Bytes <= Packet Length <= Maximum Packet Length
3. SA MAC and DA MAC should not be the same

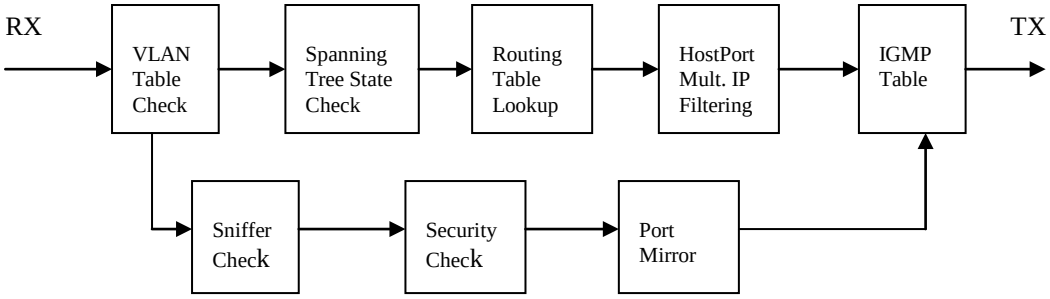


Fig 15 Forwarding Process

The switch engine receives good Ethernet frame from the Receive MAC. The Fig 15 shows how the forwarding process performs inside the AX88782/AX88783 switching engine.

1. First if the receive Ethernet frame is a tag frame and if 802.1Q function is enabled then the switch will go through the VLAN table and check forwarding information based on the VLAN group information.
2. If 802.1D is enabled and spanning tree status is checked then the switch will decide whether to continue forwarding process or drop the packet.
3. The switch performs routing table look-up based on the DA MAC hashing index approach.
4. The Host Port Multicast Filter Table checks if the incoming multicast MAC address matches with any valid entries found in this table. If DA is not a legal MAC entry from the expect source port and the table has valid entry, then the packet will be dropped.
5. If IGMP is enabled, then the switch engine will forward the multicast packet if destination IP found in the table.
6. If sniffer function is enabled and the packet matches with the sniffer condition, then the packet will be copied to the sniffer port.
7. The switch engine also examines the packet for security purpose. There are eight extra security MACs defined in the AX88782/AX88783 to enhance security function. Any illegal packet will be dropped if the packet cannot pass the internal security check.
8. If the port mirror function is turned on then the incoming packet will be duplicated to the mirror port.

Host Port Software Switching Function

The AX88782/AX88783 also supports host port software switching function. When the GMCR [28] is set to one, all incoming packets from port 0 and port 1 forward to the host port will be inserted an extra byte before CRC field to indicate source port information. If GMCR bit [28] is set to one, then software will provide forwarding information in the last byte of payload and the AX88782/AX88783's switch engine will decode last 2-bit information and forward to corresponding ports. The software can take over the switch engine and control forwarding function. If the last two bits are 00 then the packet will forward to port 0. If the last two bits are 01 then the packet will forward to port 1.

3.8 VLAN Support

Port-Based VLAN

The AX88782/AX88783 supports three port-based VLAN groups to ease the administration of logical groups of stations that can communicate as if they were on the same LAN, and it can move, add or change numbers of these groups. This method can effectively prevent the broadcast storming from interfering with the transmission performance between ports. If port-based VLAN is enabled, the ports belonging to different groups are independent. Only the destination port of broadcast packets in the same group will be allowed. Furthermore, this method of the VLAN group dividing is very useful to avoid unnecessary broadcast packets and increase security.

Overlapping port-groups are allowed during some operations. For example, two VLAN groups can share any port, and all the packet-forwarding operations between these two groups remain independent except for the overlapping port. Only the overlapping port can use the same destination MAC address for two different VLAN port-groups and receive broadcast packets from two different VLAN groups. The Port-based VLAN provide a very simple approach to VLAN function.

The user need to enable LGCR [20] Port-based VLAN enable bit and program PVCR to set up port-based VLAN per-port mapping information before using this function.

Tag-Based VLAN

Virtual LANs are used to form broadcast domains of hosts etc. on the network, thus ensuring that broadcast traffic is limited. Virtual LANs also add some intra-networking security features. Virtual LANs are identified within a four-byte tag attached to the packet.

<table>
<tr><th>6 bytes</th><th>6 bytes</th><th>2 bytes</th><th colspan="3">2bytes TAG Field</th><th></th></tr>
<tr><td rowspan="2">DA [47:0]</td><td rowspan="2">SA [47:0]</td><td rowspan="2">81-00</td><td>3bits</td><td>1bits</td><td>12bits</td><td rowspan="2">----</td></tr>
<tr><td>Priority</td><td>CFI</td><td>VID [11:0]</td></tr>
</table>

Fig 16 802.1Q VLAN Tag Frame Format

There are two types of VLAN tagging options: Implicit and Explicit. Explicitly tagged packets are 802.1Q compatible. In this case, the VLAN tag is already attached to the incoming packet by the source. Implicitly tagged packets have no tag on the input, but are tagged in the AX88782/AX88783. They are tagged based on the port, sub-net, MAC address or protocol of the packet. If no tagging is required in the output (defined in the address look-up results), the AX88782/AX88783 will de-tag the packet before transmission.

According to 802.1Q (1998 p.39), packets can be untagged, priority-tagged or VLAN-tagged at the input, but only untagged or VLAN-tagged at the output.

The VLAN classification is the first step to be performed before the VLAN table lookup. To classify a unique VID value to a received frame is defined as follows:

1. VLAN-tagged frame: If the tagged VID = 0 (i.e., Null VID or priority tag), then replaced with port's PVID value. Else its tagged VID value is used.
2. Non-VLAN-tagged frame: Append with port's PVID value and Priority field. (Default PVID=0x001)

After the unique 12-bits VID is classified, the AX88782/AX88783 then looks up the port mapping information in the VLAN table, processes the incoming VLAN packet with the ingress/egress rule and then forward this packet to the valid destination ports with specified tagging control process. Note: The VID=0x000 and 0xFFF are reserved VLAN ID.

Ingress/Egress rule:

1. Ingress frame type control: to admit all frames or to admit only VLAN-tagged frames.
2. Ingress filtering control: to filter the Ethernet frame received from a port that is not included in the classified VLAN group member. That is, if VLAN ID of this receiving port is not list in the VLAN table port mapping field then this packet will be dropped.
3. Egress frame type control: if this port is configured to be the untagged member set of VID entry then all the forwarding packets to this port will passing the untag packets out. The VLAN table entry has a tag-untag field to define whether to tag or to untag on specific output ports.

The user needs to enable LGCR [22] 802.1Q enable bit, and build up VLAN table by filling in VLAN entry through register write operation between VER0 (entry1) and VER15 (entry16) before processing VLAN function.

- Ingress rule flow:

1. Priority packet (VID = 0) is taken as untagged packet.
2. If (Untagged packet or priority packet)

```
{If (Tagged-frame only) then drop this untagged packet.
     Else
       {If (Destination Port exist on VLAN Table)
              Forward this packet to Destination Port.
        Else
           Drop this packet
       }
 }
```

Note:

- Untagged frame will be added VID and QoS filed, using the PVID & QoS setting of the receive port.
- Priority Packet will be replaced its VID field with the PVID of the receive port, but no change to QoS field.

3. If (Tagged Frame)

```
{If the port that received this packet is not in member set of VID in this packet
    { If (Ingress filter disable)
        {If (Destination Port exist on VLAN Table)
              forward this packet to Destination Port.
         else
              drop this packet
         }
      else
         drop this packet.}
 else
    {If (Destination Port exist on VLAN Table)
         forward this packet to Destination Port.
      else
          drop this packe}
 }
```

- Egress rule flow:

```
If (this port is in Untagged member set of this VID)
   {Take the tag off and transmit this packet}
Else
   {Transmit this packet}
```

802.1Q-in-1Q Double Tagging Support

The AX88782/AX88783 supports double tagging if the LGCR [15] QinQ enable bit is set to one. The QSR rgi_sptag [15:0] is defined as service provider tag when
1. The Receiving Port is the Access Port
2. The Receiving Port is the Uplink Port and the receiving tag does not match with the QSR rgi_tpid [15:0] *

If both these conditions are true then service provider tag will be asserted.
Note: Make sure VLAN ID in rgi_tpid [11:0] is a valid entry and can be found on VLAN Table Entry.

When the egress port is an access port then the service provider tag will be removed.
The user can configure access port or uplink port by programmed P0MCR/P1MCR/P2MCR [15] uplink port bit.

RX Port Type	RX Frame Type	TX (Access Port)	TX (Uplink Port)
Access Port	Un-Tag	Untag	One Tag (SP tag)
Access Port	One Tag (tag)	One Tag (tag)	Double Tag (SP tag + tag)
Access Port	Double Tag (tag1+tag2)	Double Tag (SP tag + tag2)	Triple Tag (SP tag+SP Tag+tag2)
Uplink Port	Un-tag	Un-Tag	One Tag (SP tag)
Uplink Port	One tag (tag==tpid)	Un-tag	One Tag (SP tag)
Uplink Port	One tag (tag! = tpid)	One tag (SP tag)	Double Tag (SP tag+tag)
Uplink Port	Double tag (tag==tpid)	One tag (tag)	Double Tag (SP Tag + tag)
Uplink Port	Double tag (tag! =tpid)	Double tag (SP tag +tag)	Triple Tag (SP tag+SP tag+tag)

Table 2 Double Tagging Access Port and Uplink Port TX operation

Table 2 shows how the AX88782/AX88783 handle double-tagging function when RX port is configured to Access port or Uplink port and receiving Ethernet frame is untag, one tag, double-tag frame.

3.9 IEEE 802.1D Spanning Tree

The AX88782/AX88783 has the capability to support implementation of the IEEE 802.1D Spanning Tree Protocol. All ports can be programmed to be in the port state as required by the spanning tree protocol. If the Spanning Tree Protocol option is enabled, BPDUs are identified and treated according to port state. All five states defined in IEEE 802.1D are supported: Blocking, Listening, Learning, Forwarding and Disabled. The following is performed in the different states:

- **Blocking** - No frame relay (to prevent frame duplication due to multiple paths). Forwarding and learning are disabled but BPDUs will still be received and sent to the processor. The Ethernet frame is forwarded to the CPU if it is a BPDU frame and the frame is discarded otherwise. All outgoing frames except outgoing BPDUs will be masked from the path to the PHY.

- **Listening** - Preparing to participate in frame relay. Forwarding and learning are disabled but BPDUs will still be received and sent to the processor. That is, the frame is forwarded to the CPU if it is a BPDU frame and the frame is discarded otherwise. All outgoing Ethernet frames except outgoing BPDUs will be masked from the path to the PHY.

- **Learning** - Preparing to participate in frame relay. If the port is in the Learning State, all source addresses of the incoming Ethernet frames from the PHY will be learned. All incoming Ethernet frames except incoming BPDUs from the PHY will be discarded after being learned, all outgoing Ethernet frames except outgoing BPDUs will be masked from the path to the PHY. That is, forwarding is disabled but learning is enabled. BPDUs are received and sent to the processor.

- **Forwarding** - Participating in frame relay. If the port is in the Forwarding State, the frame is forwarded to the CPU if it is a BPDU frame. All source addresses of the incoming Ethernet frames from the PHY will be learned and then forwarded based on the switch routing decision. All outgoing Ethernet frames will be transmitted to the PHY.

- **Disabled** - No participation in frame relay or Spanning Tree algorithm. Both forwarding and learning are disabled. BPDUs are discarded.

The AX88782/AX88783 pass all the BPDU packets to the CPU port and enable the CPU to implement the spanning tree algorithm. The default values are the Bridge group address and the All LANs bridge management group address according to 802.1D.The user can find Spanning Tree status bit information in PVCR [5:4](Port 2), [3:2] (Port1) and [1:0] (Port 0).

Note: Blocking and Listening is the same operation for the AX88782/AX88783.

3.10 QoS and Ingress/Egress Rate Limit Operation

Based on market trends, networking increasingly demands support data, voice and video streams. The switch not only controls data packet but also provides service of multimedia data. The AX88782/AX88783 provides four priority queues on each port. The AX88782/AX88783 identifies the packets as high priority based on several types of QoS priority information:

- Port-based priority
- 802.1P/Q VLAN priority tag
- IPv4 TOS/IPv6 COS/DiffServ (DSCP) priority information

Port-Based Priority (Port Pair Priority)
The AX88782/AX88783 provides two Port-Pairs for bandwidth management. The user can assign any two ports as one Port-Pair with internal registers setting. All traffic between these two defined port-pair ports' packets will always map to the configured priority queue in the PPMR [11:10]. That is, the two Port-Pair ports will obtain more bandwidth than other ports when congested. If PPMR AllBit is set to one and Port Pair is defined to the same port number then all the traffic in and out of the switch will forward to this monitor port. Port Pair control register is located in PPMR.

802.1P-Based Priority
When the 802.1P VLAN tag priority applies, the AX88782/AX88783 recognizes the 802.1Q VLAN tag frames and extracts the 3-bit User-defined Priority information from the VLAN tag. The AX88782/AX88783 has a programmable 8-to-4 priority-mapping table to convert receiving VLAN tag frame's 3 priority bits into one of the internal 4 queues. Therefore, VLAN tagged frames with User-defined Priority value = 0~7 will be mapped to the AX88782/AX88783 's internal queue i (i=0~3). The mapping table located in P0QMTR/P1QMTR/P2QMTR can be update through register read/write or pre-configured in EEPROM.

IPv4/IPv6 Priority
The AX88782/AX88783 supports both IPv4 and IPv6 Priority mapping to help differential traffic pattern and improve QoS quality between voice, data, multimedia, and VOIP and network management. The IPv4 TOS (Type of Service) and the IPv6 COS (Class of Service) table are located in QPTR.

The user can build an 8-to-4 QoS mapping table by filling in the mapping queue number (0-3). There is a global enable bit to turn on the mapping table function and it is located in LGCR [1] COS_En and LGCR [2] TOS_En. The LGCR [0] QoSSel is defined whether to convert upper 3 bits [5:3] or lower 3 bits [2:0] of COS/TOS as Priority table index. (Default is upper 3 bits, which is IP Precedence) The VLAN tagged frame and 6-bit DS-field in the IPv4 and IPv6 frame format are shown below:

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	
DA	SA	802.1Q Tag (Optional)	08-00	Version IPv4=0100	IHL	TOS [0:5]= DSCP field	----

Fig 17 IPv4 Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	6 bits	
DA	SA	802.1Q Tag (Optional)	86-DD	Version Ipv6=0110	COS [0:5]= DSCP field	----

Fig 18 IPv6 Frame Format

DiffServ-Based Priority

The AX88782/AX88783 identifies TCP/IP Differentiated Services Code point (DSCP) priority information from the DSCP-field defined in RFC2474, if TCP/IP's TOS/DiffServ (DS) based priority is applied. The DSCP field byte for the IPv4 is a Type-of-Service (TOS) octet and for IPv6 is a Traffic-Class octet.

The recommended DiffServ Code point is defined in RFC2597 to classify the traffic into different service classes. The AX88782/AX88783 extracts the code point value of DSCP-fields from IPv4 and IPv6 packets, and recognizes the priority of the incoming IP packet following user-defined QoS mapping table (DQR). Recommend mapping priority example is list below:

High priority: if the DS-field = (EF, Expected Forwarding:) 101110
(AF, Assured Forwarding:) 001010; 010010; 011010; 100010
(Network Control:) 110000 and 111000

Low priority: if the DS-field = other values.

The 6-bit DSCP field with 64 possibilities can be fully decoded and mapped to internal four queues through register setting. The DSCP mapping table is located in DQR0~DQR3 and total 64 DSCP level is able to assign to any queue from 0 to 3 within switch core engine. There is a Table mapping enable bit located in LGCR [3] DSCP_En to turn on DSCP mapping function.

QoS Mapping Order and Flow

If the flow control is enabled then all the traffic within the port will map to queue 0, which means no QoS within that port. By default, IPv4/IPv6 DSCP priority mapping > IPv6 priority mapping or the IPv4 priority mapping > VLAN priority mapping. If LGCR [8] VLAN_QoS_En is set to one then VLAN QoS priority mapping will override the mapping result.

There is a per-queue weighting register located in register P0QWR/P1QWR/P2QWR to program weighting on each queue. The higher the weighting value, the more traffic bandwidth will be scheduled out from that queue.

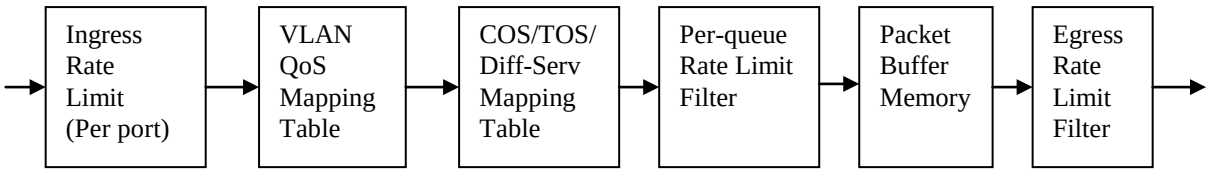


Fig 19 Rx/Tx Bandwidth Filtering and QoS Mapping Data Flow

The AX88782/AX88783 QoS flow and traffic shaping flow is shown in the Fig19. The per-port ingress rate limit control will drop the packets that exceed the ingress bandwidth threshold value defined in the register P0RLR [11:0], P1RLR [11:0] and P2RLR [11:0]. If LGCR 1P_En is set to one then receiving packet will reference QoS mapping table in the register P0QMTR, P1QMTR and mapping the VLAN QoS value to the internal queue 0 ~ 3. If LGCR COS_En is enabled and the receiving packet is an IPv6 packet then the COS mapping table located in the QPTR will convert the 3-bit QoS value to one of the internal queues (0~3). If LGCR TOS_En is enabled and the incoming packet is an IPv4 packet then the TOS mapping table located in the QPTR register will map the 3-bit QoS value to one of the internal queues. If LGCR DSCP_En is enabled and the receiving packet is an IPv4 or IPv6 packet then 6-bit QoS (64 levels) mapping table located in the DQR0/DQR1/DQR2/DQR3 register will map this QoS value to an internal assigned queue.

The DSCP mapping table has higher priority if both DSCP_En and TOS_En (or COS_En) are enabled. The RX Per queue rate limit filter will filter out packets that exceed the per-queue threshold register value defined in the register P0RQR0/1, P1RQR0/1 and P2RQR0/1.

The egress rate limit filter will make sure the output port or output queue traffic has its own bandwidth that constraint in the per port threshold register P0RLR, P1RLR and P2RLR and per queue rate limit register P0TQR0/1, P1TQR0/1 and P2TQR0/1.

Bandwidth Control Scheme

The bandwidth control logic will set the maximum bandwidth that each port/queue can support. The AX88782/AX88783 provides 12 bits programmable bandwidth setting from 0 to 12.5 M byte (100MBps) with 4K bytes per unit. In half duplex mode, the receiving side (ingress) will drop packets or send JAM if total receiving bytes exceed the bandwidth threshold. On the transmitting side (egress), if total transmit bytes goes over the threshold limit, then the AX88782/AX88783 will stop transmitting data out until rate limit timer is reach, and then transmit data again. The rate limit timer is located in P0RLTR/P1RLTR/P2RLTR and default value is one second. The default ingress and egress rate limit value is 0xFFF means no bandwidth constraint on ingress port and egress port.

Under full duplex mode, if the receiving data exceed the bandwidth threshold, the bandwidth control scheme will send the 802.3x PAUSE frame out if Flow Control function is enabled. If the receiving port turn off the flow control function, then the bandwidth control scheme will drop the exceeding packets if receiving packets exceed the bandwidth threshold. The AX88782/AX88783 also supports both ingress and egress per queues rate limit control from 0 to 100M Bps.

3.11 Security Operation

The AX88782/AX88783 provides the following types of security functions:
- Port-Based SA MAC Restriction
- IEEE 802.1x Port-Based Authorization
- 802.1Q VLAN Ingress Check
- Routing Table security handling
- Eight Special Security Entry Restriction

Port-based SA MAC Restriction
The AX88782/AX88783 provides source MAC address security support. When OneSAEn bits (LLCR [31:29]) is turned on, then the configure port will learn the first receiving packet's SA MAC address and stop learning. The switch core will only receive packets with the matched SA MAC address. Any packets with different SA MAC address will be dropped.

If LLCR [28:26] OneSARst bits is toggled from one to zero then the original secure SA MAC address will be reset and the configure port will learn a new source MAC address again if OneSAEn bits is still turn on and make sure the "StopLearn" bit in LGCR [5] is set to one when One SA function is enabled.

802.1x Port-Based Authorization
The AX88782/AX88783 provides a global 802.1x enable bit in LGCR [21] and per port 802.1x function enable bits in P0MCR/P1MCR/P2MCR [11] to turn on the 802.1x function. When 802.1x function is enabled, all the 802.1x frames will forward to host/CPU port. The AX88782/AX88783 will detect the 802.1x packet if the incoming packet's Ethernet Type field is 0x888E or DA MAC address is 0x0180C2000003 and forward the 802.1x control packet to CPU or host port.

Port State	Unauthorized	Authorized
Receive EAPOL packets to CPU with port information	Yes	Yes
Transmit EAPOL packets from CPU (CPU has the ability to specify which port to send EAPOL packets)	Yes	Yes
Receive normal packets	No	Yes
Transmit normal packets	No	Yes

Table 3 IEEE 802.1x Port-Based Authorization

Note - use Ethernet Type (0x888E) and special MAC Address = 0x0180C2000003 to identify EAPOL packets. That is, the AX88782/AX88783 only examine Ethernet type field or DA MAC address. If Ethernet type is 0x888E or DA MAC address is 0x0180C2000003, then it is EAPOL 802.1x control packet.

802.1Q VLAN Ingress Check
If "**IngressFilter"** bit in PVCR [10:8] is set to one, the VLAN ingress checker will verify if the packet's receiving port information belonging to the proper VLAN ID group. For example, if port 1 receives a tag frame with VID=4 and the VLAN Table VID=4 entry's port map information doesn't include Port 1, then if the IngressFilter function is enabled then this frame will be dropped.

Routing Table Security Handling:

1. Freeze Whole Routing Table

If the "StopLearn" bit in LGCR [5] is set to one, then all entries within the routing table will be freeze and stop learning new MAC address and aging function will also be disabled. This mode could be used if increased security is required.

2. Freeze Specific Entry inside Routing Table

If the routing table entry's "Static" bit is set to one, then the entry's MAC address will be fixed and will not be update by any new learned MAC address. This mode could be used if increased security on some special MAC address is required.

3. Filter DA/SA matched Packet

If the "FilterEn" bit in LGCR [4] is turn on, then the Filter_DA and the Filter_SA control function in the routing table entry will be enabled. Any receiving packets's DA MAC address that match with the routing table entry's MAC address has this Filter_DA bit set to one, then the forwarding engine will drop this packet. The same filter function can apply to the Filter_SA bit. If the receiving SA MAC address has the same MAC address entry inside the routing table and its Filter_SA bit is enabled then the forwarding engine will drop this packet.

The user can turn on DA or SA Match-and-Drop function on any entry within the routing table. For example, an Ethernet frame who's DA is 0x001234567800 will be dropped by the AX88782/AX88783 if the routing table has an entry with MAC address equal to 0x001234567800 and Filter_DA bit is set to one.

Eight Special Security MAC Entry Support

The AX88782/AX88783 provides additional eight special MAC entries (SM0CR ~ SM7CR) for extra security protection support. The user can use these eight special security MAC entries for their DA or SA Match-and-Drop filtering protection. For example, the forwarding engine will drop any Ethernet packets with SA MAC address equal to 0x055555555550 if one of the Security MAC Entries set to SA Match-and-Drop mode with MAC address programmed to be 0x055555555550. Please make sure Security MAC address and source port information is matched when programmed these security MAC address.

	Filter_DA	Filter_SA	Filter_Pair	Description
Security MAC0 ~ 7	1	0	0	Drop packet if DA match with Security MAC
Security MAC0 ~ 7	0	1	0	Drop packet if SA match with Security MAC
Security MAC0 Security MAC1	1 0	0 1	1 1	Drop packet if either DA match with Security MAC0 or SA match with Security MAC1 (must enable by pair)
Security MAC2 Security MAC3	1 0	0 1	1 1	Drop packet if either DA match with Security MAC2 or SA match with Security MAC3 (must enable by pair)
Security MAC4 Security MAC5	1 0	0 1	1 1	Drop packet if either DA match with Security MAC4 or SA match with Security MAC5 (must enable by pair)
Security MAC6 Security MAC7	1 0	0 1	1 1	Drop packet if either DA match with Security MAC6 or SA match with Security MAC7 (must enable by pair)
Security MAC0 Security MAC1	0 1	1 0	1 1	Drop packet if either SA match with Security MAC0 or DA match with Security MAC1 (must enable by pair)
Security MAC2 Security MAC3	0 1	1 0	1 1	Drop packet if either SA match with Security MAC2 or DA match with Security MAC3 (must enable by pair)
Security MAC4 Security MAC5	0 1	1 0	1 1	Drop packet if either SA match with Security MAC4 or DA match with Security MAC5 (must enable by pair)
Security MAC6 Security MAC7	0 1	1 0	1 1	Drop packet if either SA match with Security MAC6 or DA match with Security MAC7 (must enable by pair)

Table 4 Security MAC Filtering function table

Note1: When enable Filter_Pair function, please make sure MAC0 and MAC1 (or MAC2 and MAC3 or MAC4 and MAC5 or MAC6 and MAC7) 's Filter_Pair bit both set to one.

Note2: When there is any conflict between these eight security MACs and routing table entry, the security MAC will have higher priority than the routing table entry if the same MAC found on both location.

3.12 PPPoE/TCP/UDP/ICMP/IGMP/IPv4 Checksum Off-load Support

The AX88782/AX88783 has a built-in hardware TCP/IP check-sum off-load engine to help reduce the software loading and increase system overall performance. Fig 20 to Fig 27 is the list of all the supporting Ethernet frame type.

6 bytes	6 bytes	4 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	…..
DA	SA	802.1Q Tag (Optional)	88-64 PPPoE Type	PPPoE Version	PPPoE ID	PPPoE LEN	00-21 PPPoE Protocol	IPv4/TCP/UDP/ ICMP/IGMP Frame

Fig 20 PPPoE Frame Format

4 bits	4 bits	1 byte	2 bytes	2 bytes	3 bits	13 bits
0x4 IP Ver.	IHL	Type of Service	Total Length	Identification	Flags	Fragment Offset
1 byte		1 byte	2 bytes	4 bytes		
Time to Live		Protocol	Header Checksum	Source IP Address		
4 bytes				4 bytes		
Destination IP Address				Options (Optional)		

Fig 21 IPv4 Header

2 byte		2 bytes	4 bytes			
Source Port		Destination Port	Sequence Number			
4 bytes			6 bits	4 bits	6 bits	2 bytes
Acknowledgement Number			Offset	Reserved	Flags	Window
2 bytes		2 bytes	4 bytes			
Checksum		Urgent Pointer	Options (Optional)			

Fig 22 TCP Header

2 bytes	2 bytes	2 bytes	2 bytes
Source Port	Destination Port	Length	Checksum

Fig 23 UDP Header

1 byte	1 byte	2 bytes	……
Type	Code	Checksum	Other message-specific information….

Fig 24 ICMP Header

1 byte	1 byte	2 bytes	……
Type	Code	Checksum	Identifier Group Address Access Keys….

Fig 25 IGMP version 0 Header

4 bits	4 bits	1 byte	2 bytes	4 bytes
Version	Type	Unused	Checksum	Group Address

Fig 26 IGMP version 1 Header

1 byte	1 byte	2 bytes	4 bytes
Type	Max Response Time	Checksum	Group Address

Fig 27 IGMP version 2 Header

Checksum off-load Processing

1. The user can enable TOCR [5:0] and select which type of the protocol checksum offload function they need to reduce CPU loading.

TOCR[5]	TOCR[4]	TOCR[3]	TOCR[2]	TOCR[1]	TOCR[0]
PPPoE	IPv4	ICMP	IGMP	TCP	UDP

2. All packets receiving from host port (port 2) will be examined. If it is one of the selected packet type list on the above table, then the AX88782/AX88783 checksum engine will re-calculate a new CRC value on the fly and pass the calculated CRC value to the switch core.

3. The AX88782/AX88783 switch engine will forward the packet to destination ports and the checksum field will be replaced with the new calculated CRC value.

Checksum Off-load Filtering Function

The AX88782/AX88783 also provides checksum-offload filtering function on receiving port 0 and port 1. Any bad check-sum packets receiving from port 0 or port 1 hit the selected drop packet protocol defined in the TOCR register [13:8] will be dropped. Again, the user can select multiple protocols they like the hardware to filter the bad checksum packets before forward to the host or CPU port.

The TOCR register bit [8] to bit [13] defines which type of the protocol packet to be dropped if the check-sum value is wrong.

TOCR[13]	TOCR[12]	TOCR[11]	TOCR[10]	TOCR[9]	TOCR[8]
PPPoE	IPv4	ICMP	IGMP	TCP	UDP

The AX88782/AX88783 will calculate checksum on the fly on the receiving side and drop the bad checksum packets on forwarding engine to reduce CPU or host port loading. The Fig 28 shows the AX88782/AX88783 checksum offload insertion and filtering flow. The AX88782/AX88783 also provides a per-port drop counter P0RDCR and P1RDCR.

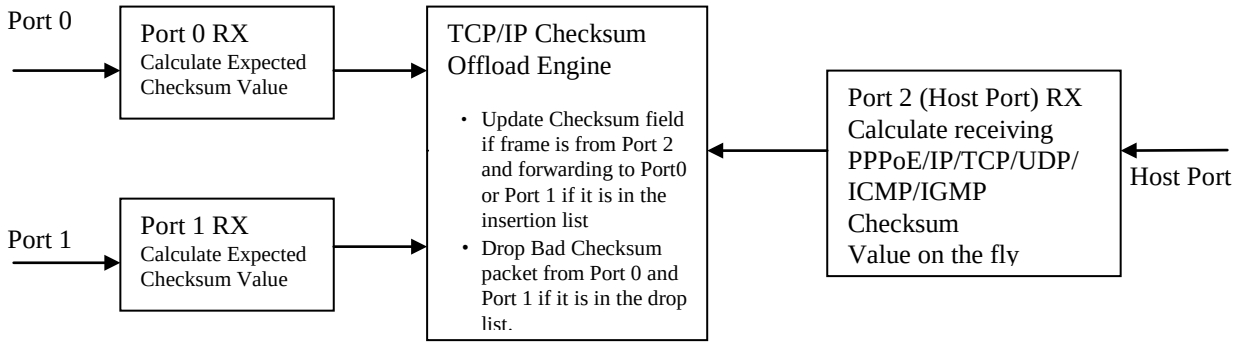


Fig 28 TCP/IP Checksum off-load Processing

The checksum off-load logic inside the AX88782/AX88783 will not able to support IP fragmentation and RFC1042 SNAP encapsulation format.

3.13 RMON Counter Support

The AX88782/AX88783 provides 30 counters to statistic events in each port for remote network monitor. The counters are listed below. All counters are 32-bit wide except the Rx Byte counter and the TX Byte counter, which are 64-bit. The priority of a read counter request from the host port is always higher than the updating process. All counters will be automatically cleared in system-reset period or by setting the register RCR bit [4] ClrAllCounter to one.

Offset	Counter	Description
0x00	Rx Packet Counter	The total number of packets received (include bad packets)
0x01	Rx Good Packet Counter	The total number of good packets received.
0x02	Rx Byte Counter (low 32 bit)	The total number of bytes received (include bad packets).
0x03	Rx Byte Counter (high 32 bit)	
0x04	Rx Broadcast Packet Counter	The total number of good broadcast packets received.
0x05	Rx Multicast Packet Counter	The total number of good multicast packets received.
0x06	Rx PAUSE Frame Counter	The total number of PAUSE frames received.
0x07	Rx Packet Length Counter 1	The total number of packets received that length is less than 64 bytes (include bad packets).
0x08	Rx Packet Length Counter 2	The total number of packets received that length is 64 bytes (include bad packets).
0x09	Rx Packet Length Counter 3	The total number of packets received that length is between 65 bytes and 127 bytes (include bad packets).
0x0A	Rx Packet Length Counter 4	The total number of packets received that length is between 128 bytes and 255 bytes (include bad packets).
0x0B	Rx Packet Length Counter 5	The total number of packets received that length is between 256 bytes and 511 bytes (include bad packets).
0x0C	Rx Packet Length Counter 6	The total number of packets received that length is between 512 bytes and 1023 bytes (include bad packets).
0x0D	Rx Packet Length Counter 7	The total number of packets received that length is between 1024 bytes and maximum bytes (include bad packets).
0x0E	Rx Packet Length Counter 8	The total number of packets received that length is longer maximum bytes (include bad packets).
0x0F	Rx CRC Error Packet Counter	The total number of packets with CRC error received.
0x10	Rx Alignment Error Packet Counter	The total number of packets with Alignment error received.
0x11	Fragment Error Counter	The total number of packets received that are less than 64 bytes, but has an either CRC error or Alignment Error.
0x14	Tx Packet Counter	The total number of packets transmitted or aborted.
0x15	Tx Good Packet Counter	The total number of good packets transmitted successfully.
0x16	Tx Byte Counter (low 32 bit)	The total number of bytes transmitted or aborted.
0x17	Tx Byte Counter (high 32 bit)	
0x18	Tx Broadcast Packet Counter	The total number of good broadcast packets transmitted successfully.
0x19	Tx Multicast Packet Counter	The total number of good multicast packets transmitted successfully.
0x1A	Tx PAUSE Frame Counter	The total number of PAUSE frames transmitted.
0x1B	Tx Collision Counter	The total number of collisions occurred.
0x1C	Tx Packet with one Collision Counter	The total number of packets transmitted successfully which experienced one collision.
0x1D	Tx Packet with Multiple Collision Counter	The total number of packets transmitted successfully which experienced multiple collisions.
0x1E	Tx Excessive Collision Counter	The total number of packets aborted due to experienced excessive collisions.
0x1F	Tx Late Collision Counter	The total number of packets experienced late collisions.

Table 5 RMON Counter Mapping Table

RMON counter access

The AX88782/AX88783 provides indirect access to all the RMON counters. The register RCR [14:8](RmonAddr [6:0]) provides Port ID number (RmonAddr [6:5]) and the RMON counter offset address (RmonAddr [4:0]) and the register RDR provides the RMON data information. All RMON counters can be clear through RCR [4] RMON counter clear bit which is write one clear bit.

For example, if the user likes to read the port 1 RX good packet counter value

1. Write 0x0000A100 to the RCR register
2. Read RDR register to get the port 1 RX good packet counter value

3.14 Layer 2/3/4 Sniffer Function Support

The AX88782/AX88783 provides multi-layer sniffer function include source port or destination port, Layer 2 DA or SA MAC address, Ethernet Packet Type, VLAN ID, Layer 3 IPv4 or IPv6 protocol and layer 4 IPv4 or IPv6 TCP/UDP source port number and destination port number. The user can program SFCR0 ~ SFCR1, define the sniffer port and monitor all kind of sniffer packets in-and–out of switch engine from the assigned sniffer port.

The eight extra security MAC registers defined in SM0CR ~ SM7CR can also provide the sniffer DA/SA match function by enabled sniffer_DA, sniffer_SA or sniffer_Pair bits which is similar to the filter function list on the table 4.

The AX88782/AX88783 can select the following types of packet and copy these user specify packets to the sniffer port. Please reference SFCR0/SFCR1/SFCR2 register descriptions for more detail sniffer function usage.

1. Source port
2. Destination port
3. Source and Destination Port
4. DA MAC match
5. SA MAC match
6. Both DA MAC and SA MAC match
7. VLAN VID [11:0] match (user-defined sniffer VID, SFCR1 [27:16])
8. Layer 2 Ethernet Packet Type Sniffer Function

There are seven pre-defined Ethernet packet types and one user defined Ethernet packet to select.

Layer 2 Sniffer Type (SFCR0[31:24])	Ethernet Type Field	Protocol Type
[0]	0x0806	ARP
[1]	0x8035	RARP
[2]	0x8847 or 0x8848	MPLS Unicast MPLS Multicast
[3]	0x888E	802.1X
[4]	0x8137	IPX/SNAP
[5]	0x8040	NetBIOS
[6]	0x8863(default)	User -defined in USTR [15:0] (Default Type: PPPoE Discovery)
[7]	0x8864	PPPOE Session

Table 6 Layer 2 Sniffer Table

9. Layer 3 IPv4 Protocol Sniffer Function

IPv4 Sniffer Type (SFCR1[7:0])	Protocol Index	Protocol Type
[0]	ALL (Ethernet Type=0x0800)	ALL IPv4 Packets
[1]	6	TCP

[2]	17	UDP
[3]	89	OSPF
[4]	46	RSVP
[5]	115(default)	User-defined in USTR [23:16] (Default: L2TP)
[6]	1	ICMPv4
[7]	2	IGMP

Table 7 IPv4 Sniffer Table

10. Layer 3 IPv6 Protocol Sniffer Function

IPv6 Sniffer Type (SFCR1[14:8])	Protocol Index	Protocol Type
[0]	ALL (Ethernet Type=0x86DD)	ALL IPv6 Packets
[1]	6	TCP
[2]	17	UDP
[3]	89	OSPF
[4]	46	RSVP
[5]	115(default)	User -defined in USTR [23:16] (Default: L2TP)
[6]	1	ICMPv6

Table 8 IPv6 Sniffer Table

11. Layer 4 IPv4/IPv6 TCP/UDP Source Port or/and Destination Port number match
- Sniffer Source Port
- Sniffer Destination Port
- Sniffer both Source and Destination Port

The AX88782/AX88783 only supports one IPv4/IPv6 TDP/UDP User-defined Source Port and Destination Port number to sniffer, which is located in SFCR2 [15:0] and SFCR2 [31:16].

The SFCR0 Sniffer Configuration register is list below:

[0]	[1]	[2]	[3]	[4]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]
Source Port	Dest. Port	SA Match	DA Match	VID Match	Packet Type Match	IPv4 TCP Src Match	IPv4 TCP Dst Match	IPv4 UDP Src Match	IPv4 UDP Dst Match	IPv6 TCP Src Match	IPv6 TCP Dst Match	IPv6 UDP Src Match	IPv6 UDP Dst Match

[15]	[16:17]	[18]	[19]	[20]	[21]	[22]	[23]
Sniffer Enable	Sniffer Port	Source Port 0	Source Port 1	Source Port 2	Dest Port 0	Dest Port 1	Dest Port 2

How to set up the sniffer function?
1. Bit [15] Sniffer Enable need to be one
2. Define the sniffer port location in bit [17:16] where all the matched packets will cope to this sniffer port
3. If [6] is set to one then check the following options
   - SFCR0 L2_Type[7:0]: select multiple Layer 2 Ethernet type of packets from Table 6.
   - SFCR1 IPv4_Type[7:0]: select multiple IPv4 protocols from Table 7.
   - SFCR1 IPv6_Type[7:0]: select multiple IPv6 protocols from Table 8.
4 If bit [4] is set to one then check SFCR1 SnifferVID for VLAN VID comparison
5 Sniffer equation: (AND any one from [0:1], [2:3], [4]) AND [6] AND (AND any one from [7:14]) AND (AND any one from [18:23])

Note1: Any zero on Bit [0:4] and [6] will be removed from of this AND equation.
Note2: Any zero on [18:23] will be removed from the AND function
Note3: Only one source port number and destination number is supported. The IPv4 source port and destination port function will has higher priority than the IPv6 if both turn on at the same time.

3.15 IPv4 IGMP and IPv6 ICMP/MLD Snooping

The AX88782/AX88783 supports IPv4 IGMP (Internet Group Management Protocol) and IPv6 ICMP MLD (Multicast Listener Discovery) snooping function.

IPv4 IGMP Snooping
The LGCR [13] IGMP_En need to set to one to enable IPv4 IGMP snooping function. If LGCR [14] IGMP_Mode is set to one then all receiving IPv4 IGMP packets will only forward to CPU port. If LGCR [14] IGMP_Mode is set to zero then the switch engine will make a extra copy of the packet to CPU port plus normal forwarding process.

IPv6 Snooping
The ITCR [7: 2] IPv6_Snooping configuration register defines a few different kinds of IPv6 snooping function. The bit [7] IPv6 snooping enable bit need to set to one if any of the configure bit from bit [2] to bit [6] is turn on. Please reference ITCR register for further detail.

4 bits	**8 bits**	**20 bits**	
Version	Traffic Class	Flow Label	
2 bytes		**1 byte**	**1 byte**
Payload Length		Next Header	Hop Limit
4 bytes			
Source IP Address [127:96]			
Source IP Address [95:64]			
Source IP Address [63:32]			
Source IP Address [31:0]			
Destination IP Address [127:96]			
Destination IP Address [95:64]			
Destination IP Address [63:32]			
Destination IP Address [31:0]			
Next header1 (If next header=0)	Payload		

Fig 29 IPv6 Frame Format

Next Header/Next Header1	Protocol
0	Hop-by-hop Options (NOTE: special processing)
1	ICMPv4
43	Routing (Type0)
44	Fragment
51	Encapsulating Security Payload
58	ICMPv6
60	Destination Options

Table 9 Next Header Table

IPv6/ICMPv4 Multicast Snooping
If ITCR bit [2] and bit [7] both set to 1 and the following conditions match then the packet will forward to CPU port.

- IPv6 Multicast packet
- Next header = 1 or next header =0 and next header1 = 1
- Hop Limit =1

IPv6/ICMPv6 Multicast Snooping (MLD Snooping)
If ITCR bit [3] and bit [7] both set to 1 and the following conditions match then the packet will forward to CPU port.
- IPv6 Multicast packet
- Next header = 58 or next header =0 and next header1 = 58
- Hop Limit =1

IPv6/ICMPv4 Snooping
If ITCR bit [4] and bit [7] both set to 1 and the following conditions match then the packet will forward to CPU port.
- IPv6 packet
- Next header = 1 or next header =0 and next header1 = 1
- Hop Limit =1

IPv6/ICMPv6 Snooping
If ITCR bit [5] and bit [7] both set to 1 and the following conditions match then the packet will forward to CPU port.
- IPv6 packet
- Next header = 58 or next header =0 and next header1 = 58
- Hop Limit =1

IPv6/Miscellaneous Snooping
If ITCR bit [6] and bit [7] both set to 1 and the following conditions match then the packet will forward to CPU port.
- IPv6 packet
- Next header = 43, 44, 50, 51 and 60 or next header =0 and next header1 = 43, 44, 50, 51 and 60
- Hop Limit =1

3.16 Wake-On-LAN Function Support

The AX88782/AX88783 supports four different kinds of wake-up mechanism: Link-Status Change, GPIO Wake-up, Magic Packet and Microsoft Wake-Up Frame detection. The user can program the WCR register to configure any of these four wake-up mechanisms on Port 0 and/or Port 1. The AX88782/AX88783 provides the PME (Power Management Event) output pin to pass the information to host processor. The polarity of PME signal can also configure in WCR [22:20]. They are active low, level high, level low, pulse high and pulse low to select. Please reference 3.21 GPIO section for GPIO wakeup support.

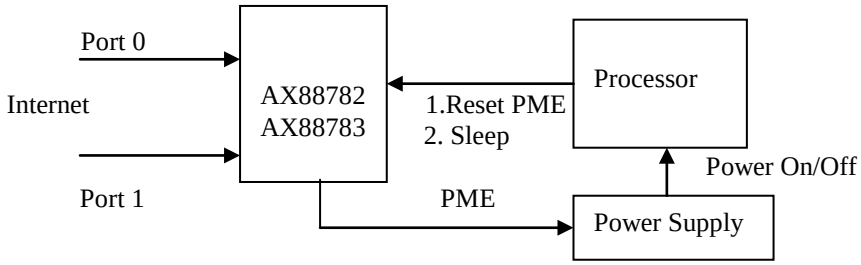


Fig 30 Wake-On -LAN Application

Remote Wake-up Process (Microsoft Wake-up Frame Mode)
The Fig 30 shows one of the Wake-On-LAN applications with the power supply control. The AX88782/AX88783 can detect the wake up event and the PME signal will trigger the power supply to turn on core process and bring up the whole system remotely.

The user can enable Microsoft Wake-up function, set the PME signal polarities and enable wakeup frame detection mode first. Port 0 and Port 1 will detect Microsoft wake-up frame from the incoming traffic. When receiving the expected wake-up frame pattern, the AX88782/AX88783 will toggle the PME signal. Once the power supply is up, the processor or the system will be powered up and re-initialize the AX88782/AX88783 to normal state. The processor can reset the PME

signal and programmed the AX88782/AX88783 back to the wakeup frame detection mode. And the power supply will turn off the core power automatically.

Sleep Mode Process

The processor can turn on sleep mode by writing one to the register WCR bit [19] to clear the sleep mode status and write one to WCR bit [17] to enter the sleep mode. The AX88782/AX88783 will then disable the internal clock and power down both internal PHY and stay in the power saving state. The host processor can write address 0x1F4 with any value to exit sleep mode and back to normal state.

Link-Status Change Detection

There are two internal PHY built-in the AX88782/AX88783. Any time when the internal PHY's PSR LinkDone0 or LinkDone1 status changes (one-to-zero or zero-to-one) and the Link-Status Change Wake-up option in the WCR register bit [0] for port 0 or bit [5] for port 1 is enabled, then the AX88782/AX88783 will detect a link-status change wakeup event and generate a valid PME signal to inform the host processor.

Magic Packet Detection

The Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a network. The user can turn on Magic Packet enable bit for port 0 and port 1 from the WCR register bit [1] and bit [6]. Once the AX88782/AX88783 has been put into the Magic Packet mode, it scans all incoming Ethernet frames addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the Ethernet frame, such as SOURCE MAC ADDRESS, DESTINATION MAC ADDRESS (which may be the receiving station's IEEE address or a MULTICAST address which includes the BROADCAST address), and good CRC. The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler.

The synchronization stream is defined as 6 bytes of 0xFF. The device will also accept a BROADCAST frame, as long as the 16 duplications of the IEEE address matches the address of the machine to be awakened. If the IEEE address for a particular node on the network is 0x112233445566, then the AX88782/AX88783 scans for the data sequence (Assuming an Ethernet Frame):

DA + SA + Misc. + FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 + Misc. + CRC.

There are no other restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet, an IPX packet, etc. The frame may be bridged or routed across the network, without affecting its ability to wake up a node at the destination of the frame.

If the AX88782/AX88783 scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the controller detects the data sequence, however, then it alerts the PC's power management circuitry to wake up the system.

A Wake-up frame is a special data packet containing the Ethernet address of the remote network card. Somewhere in this frame should exist a byte stream (magic sequence) composed by, at the least, 16 times the repetition of the Ethernet address and preceded by a synchronization stream of 6 bytes of 0xFF.

The following steps provide a simple way to set-up Magic Packet Detection process.

1. Enable EnMagicPacket bit in WCR bit [1] for Port 0 and bit [6] for Port 1
2. Program expected repeat MAC address for Port 0 (P0DAR0 [31:0] and P0DAR1 [15:0]) and for Port 1 (P1DAR0 [31:0] and P1DAR1 [15:0])

Microsoft Wake-up frame Detection

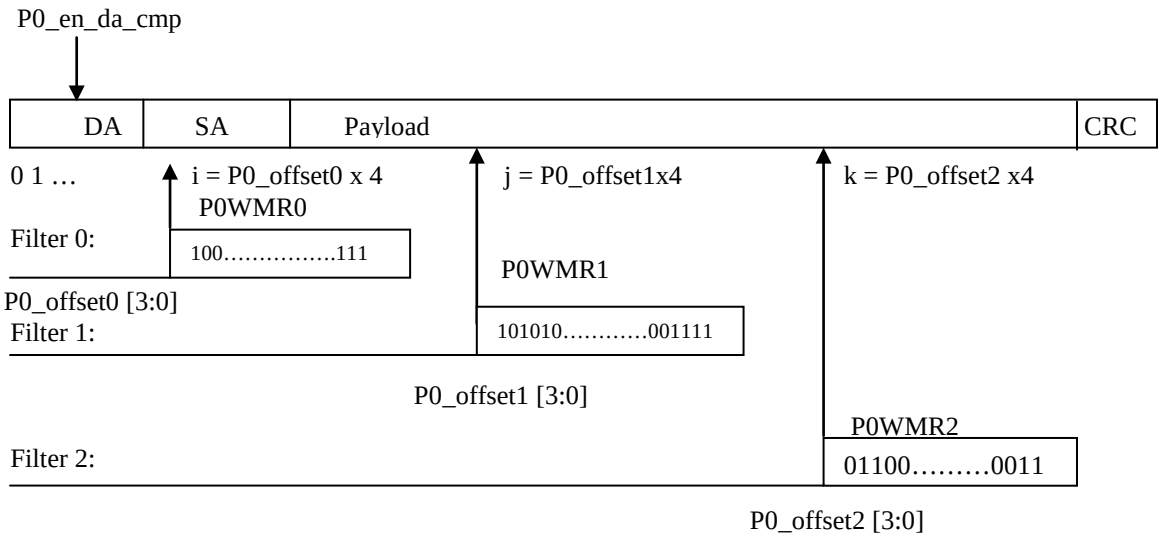
The AX88782/AX88783 supports three programmable filter rules that help to locate the expected pattern within the receiving packet. If the Microsoft wakeup frame detection mode is enabled (in D1 state), the remote wakeup function receives all Ethernet frames and checks each frame against the enabled filter patterns and recognizes the frame as a remote wake-up frame if it passes the MAC address filtering and CRC value match.

The AX88782/AX88783 uses a programmable byte mask and a programmable pattern offset for each of the three supported filters. The AX88782/AX88783 also provides an option to cascade three programmable filters together. The three pattern detectors can operate simultaneously or sequentially based on the cascade register within the WCR Encascade0 [1:0] or Encascade1 [1:0].

The byte mask is a 32-bit field that specifies whether the next 32 contiguous bytes right after the offset location should be calculated CRC value or not. If bit [j] in the byte mask is set to one, then the detection logic will calculate the byte [offset +j]'s CRC value. Once the detection logic scans through all the mask location and calculates all the mask bytes' CRC32 value. The calculated CRC value will be compare against to the expected CRC value in P0WCR and P1WCR's rgi_crc value to decide if the receiving frame has the expected pattern.

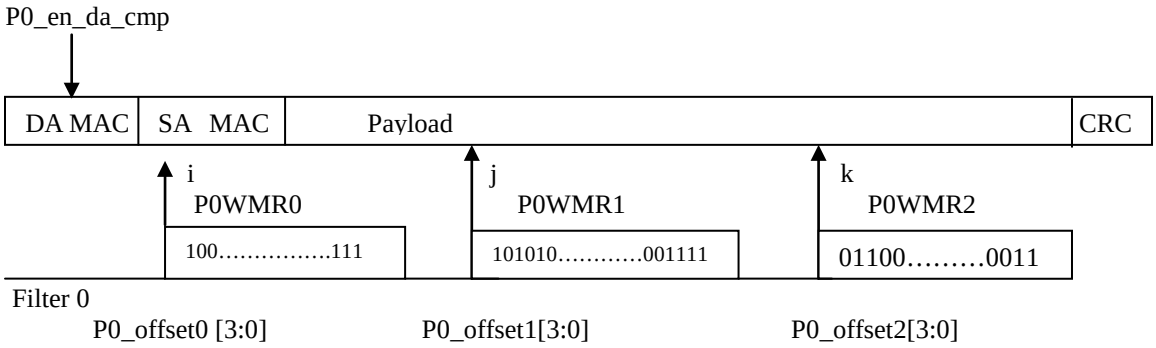
The WSR register defines both port 0 and port 1 three offset index registers. Each unit in the offset register represents a double word offset (four bytes). For example, if P0_offset0 is 0x1 then the first mask byte will start from the fourth byte location. If filter 0 and filter 1is cascade and P0_offset1 is 0x2 then the second mask byte will start from the 44th byte location. (4x1+ 32 + 2x4 = 44)

1) If En_cascade0 [1:0] = 00 (No cascade)



1. First, make sure receive CRC is good.
2. If WSR [15] P0_en_da_cmp is set to one, then compare receive DA MAC [47:0] against expect MAC [47:0] in P0DAR0 and P0DAR1 register value.
3. The three wake-up filter index will move to its offset starting position i , j, k.
   Where i = P0_offset0 [3:0] x 4, j =P0_offset1 [3:0] x 4 and k =P0_offset2 [3:0] x 4
4. From i, j, k to i+31, j+31, k+31 byte position, scan through the next 32 bytes data and calculate CRC32 if corresponding mask bit is set to one. For example if Port 0 P0WMR make register is 0xC000_0003, then filter0 will only calculate i, i+1, i+30, and i+31 CRC value.
5. Compare rgi_crc register (P0WCR) against calculated CRC value from filter 0, 1, and 2.
6. If any one matches, then it is consider as remote wake-up frame and the AX88782/AX88783 will enable PME event signal.

2) If En_cascade0 [1:0] = 11 (cascade all three filters together)



1. First make sure receive CRC is good.
2. If WSR [15] P0_en_da_cmp is set to one, then compare receive DA MAC [47:0] against expect MAC [47:0] in P0DAR0 and P0DAR1 register value.
3. The filter index will move to its offset starting position i, j, k. where i = P0_offset0 [3:0] x 4, j = i + 32 + P0_offset1 [3:0] x 4 and k = j + 32 + P0_offset2 [3:0] x 4
4. From i, j, k to i+31, j+31, k+31 byte position, scan through the next three 32 byte data and calculate CRC32 if corresponding mask bit is set to one. For example if Port 0 address 10Ch make register is 0xC000_0003, then filter0 will only calculate i, i+1, i+30, and i+31 CRC value.
5. Compare rgi_crc register (P0WCR) against the calculated CRC value from filter 0.
6. If calculated CRC matches the CRC register value, then it is considered a remote wake-up frame and the AX88782/AX88783 will enable the PME event signal.

The user can use the AX88782/AX88783's cascade function, en_da_cmp DA match function and the three mask registers to generate any kind of match pattern they need and create their own wake-up frame.

3.17 Power Management

The AX88782/AX88783 supports power-saving modes to allow applications to minimize power consumption. There is one normal operation power state, D0 and two power saving states: D1 wake-up mode, and D2 sleep mode. The Wake-On-LAN Configuration Register (WCR) is able to enable these power management modes. In D1 power saving state, the AX88782/AX88783 supports Wake-on-LAN function. In D2 power saving state, the AX88782/AX88783 will power down all functional block and clocks to minimize power consumption. After a wakeup event, the AX88782/AX88783 will revert back to the normal operation power state.

When the AX88782/AX88783 is in either D1 or D2 power saving mode, the host port can write "Clear Sleep Mode Register" (SMER) and return the AX88782/AX88783 back to the D0 state. The Power is reduced to various modules by disabling the clocks as outlined in the table below.

AX88782/ AX88783	D0 (Normal Mode)	D1 (Wake-up Mode)	D2 (Sleep Mode)
Core Clock	On	On	Off
Interface	On	Off	Off
WOL Logic	On	Rx Block On	Off
PHY	On	On	Off

Table 10 Power Management Statuses

3.18 Auto-Polling Function

The AX88782/AX88783 supports PHY management through the serial MDIO/MDC interface. That is, the AX88782/AX88783 accesses related PHY registers via MDIO/MDC interface after power on reset. The AX88782/AX88783 will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface. All the polling status will be automatically update in the register P0MCR and P1MCR's MAC_enable, Speed, Full_duplex and FlowCtrl_ON location if the auto-polling function is enable in the ACR register.

3.19 Port Mirroring

Port mirroring is a function that mirrors or duplicates traffic from one "mirror port" to a "target port". The mirror or target port mirroring can be set up for each port individually to mirror either incoming packets or outgoing packets. Incoming and outgoing traffic need not be mirrored to the same port. Unidirectional traffic on a port can only be mirrored to the target port. Only correct packets that would normally be handled by the AX88782/AX88783 will be mirrored. Packets with CRC errors and collision fragments etc are **not** mirrored.

- **Ingress mirroring:** Traffic received on a port will be sent to the mirror port as well as to any other addressed port.
- **Egress mirroring:** Traffic sent out on a port will also be sent to the mirror port.

3.20 Serial EEPROM Protocol

The serial EEPROM interface is responsible for reading configuration data automatically from the external serial EEPROM or writing data from internal register into external serial EEPROM. The AX88782/AX88783 can automatically be configured from an external serial EEPROM. If a properly configured EEPROM is detected by the AX88782/AX88783 at power-up, hard reset or host set a reload EEPROM request, the constants of EEPROM data will be auto loading to internal register address space automatically. The EEPROM size is detected during the reset cycle from pull-up/pull-down state found on CS and SK pins.

EEPROM size	SK	CS
N/A (default)	PD	PD
1K-bit (93C46)	PD	PU
2K-bit (93C56)	PU	PD
4K-bit (93C66)	PU	PU

Table 11 EEPROM Size mapping (PD: tie a 4.7K ohm pull-down resistor to ground PU: tie a 4.7K ohm pull-up resistor to VCC)

EEPROM Data Format:

Address [9:2]	Data [31:24]	Data [23:16]	Data [15:8]	Data [7:0]

EEPROM Address	EEPROM Contents
0	Address [9:2] (1St Write Command)
1	Data [31:24]
2	Data [23:16]
3	Data [15:8]
4	Data [7:0]
5	Address [9:2] (2nd Write Command)
6	Data [31:24]
7	Data [23:16]
8	Data [15:8]
9	Data [7:0]
:	:
:	:
:	:

All the registers within the AX88782/AX88783 are 32-bit wide that's why the EEPROM data format includes an address [9:2] and four bytes of the data. The AX88782/AX88783 will auto-configure the internal registers based on the write commands in the EEPROM contents after the hardware reset operation or the reload EEPROM operation. The Address [9:2] field defines the internal register address [9:2], and the 4-byte data fields define the write data value. For example, when the Address [9:2] = 0x8C and the Data [31:0] = 0x12345678, the AX88782/AX88783 will write 0x12345678 into the address 0x230 P0ADR0 register.

Note: If the data format is "00 -- -- -- --" and "FF -- -- -- --" then they will be translated to wait state command. The address [9:2] = 0x00 and 0xFF are reserved. The AX88782/AX88783 will ignore this write command and continue move to next write command. Normally, the EEPROM reader will read through all 1K/2K/4K pre-defined address space. There is a speed-up end of the EEPROM read process command by assign the address [9:2] to 0x00 and the Data [31:0] to 0x84149435 at the end of the last valid write command.

The following is a sample EEPROM code to set up the internal PHY0 and PHY1 function.

01 11 01 10 01 //Turn On PHY0 and PHY1 (PCR)
37 03 04 02 01 //Enable LED function (LCR)
0F 90 18 80 2C //Set Phy0 Reg24.2=1 internal PHY Link speed-up (MRCR)
00 00 00 00 00 // Wait
0F 91 18 80 2c //Set Phy1 Reg24.2=1 internal PHY Link speed-up (MRCR)
00 00 00 00 00
0F 90 10 10 00 //Set Phy0 Reg16.12=1 internal PHY Link speed-up (MRCR)
00 00 00 00 00
0F 91 10 10 00 //Set Phy 1 Reg16.12=1 internal PHY Link speed-up (MRCR)
00 00 00 00 00
0F 90 04 05 E1 //Set Phy0 Pause capability (MRCR)
00 00 00 00 00
0F 91 04 05 E1 //Set Phy1 Pause capability (MRCR)
00 00 00 00 00
0F 90 00 33 00 //Restart Phy0 Auto-negotiation (MRCR)
00 00 00 00 00
0F 91 00 33 00 //Restart Phy1 Auto-negotiation (MRCR)
00 00 00 00 00
50 33 00 11 10 //Auto polling enable (ACR)
00 00 00 00 00 / or apply "00 84 14 94 35" End Command here to stop process
: : : : :
00 00 00 00 00 // End of 1K/2K/4K pre-defined EEPROM address space

3.21 GPIO Interface Support (Only for AX88783)

The AX88783 has an optional feature to support 6 GPIO, 5 GPI and 1 GPO function through multi-functional pin out on Port 0 MII interface when Port 0 MII/RMII/RevMII/RevRMII function is disabled and internal PHY is enabled.

3.21.1 GPIO Interface

The AX88783 is able to support up to six GPIO pin-outs. Each GPIO is able to trigger interrupt event and wakeup event to external CPU.

GPIO	GPIO Enable	Input	Output	Output Enable	Interrupt Enable	Interrupt Mask	Interrupt Status	Interrupt Select
GPIO0	GPIOCR1[16]	GPIOCR1[0]	GPIOCR2[0]	GPIOCR2[16]	GPIOCR3[0]	GPIOCR4[16]	GPIOCR4[0]	GPIOCR3[16]
GPIO1	GPIOCR1[17]	GPIOCR1[1]	GPIOCR2[1]	GPIOCR2[17]	GPIOCR3[1]	GPIOCR4[17]	GPIOCR4[1]	GPIOCR3[17]
GPIO2	GPIOCR1[18]	GPIOCR1[2]	GPIOCR2[2]	GPIOCR2[18]	GPIOCR3[2]	GPIOCR4[18]	GPIOCR4[2]	GPIOCR3[18]
GPIO3	GPIOCR1[19]	GPIOCR1[3]	GPIOCR2[3]	GPIOCR2[19]	GPIOCR3[3]	GPIOCR4[19]	GPIOCR4[3]	GPIOCR3[19]
GPIO4	GPIOCR1[20]	GPIOCR1[4]	GPIOCR2[4]	GPIOCR2[20]	GPIOCR3[4]	GPIOCR4[20]	GPIOCR4[4]	GPIOCR3[20]
GPIO5	GPIOCR1[21]	GPIOCR1[5]	GPIOCR2[5]	GPIOCR2[21]	GPIOCR3[5]	GPIOCR4[21]	GPIOCR4[5]	GPIOCR3[21]

Table 12 GPIO Configuration Table

When GPIO Enable is set to one, GPIO pin will be configured to output pin and pass output data from register to pin if the correspondent Output Enable is set to one. Otherwise, if output enable is set to zero then GPIO pin will consider as input pin and pass the pin data save to input register.

The GPIO pins support the interrupt function if the interrupt enable bit and GPIO enable bit both set to one. The Interrupt Select register will define interrupt polarity active high if set to one or active low if set to zero. The interrupt mask register is able to mask the interrupt if the mask bit is set to one. The interrupt status value can read out from the Interrupt Status register and write one to clear the interrupt status bit.

The AX88783 also supports GPIO Wakeup function. The wakeup function can be enabled if the wakeup enable bit and GPIO enable bit both set to one. And the wakeup status bit will show if the wakeup event is detected or not. The wakeup event can be configured from the Wakeup Select Register. If the Wakeup Select bit is set to 00 then the wakeup event will be triggered if detect a falling edge. If the Wakeup Select is configured to 01 then any rising edge will trigger wakeup event.

GPIO	Wakeup Enable	Wakeup Status	Wakeup Select
GPIO0	GPIOWR[0]	GPIOWR[24]	GPIOWR[9:8]
GPIO1	GPIOWR[1]	GPIOWR[25]	GPIOWR[11:10]
GPIO2	GPIOWR[2]	GPIOWR[26]	GPIOWR[13:12]
GPIO3	GPIOWR[3]	GPIOWR[27]	GPIOWR[15:14]
GPIO4	GPIOWR[4]	GPIOWR[28]	GPIOWR[17:16]
GPIO5	GPIOWR[5]	GPIOWR[29]	GPIOWR[19:18]
			Wakeup Select Function: 00: Falling edge 01: Rising edge 10: Level Low 11: Level High

Table 13 GPIO Wakeup Configuration Table

3.21.2 GPO Interface

The AX88783 supports one GPO Pin outs. When GPO Enable bit (GPIOCR1 [22]) is set to one, GPO pin drive data from output register (GPIOCR2 [6]) to GPO pin if GPO output enable bit (GPIOCR2 [22]) is set to one.

3.21.3 GPI Interface

The AX88783 is able to support up to five GPI function pins. Each GPI is able to trigger interrupt event to external CPU.

GPI	GPI Enable	Input	Interrupt Enable	Interrupt Mask	Interrupt Status	Interrupt Select
GPI0	GPIOCR1[24]	GPIOCR1[8]	GPIOCR3[8]	GPIOCR4[24]	GPIOCR4[8]	GPIOCR3[24]
GPI1	GPIOCR1[25]	GPIOCR1[9]	GPIOCR3[9]	GPIOCR4[25]	GPIOCR4[9]	GPIOCR3[25]
GPI2	GPIOCR1[26]	GPIOCR1[10]	GPIOCR3[10]	GPIOCR4[26]	GPIOCR4[10]	GPIOCR3[26]
GPI3	GPIOCR1[27]	GPIOCR1[11]	GPIOCR3[11]	GPIOCR4[27]	GPIOCR4[11]	GPIOCR3[27]
GPI4	GPIOCR1[28]	GPIOCR1[12]	GPIOCR3[12]	GPIOCR4[28]	GPIOCR4[12]	GPIOCR3[28]

Table 14GPI Configuration Table

When the GPI Enable bit is set to one, the GPI pin will be configured as an input pin and load the data from pin to internal input data register. The GPI pin supports interrupt function if the interrupt enable bit and the GPI enable bit both set to one. The Interrupt Select register in GMCR bit [27] Int_hl defines the interrupt polarity active high if set to one or active low if set to zero. The interrupt mask register in ISMR is able to mask the interrupt if the mask bit is set to one. The interrupt status value can read out from the Interrupt Status register in ISMR and write one to clear the interrupt status bit.

3.22 CPU Interface Protocol

The AX88782/AX88783 defines a simple CPU interface protocol to transfer packet in and out the AX88782/AX88783.

CPU-to-Switch Packet Header Format (CPU write packet to the AX88782/AX88783 host port)

31 ~ 16	15	14~13	12	11	10 ~ 0
Bit [15:0] inverse	PID_En	PID	0	0	Packet Length

Bit	Name	Description
[10:0]	Packet Length	12 ~ 2047 Bytes. The internal hardware will add padding if the packet size is less than 64 bytes.
[14:13]	PID [1:0]	Port ID 00: Assign forward to Port 0 01: Assign forward to Port 1 10: Reserved 11: The forwarding engine makes its own decision
[15]	PID_En	When set to 1, the AX88782/AX88783 will add an extra byte of the Port ID information at the end of payload before CRC field. Otherwise, the software will insert PID information.
[31:16]	Header Error Check	The CPU will need to check if bit [31:16] value equal to the invert of bit [15:0]. If error is detected, CPU will need to write zero into CIRR [26] register to clear internal FIFO.

Switch-to-CPU Packet Header Format (CPU read packet from the AX88782/AX88783 host port)

31 ~ 16	15	14~12	11	10 ~ 0
Bit [15:0] inverse	Source Port	Packet Type	0	Packet Length

Bit	Name	Description
[10:0]	Packet Length	64 ~ 2047 Bytes.
[14:12]	Packet Type	Receiving Packet Type

		001: BPDU Packet (DA MAC address 0x0180_C200_0000) 010: LACP Packet (DA MAC address 0x0180_C200_0002) 011: GARP Packet (DA MAC address 0x0180_C200_0010) 100: GMRP (DA MAC address 0x0180_C200_0020) 101: GVRP (DA MAC address 0x0180_C200_0021) 110: 802.1X (DA MAC address 0x0180_C200_0003) 111: Special MAC (DA MAC address 0x0180_C200_0000 ~ 0x0180_C200_00FF and not include packet type 001 to 110) 000: Normal Packet
[15]	Source Port	Packet Source Port ID 0: From Port 0 1: From Port 1
[31:16]	Header Error Check	The CPU will need to check if bit [31:16] value equal to the invert of bit [15:0]. If error is detected, CPU will need to write zero into CIRR [27] register to clear internal FIFO.

Procedure to start the read or write transaction will be follow the three steps in Fig 31.

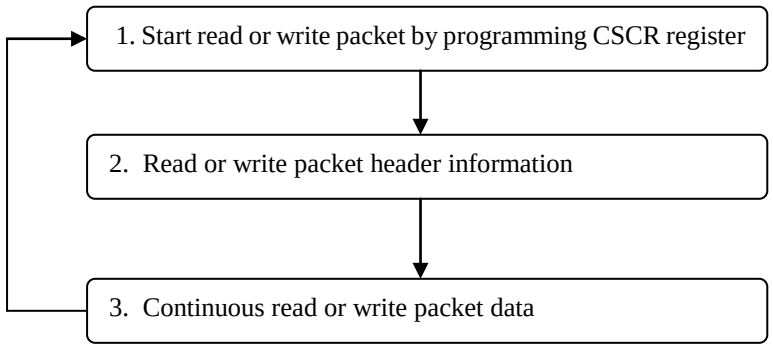


Fig 31 CPU Interface Packet Read/Write Flow

The following three steps show how the CPU reads the packet out of the AX88782/AX88783 host port process.

1. The CPU needs to write one to the CSCR bit [31] to start the process.
2. The CPU reads the address CCR (0x04C) to get the packet size, packet type and source port information. If the GMCR [29] (InsSrcToCPU) is set to one then source port ID will be inserted by the switch engine at the end of the payload.
3. The CPU continuously reads the address CCR (0x04C) or 0x0800 to collect packet data till the end.

The following three steps show how the CPU writes the packet into the AX88782/AX88783 host port process.

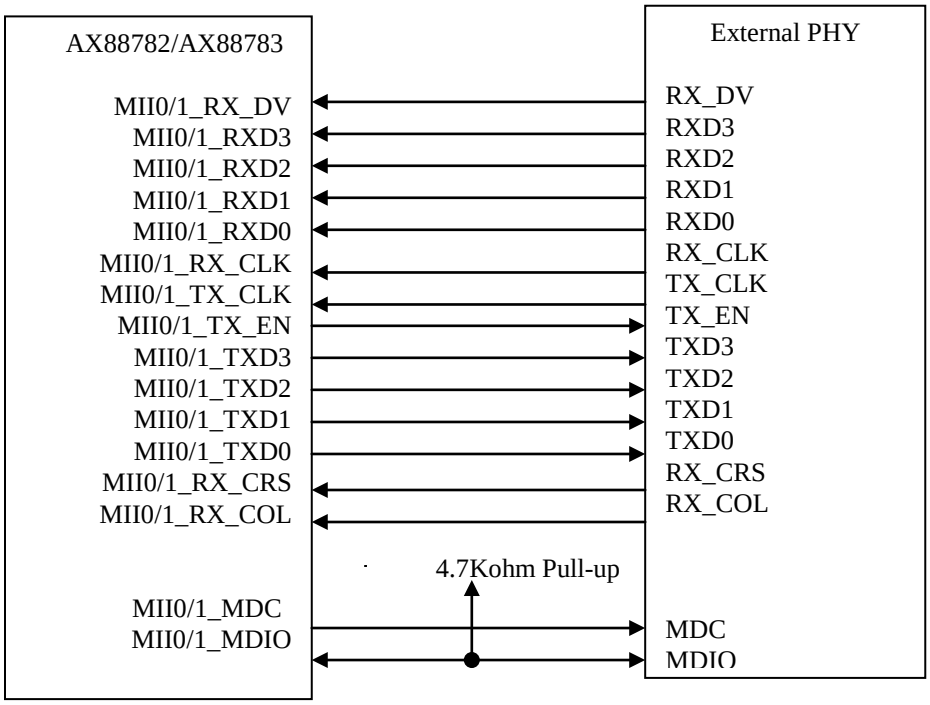
1. The CPU needs to write one to the CSCR bit [15] to start the process.
2. The CPU writes the address CCR (0x04C) to set the packet size. If the PID_En and the GMCR [28] (InsSrcFromCpu) both set to one, then the PID will represent software-forwarding information. For example, if the PID is 00, then the switch should forward this packet to the port 0. If the GMCR [28] (InsSrcFromCpu) is set to one then the forwarding information (PID) will need to be inserted by the software at the end of the payload before CRC field..
3. The CPU continuously reads the address CCR (0x04C) or 0x0800 to collect packet data till the end.

NOTE1: The CSCR register only support single read/write operation.
NOTE2: The AX88782/AX88783 also supports burst transaction to speed up the transaction process. The burst starting address should be 0x800 and follow by 0x0804, 0x0808, 0x080C ….etc. The CSN pin (chip select) and read/write control will need to be set active until the end of burst transaction. Please reference 6.6.7 for detail CPU interface timing diagram.

4.0 Interface

4.1 MII Interface

The AX88782/AX88783 host port to external PHY connection when configured to MII mode.



NOTE: If both Port 0 and Port 1 are set to MII Mode then please tie MDIO to MII0_MDIO and MDC to MII0_MDC and ignore MII1_MDIO and MII1_MDC.

4.1.1 MII Interface Set-Up Procedure

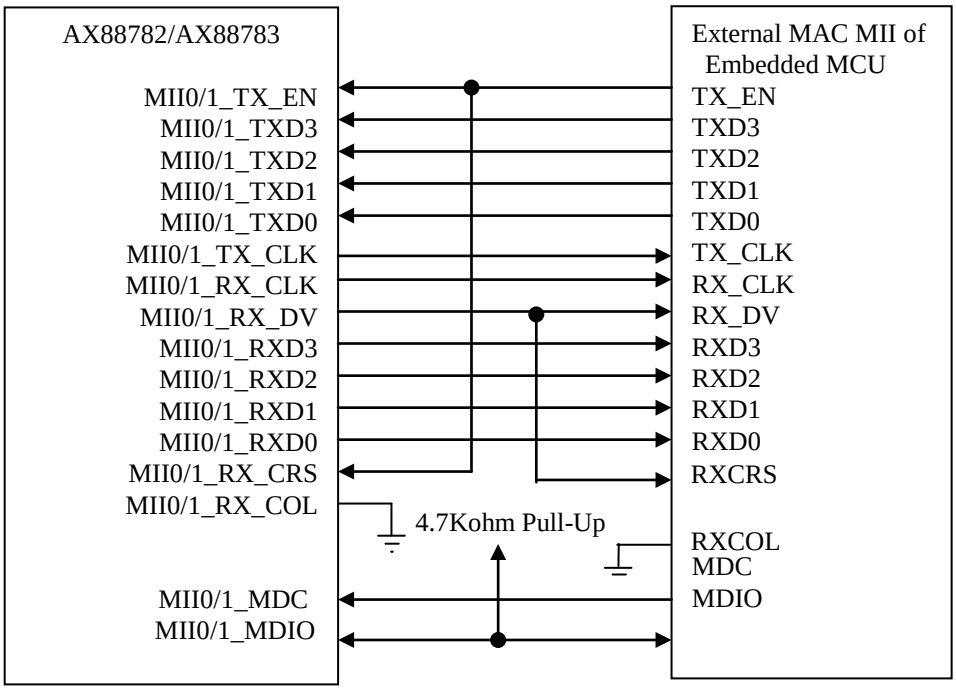
Enable MII Interface on Port 0:

1 Set PHY0 Power down through MDIO. (Please refer to section 3.5 Power-down mode through MDIO interface)
2 Disable internal PHY0 by Setting PCR bit [0] to 0.
3 Set ICR bit [16] and bit [28] to 1
  ICR [16]: Port 0 MII Enable
  ICR [28]: Port 0 MDIO Link Enable.
4 Set ACR bit [24] and bit [28] to 1 and Define Port 0's PHY ID on ACR [4:0]
  ACR [24]: Enable Port 0 Auto-Polling Function
  ACR [28]: Enable Port 0 Auto-Flow-Control-Polling Function

Enable MII Interface on Port 1:

1 Set internal PHY1 Power down, set PCR bit [17] to 1 and disable internal PHY1 by Setting PCR bit [16] to 0.
2 Set ICR bit [17] and bit [29] to 1.
  ICR [17]: Port 1 MII Enable
  ICR [29]: Port 1 MDIO Link Enable
3 Set ACR bit [25] and bit [29] to 1 and Define Port 1's PHY ID on ACR [12:8]
  ACR [25]: Enable Port 1 Auto-Polling Function
  ACR [29]: Enable Port 1 Auto-Flow-Control-Polling Function

4.2 Reverse MII Interface (Only Support 100M Full Duplex Mode)



4.2.1 Reverse MII Interface Set-Up Procedure

Enable Reverse MII Interface on Port 0:

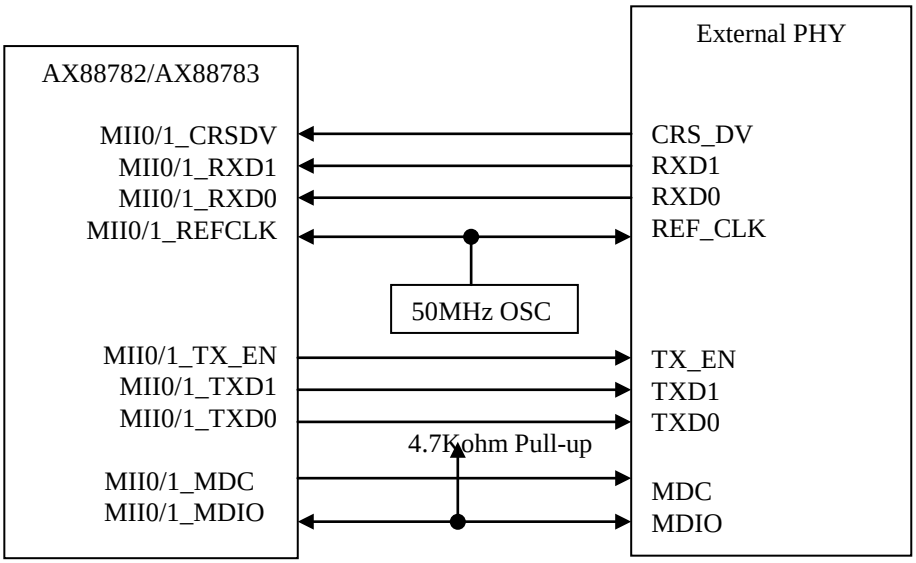
1 Set PHY0 Power down through MDIO. (Please refer to section 3.5 Power-down mode through MDIO interface)
2 Disable internal PHY0 by Setting PCR bit [0] to 0.
3 Set ICR [24] to 1. (Enable Reverse MII Interface on Port 0)
4 Set P0SMR0 bit [31] and bit [30] to 1 and Define Port 0's MDIO PHY ID on P0SMR0 [4:0]
P0SMR0 [31]: Port 0 Slave-MDIO Interface Enable
P0SMR0 [30]: Port 0 Slave-MDIO PHY Address Enable.
5 Set P0MCR Port 0's MAC Configuration Register
P0MCR [0]: Enable Port 0 MAC Function
P0MCR [3]: Port 0 Speed Configuration
P0MCR [4]: Port 0 Duplex Selection
P0MCR [7]: Port 0 Flow-Control ON/OFF Selection
P0MCR [8]: Port 0 CRC Check Function

Enable MII Interface on Port 1:

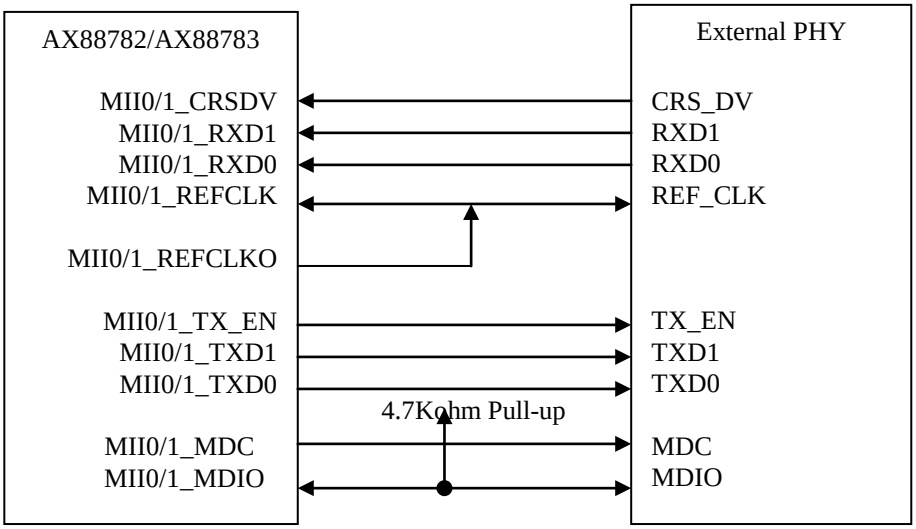
1 Set internal PHY1 Power down, set PCR bit [17] to 1 and disable internal PHY1 by Setting PCR bit [16] to 0.
2 Set ICR [25] to 1. (Enable Reverse MII Interface on Port 1)
3 Set P1SMR0 bit [31] and bit [30] to 1 and Define Port 1's MDIO PHY ID on P1SMR0 [4:0]
P1SMR0 [31]: Port 1 Slave-MDIO Interface Enable
P1SMR0 [30]: Port 1 Slave-MDIO PHY Address Enable
4 Set P1MCR Port 1's MAC Configuration Register
P1MCR [0]: Enable Port 1 MAC Function
P1MCR [3]: Port 1 Speed Configuration
P1MCR [4]: Port 1 Duplex Selection
P1MCR [7]: Port 1 Flow-Control ON/OFF Selection
P1MCR [8]: Port 1 CRC Check Function

4.3 RMII and Reverse RMII Interface

4.3.1 RMII Mode Reference connection



The AX88782/AX88783 can use either external system reference 50 MHz clock (figure above) or internal generated 50MHz reference clock (figure below) as RMII reference clock input.



4.3.2 RMII Interface Set-Up Procedure

Enable RMII Interface on Port 0:

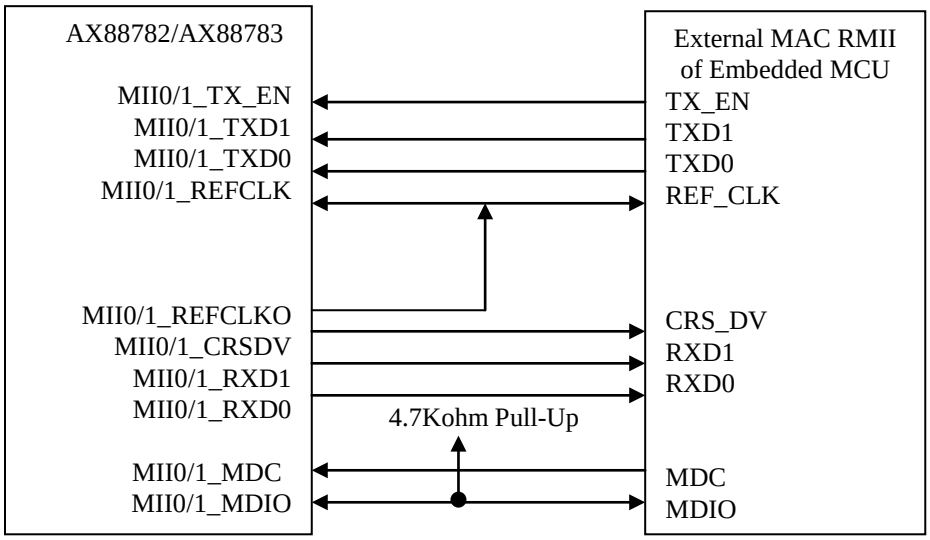
1 Set PHY0 Power down through MDIO. (Please refer to section 3.5 Power-down mode through MDIO interface)
2 Disable internal PHY0 by Setting PCR bit [0] to 0.
3 Set OCSR [7:0] = 0x41 to use internal 50MHz clock divide from core 100MHz.
4 Set ICR [28], [12], [4] and [0] to 1.
ICR [0]: Enable Port 0 RMII internal clock
ICR [4]: Enable Port 0 RMII Interface MUX
ICR [12]: Enable Port 0 RMII 50MHz Reference Clock Output
ICR [28]: Enable Port 0 MDIO Communication Interface
5 Set ACR bit [24] and bit [28] to 1 and Define Port 0's PHY ID on ACR [4:0]
ACR [24]: Enable Port 0 Auto-Polling Function
ACR [28]: Enable Port 0 Auto-Flow-Control-Polling Function

Enable RMII Interface on Port 1:

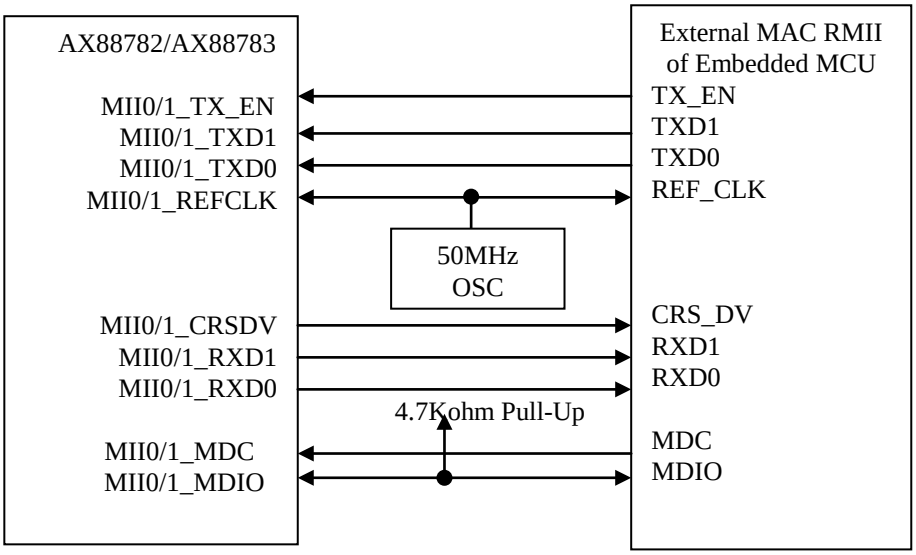
1 Set internal PHY0 Power down, set PCR bit [17] to 1 and disable internal PHY1 by Setting PCR bit [16] to 0.
2 Set OCSR [7:0] = 0x41 to use internal 50MHz clock divide from core 100MHz.
3 Set ICR [29], [13], [5] and [1] to 1.
ICR [1]: Enable Port 1 RMII internal clock
ICR [5]: Enable Port 1 RMII Interface MUX
ICR [13]: Enable Port 1 RMII 50MHz Reference Clock Output
ICR [29]: Enable Port 1 MDIO Communication Interface
4 Set ACR bit [25] and bit [29] to 1 and Define Port 1's PHY ID on ACR [12:8]
ACR [25]: Enable Port 0 Auto-Polling Function
ACR [29]: Enable Port 0 Auto-Flow-Control-Polling Function

4.3.3 Reverse RMII Mode Reference connection: (Only support 100 Full Duplex mode)

The AX88782/AX88783 is able to generate a 50MHz clock output after power on reset plus 2ms delay.



The AX88782/AX88783 can use system ‘s 50MHz reference clock as Reverse RMII reference clock source.



4.3.4 Reverse RMII Interface Set-Up Procedure

Enable Reverse RMII Interface on Port 0:

1 Set PHY0 Power down through MDIO. (Please refer to section 3.5 Power-down mode through MDIO interface)
2 Disable internal PHY0 by Setting PCR bit [0] to 0.
3 Set OCSR [7:0] = 0x41 to use internal 50MHz clock divide from core 100MHz.
1 Set P0SMR0 bit [31] and bit [30] to 1 and Define Port 0's MDIO PHY ID on P0SMR0 [4:0]
P0SMR0 [31]: Port 0 Slave-MDIO Interface Enable
P0SMR0 [30]: Port 0 Slave-MDIO PHY Address Enable
2 Set ICR [12], [8], [4] and [0] to 1.
ICR [0]: Enable Port 0 RMII internal clock
ICR [4]: Enable Port 0 RMII Interface MUX
ICR [8]: Enable Reverse RMII Ending option if necessary
ICR [12]: Enable Port 0 RMII 50MHz Reference Clock Output
3 Set P0MCR Port 0's MAC Configuration Register
P0MCR [0]: Enable Port 0 MAC Function
P0MCR [3]: Port 0 Speed Configuration
P0MCR [4]: Port 0 Duplex Selection
P0MCR [7]: Port 0 Flow-Control ON/OFF Selection
P0MCR [8]: Port 0 CRC Check Function

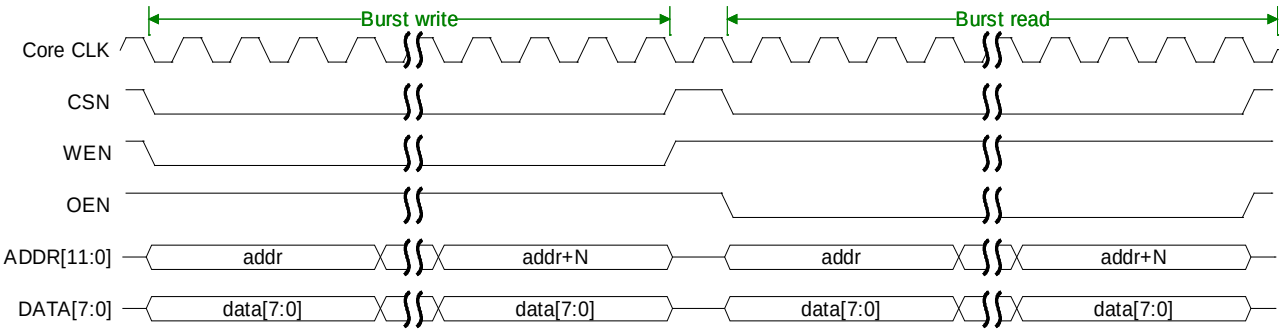
Enable Reverse RMII Interface on Port 1:

1 Set internal PHY0 Power down, set PCR bit[17] to 1 and disable internal PHY0 by Setting PCR bit [0] to 0.
2 Set OCSR [7:0] = 0x41 to use internal 50MHz clock divide from core 100MHz.
3 Set P1SMR0 bit [31] and bit [30] to 1 and Define Port 1's MDIO PHY ID on P1SMR0
P1SMR0 [31]: Port 1 Slave-MDIO Interface Enable
P1SMR0 [30]: Port 1 Slave-MDIO PHY Address Enable
4 Set ICR [13], [9], [5] and [1] to 1.
ICR [1]: Enable Port 1 RMII internal clock
ICR [5]: Enable Port 1 RMII Interface MUX
ICR [9]: Enable Reverse RMII Ending option if necessary
ICR [13]: Enable Port 1 RMII 50MHz Reference Clock Output
5 Set P1MCR Port 1's MAC Configuration Register
P1MCR [0]: Enable Port 1 MAC Function
P1MCR [3]: Port 1 Speed Configuration
P1MCR [4]: Port 1 Duplex Selection
P1MCR [7]: Port 1 Flow-Control ON/OFF Selection
P1MCR [8]: Port 1 CRC Check Function

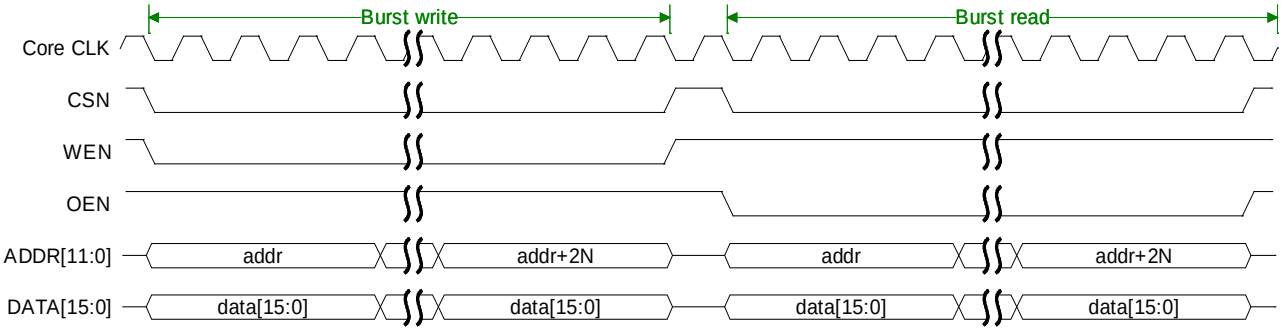
4.4 CPU Read/Write Operation

The AX88782 supports 8/16-bit SRAM-like bus interface and the AX88783 supports 8/16/32-bit SRAM-like bus interface. The following three sections list 8, 16, and 32 bit burst mode CPU read/write operation waveforms.

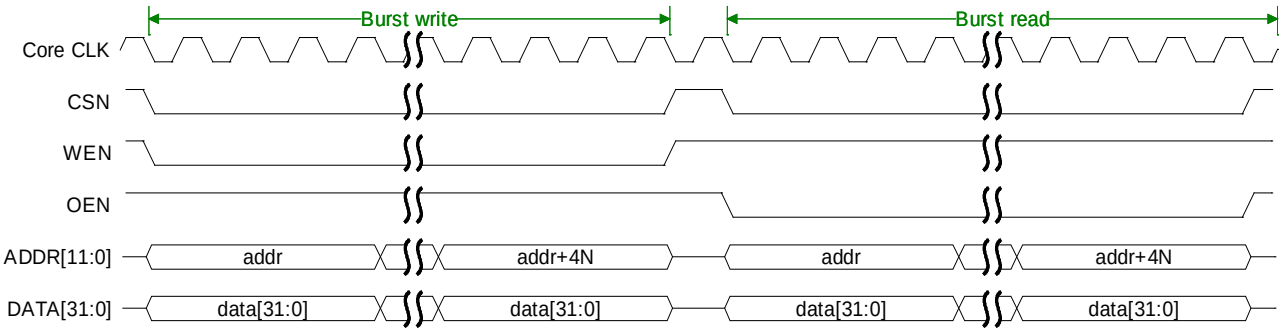
4.4.1 8-Bit CPU Burst Read/Write Operation



4.4.2 16-Bit CPU Burst Read/Write Operation



4.4.3 32-Bit CPU Burst Read/Write Operation



5.0 Internal Register Configuration

5.1 MAC Register Definition

The following set of registers allows read/write operations through host port interface for direct managing and programming of the AX88782/AX88783.

Address	NAME	Description	Default Value
0x000	CIRR	Chip ID and Reset Register	0x9D000000
0x004	PCR	PHY0/PHY1 Configuration Register	0x11009000
0x008	PSR	PHY0/PHY1 Status Register	0x0101BFBF
0x00C	GMCR	Global MAC Configuration Register (Max packet size,BC Storm)	0x048735F2
0x010	LGCR	Layer 2 Global Configuration Register (1Q, 1D, 1X, 1P, IGMP..)	0xFC000000
0x014	LLCR	Layer 2 Learning/Aging/OneSA Control Register	0x01FF7777
0x018	LRCR0	Layer 2 Routing Table Entry Read/Write Configuration Register 0	0x00000000
0x01C	LRCR1	Layer 2 Routing Table Entry Read/Write Configuration Register 1	0x00000000
0x020	PVCR	802.1D, Port-based VLAN Control Register	0x00000000
0x024	SFCR0	Sniffer Function Configuration Register 0	0x00000000
0x028	SFCR1	Sniffer Function Configuration Register I	0x00000000
0x02C	SFCR2	Sniffer Function Configuration Register 2	0x00000000
0x030	QPTR	QoS Priority Mapping Table Register	0xFA50FA50
0x034	QSR	802.1Q-in-1Q(Double-Tagging) Setup Register	0x81000000
0x038	PPMR	Port Pair and MDC Control Register	0x00310000
0x03C	MRCR	MDIO Read/Write Configuration Register	0x00000000
0x040	TOCR	TCP/IP Offload Control Register	0x00000000
0x04C	CCR	CPIO Control Register	0x00000000
0x050	SM0CR0	Security Mac 0 Control Register 0	0x00000000
0x054	SM0CR1	Security Mac 0 Control Register 1	0x00000000
0x058	SM1CR0	Security Mac 1 Control Register 0	0x00000000
0x05C	SM1CR1	Security Mac 1 Control Register 1	0x00000000
0x060	SM2CR0	Security Mac 2 Control Register 0	0x00000000
0x064	SM2CR1	Security Mac 2 Control Register 1	0x00000000
0x068	SM3CR0	Security Mac 3 Control Register 0	0x00000000
0x06C	SM3CR1	Security Mac 3 Control Register 1	0x00000000
0x070	SM4CR0	Security Mac 4 Control Register 0	0x00000000
0x074	SM4CR1	Security Mac 4 Control Register 1	0x00000000
0x078	SM5CR0	Security Mac 5 Control Register 0	0x00000000
0x07C	SM5CR1	Security Mac 5 Control Register 1	0x00000000
0x080	SM6CR0	Security Mac 6 Control Register 0	0x00000000
0x084	SM6CR1	Security Mac 6 Control Register 1	0x00000000
0x088	SM7CR0	Security Mac 7 Control Register 0	0x00000000
0x08C	SM7CR1	Security Mac 7 Control Register 1	0x00000000
0x090	VER0	VLAN Enrty 0 Register	0x00000000
0x094	VER1	VLAN Enrty 1 Register	0x00000000
0x098	VER2	VLAN Enrty 2 Register	0x00000000
0x09C	VER3	VLAN Enrty 3 Register	0x00000000
0x0A0	VER4	VLAN Enrty 4 Register	0x00000000
0x0A4	VER5	VLAN Enrty 5 Register	0x00000000
0x0A8	VER6	VLAN Enrty 6 Register	0x00000000
0x0AC	VER7	VLAN Enrty 7 Register	0x00000000
0x0B0	VER8	VLAN Enrty 8 Register	0x00000000

0x0B4	VER9	VLAN Enrty 9 Register	0x00000000
0x0B8	VER10	VLAN Enrty 10 Register	0x00000000
0x0BC	VER11	VLAN Enrty 11 Register	0x00000000
0x0C0	VER12	VLAN Enrty 12 Register	0x00000000
0x0C4	VER13	VLAN Enrty 13 Register	0x00000000
0x0C8	VER14	VLAN Enrty 14 Register	0x00000000
0x0CC	VER15	VLAN Enrty 15 Register	0x00000000
0x0D0	CBOR	CPIO Byte-Order Register	0x00000000
0x0D4	CSCR	CPIO Start Command Register	0x00000000
0x0D8	ITCR	IGMP Table Read/Write Control Register	0x00000000
0x0DC	LCR	LED Control Register	0x00000000
0x0E0	RCR	RMON Control Register	0x00000000
0x0E4	RDR	RMON Data Register	0x00000000
0x0E8	DQR0	DSCP QoS Mapping Table Register 0	0x00000000
0x0EC	DQR1	DSCP QoS Mapping Table Register 1	0x00000000
0x0F0	DQR2	DSCP QoS Mapping Table Register 2	0x00000000
0x0F4	DQR3	DSCP QoS Mapping Table Register 3	0x00000000
00xF8	ISMR	Interrupt Status and Mask Register	0xFFFF0000
0x100	USTR	User-Defined Sniffer Packet Type Register	0x73738863
0x104	WCR0	Wake-On-LAN Configuration Register 0	0x00500000
0x108	WCR1	Wake-On-LAN Configuration Register 1	0x00000000
0x10C	P0WMR0	Port 0 Wake-On-LAN Wake-up Frame Mask Register 0	0x00000000
0x110	P0WMR1	Port 0 Wake-On-LAN Wake-up Frame Mask Register 1	0x00000000
0x114	P0WMR2	Port 0 Wake-On-LAN Wake-up Frame Mask Register 2	0x00000000
0x118	P0WCR0	Port 0 Wake-On-LAN Wake-up Frame CRC Register 0	0x00000000
0x11C	P0WCR1	Port 0 Wake-On-LAN Wake-up Frame CRC Register 1	0x00000000
0x120	P0WCR2	Port 0 Wake-On-LAN Wake-up Frame CRC Register 2	0x00000000
0x124	P1WMR0	Port 1 Wake-On-LAN Wake-up Frame Mask Register 0	0x00000000
0x128	P1WMR1	Port 1 Wake-On-LAN Wake-up Frame Mask Register 1	0x00000000
0x12C	P1WMR2	Port 1 Wake-On-LAN Wake-up Frame Mask Register 2	0x00000000
0x130	P1WCR0	Port 1 Wake-On-LAN Wake-up Frame CRC Register 0	0x00000000
0x134	P1WCR1	Port 1 Wake-On-LAN Wake-up Frame CRC Register 1	0x00000000
0x138	P1WCR2	Port 1 Wake-On-LAN Wake-up Frame CRC Register 2	0x00000000
0x13C	OCSR	Output Clock Select Register	0x00000000
0x140	ACR	Auto-polling Control Registers	0x70000000
0x144	ECR	EEROM Control Registers	0x00000000
0x148	BLCR	Boot Loader Control Register	0x00000000
0x14C	IOCR	IO Pad Control Register	0x00000000
0x150	IER0	IGMP Entry 0 Register	0x00000000
0x154	IER1	IGMP Entry 1 Register	0x00000000
0x158	IER2	IGMP Entry 2 Register	0x00000000
0x15C	IER3	IGMP Entry 3 Register	0x00000000
0x160	IER4	IGMP Entry 4 Register	0x00000000
0x164	IER5	IGMP Entry 5 Register	0x00000000
0x168	IER6	IGMP Entry 6 Register	0x00000000
0x16C	IER7	IGMP Entry 7 Register	0x00000000
0x170	GPIOCR1	GPIO Control Register 1	0x00000000
0x174	GPIOCR2	GPIO Control Register 2	0x00000000
0x178	GPIOCR3	GPIO Control Register 3	0x00000000
0x17C	GPIOCR4	GPIO Control Register 4	0x00000000
0x180	P0SMR0	Port 0 Slave MDIO Register 0	0x00000001
0x184	P0SMR1	Port 0 Slave MDIO Register 1	0x78293100
0x188	P0SMR2	Port 0 Slave MDIO Register 2	0x0DE105E1
0x18C	P0SMR3	Port 0 Slave MDIO Register 3	0x00000000

0x190	P1SMR0	Port 1 Slave MDIO Register 0	0x00000001
0x194	P1SMR1	Port 1 Slave MDIO Register 1	0x78293100
0x198	P1SMR2	Port 1 Slave MDIO Register 2	0x0DE105E1
0x19C	P1SMR3	Port 1 Slave MDIO Register 3	0x00000000
0x1B0	P2MFR0	Port 2 Multicast Filter Register 0	0x00000000
0x1B4	P2MFR1	Port 2 Multicast Filter Register 1	0x00000000
0x1B8	P2MFR2	Port 2 Multicast Filter Register 2	0x00000000
0x1BC	P2MFR3	Port 2 Multicast Filter Register 3	0x00000000
0x1C0	P2MFR4	Port 2 Multicast Filter Register 4	0x00000000
0x1C4	P2MFR5	Port 2 Multicast Filter Register 5	0x00000000
0x1C8	P2MFR6	Port 2 Multicast Filter Register 6	0x00000000
0x1CC	P2MFR7	Port 2 Multicast Filter Register 7	0x00000000
0x1D0	P2MFR8	Port 2 Multicast Filter Register 8	0x00000000
0x1D4	P2MFR9	Port 2 Multicast Filter Register 9	0x00000000
0x1D8	P2MFR10	Port 2 Multicast Filter Register 10	0x00000000
0x1DC	P2MFR11	Port 2 Multicast Filter Register 11	0x00000000
0x1E0	P2MFR12	Port 2 Multicast Filter Register 12	0x00000000
0x1E4	P2MFR13	Port 2 Multicast Filter Register 13	0x00000000
0x1E8	P2MFR14	Port 2 Multicast Filter Register 14	0x00000000
0x1EC	P2MFR15	Port 2 Multicast Filter Register 15	0x00000000
0x1F0	ICR	Interface Configuration Register	0x00000000
0x1F4	SMER	Sleep Mode Exit Register	0x00000000
0x1FC	GTCR	General Purpose Timer Configuration Register	0x00000000
0x200	P0MCR	Port 0 MAC Configuration Register	0x00000100
0x204	P0QMTR	Port 0 802.1p QoS Mapping Table Register	0x0000FA50
0x208	P0QCR	Port 0 802.1Q Configuration for UnTag Frame Register	0x00000001
0x20C	P0RQR0	Port 0 RX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x210	P0RQR1	Port 0 RX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x214	P0TQR0	Port 0 TX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x218	P0TQR1	Port 0 TX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x21C	P0RLR	Port 0 per Port Rate Limit Register	0x0FFF0FFF
0x220	P0RLTR	Port 0 Rate Limit Timer Register	0x05F5E100
0x224	P0FCR	Port 0 Flow Control High/Low watermark Register	0x00001428
0x228	P0QWR	Port 0 Per Queue Weighting Register	0x0000FFFF
0x22C	P0RDCR	Port 0 RX Drop Counter Register	0x00000000
0x230	P0DAR0	Port 0 DA MAC Address Register 0	0x00000000
0x234	P0DAR1	Port 0 DA MAC Address Register 1	0x00000000
0x240	P1MCR	Port 1 MAC Configuration Register	0x00000100
0x244	P1QMTR	Port 1 802.1p QoS Mapping Table Register	0x0000FA50
0x248	P1QCR	Port 1 802.1Q Configuration for UnTag Frame Register	0x00000001
0x24C	P1RQR0	Port 1 RX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x250	P1RQR1	Port 1 RX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x254	P1TQR0	Port 1 TX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x258	P1TQR1	Port 1 TX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x25C	P1RLR	Port 1 per Port Rate Limit Register	0x0FFF0FFF
0x260	P1RLTR	Port 1 Rate Limit Timer Register	0x05F5E100
0x264	P1FCR	Port 1 Flow Control High/Low watermark Register	0x00001428
0x268	P1QWR	Port 1 Per Queue Weighting Register	0x0000FFFF
0x26C	P1RDCR	Port 1 RX Drop Counter Register	0x00000000
0x270	P1DAR0	Port 1 DA MAC Address Register 0	0x00000000
0x274	P1DAR1	Port 1 DA MAC Address Register 1	0x00000000
0x280	P2MCR	Port 2 MAC Configuration Register	0x00000100
0x284	P2QMTR	Port 2 802.1p QoS Mapping Table Register	0x0000FA50
0x288	P2QCR	Port 2 802.1Q Configuration for UnTag Frame Register	0x00000001

0x28C	P2RQR0	Port 2 RX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x290	P2RQR1	Port 2 RX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x294	P2TQR0	Port 2 TX Queue0/1 Rate Limit Control Register	0x0FFF0FFF
0x298	P2TQR1	Port 2 TX Queue2/3 Rate Limit Control Register	0x0FFF0FFF
0x29C	P2RLR	Port 2 per Port Rate Limit Register	0x0FFF0FFF
0x2A0	P2RLTR	Port 2 Rate Limit Timer Register	0x05F5E100
0x2A4	P2FCR	Port 2 Flow Control High/Low watermark Register	0x00001428
0x2A8	P2QWR	Port 2 Per Queue Weighting Register	0x0000FFFF
0x2B0	P2DAR0	Port 2 DA MAC Address Register 0	0x00000000
0x2B4	P2DAR1	Port 2 DA MAC Address Register 1	0x00000000
0x2BC	GPIOWR	GPIO Wakeup Control Register	0x00000000

Table 15 Register Mapping Table

5.1.1 Chip revision ID and Reset Register (CIRR)

Address 0x000

Bit	Name	Default Value	R/W	Function
[2:0]	Chip_mode	000	R	These three bits is read from pin MODE2, MODE1, and MODE0. 000: 8 bit CPU interface 001: 16 bit CPU interface 010: 32 bit CPU interface
[3]	Reserved	0	R	Reserved
[5:4]	Prom_mode	00	R	EEROM mode: EEROM memory size (read only) 00: NO EEROM 01: 1K-bit (93C46) 10: 2K-bit (93C56) 11: 4K-bit (93C66) Please reference Table 11 for detail information. The host CPU should read this value first to know the maximum address size of the EEPROM device before read/write or clear the EEPROM data through ECR register. The EEPROM size is detected during the power-on reset from pull-up or pull-down state found on CS and SK pins.
[6]	Reserved	0	RW	Reserved
[7]	Reserved	0	R	Reserved
[11:8]	Chip_rev [3:0]	0010	RW	Chip revision ID
[15:12]	Reserved	0000	R	Reserved
[16]	ChipInitDone	0	R	Chip Initialization process finished (read only) Chip Initialization process includes all the internal embedded SRAM initialization process and EEPROM loading process. The host CPU should constantly keep polling this bit to check if the AX88782/AX88783 is still in initialization process before read or write operation into any internal registers. 1: Complete the whole chip initialization process 0: Still waiting the whole chip initialization process to be done The host CPU need to poll this bit first to confirm the AX88782/AX88783 exit the initialization process after the following situation: 1. Power-on process 2. Back from power down state like the D1 state or the D2 state 3. Reload the EEPROM data (set Boot_En=1 in BLCR)
[23:17]	Reserved	0x00	R	Reserved
[24]	Reserved	1	RW	Always set to one
[25]	Reserved	0	R	Reserved
[26]	CPIreset	1	RW	Reset CPI (CPU memory write FIFO within the chip) related logic 0: Reset CPI FIFO 1: Normal (Default)
[27]	CPOreset	1	RW	Reset CPO (CPU memory read FIFO within the chip) related logic 0: Reset CPO FIFO 1: Normal (Default)
[28]	Wrst_n	1	RW	Switch core (except Wake-On-LAN related logic) reset 1: Normal (Default) 0: Reset switch core This bit used to reset the AX88782/AX88783 switch core block for power down function. Before the chip enter the D2 sleep mode, the CPU should set this bit to zero to reset switch core block, and then enter the D2 sleep mode. After exit the D2 sleep mode, the CPU should set this bit to 1 to let the AX88782/AX88783 switch core function to normal work state.
[30:29]	Reserved	00	R	Reserved
[31]	Chip reset	1	RW	Whole Chip Software Reset 1: Normal (Default) 0: Reset the whole chip

5.1.2 PHY0 /PHY1 Configuration Register (PCR)

Address 0x004

Bit	Name	Default Value	R/W	Function
[0]	Phy reset0	0	RW	PHY0 reset signal. Active low and should be longer than 500ns. 1: Normal 0: Reset internal PHY0 (Default) The host CPU should write one to enable PHY0 back to normal state.
[1]	Power down0	0	RW	PHY0 Power Down. Active high. 1: PHY0 power down 0: Normal (Default) NOTE: PHY0 Power down will turn off core clock and shut down the chip.
[2]	Reserved	0	R	Reserved
[3]	Loopback0	0	RW	PHY0 Loop-Back mode. Active high. 1: PHY0 Look-back enable 0: PHY0 Loop-back disable (Default)
[6:4]	Opmode0	000	RW	PHY0 Operation mode 000: Auto-negotiation mode 001: Auto-negotiation with 100 BASE-TX FDX/HDX ability 010: Auto-negotiation with 10 BASE-T FDX/HDX ability 011: Reserved 100: Manual selection of 100 BASE-TX FDX 101: Manual selection of 100 BASE-TX HDX 110: Manual selection of 10 BASE-T FDX 111: Manual selection of 10 BASE-T HDX
[7]	Reserved	0	R	Reserved
[12:8]	Phyid0	10000	RW	Programmable PHY0 ID Registers. This address is used when multiple PHY are accessed through management interface. If the value is changed, new setting will effective after hardware/software is reset. The default value is 10000.
[13]	PowerSaving0	0	RW	PHY0 Power Saving Mode 1: PHY Power Saving State 0: Normal State (Default)
[14]	Reserved	0	R	Reserved
[15]	SWPowerSaving	1	RW	Software Power Saving Control 1: Software Control the internal PHY Power Saving State (Default) 0: Hardware Power Saving State Auto-detect function Enable
[16]	Phy reset1	0	RW	PHY1 reset signal. Active low and should be longer than 500ns. 1: Normal 0: Reset internal PHY1 (Default) The host CPU should write one to enable PHY1 back to normal state.
[17]	Power down1	0	RW	PHY1 Power Down. Active high. 1: PHY1 power down 0: Normal (Default)
[18]	Reserved	0	R	Reserved
[19]	Loopback1	0	RW	PHY1 Loop-Back mode. Active high. 1: PHY1 Look-back enable 0: PHY1 Loop-back disable (Default)
[22:20]	Opmode1	000	RW	PHY1 Operation mode 000: Auto-negotiation mode 001: Auto-negotiation with 100 BASE-TX FDX/HDX ability 010: Auto-negotiation with 10 BASE-T FDX/HDX ability 011: Reserved 100: Manual selection of 100 BASE-TX FDX 101: Manual selection of 100 BASE-TX HDX

				110: Manual selection of 10 BASE-T FDX 111: Manual selection of 10 BASE-T HDX
[23]	Reserved	0	R	Reserved
[28:24]	Phyid1	10001	RW	Programmable PHY1 ID Registers. This address is used when multiple PHY are accessed through management interface. If the value is changed, new setting will effective after hardware/software is reset. The default value is 10001.
[29]	PowerSaving1	0	RW	PHY1 Power Saving Mode 1: PHY Power Saving State 0: Normal State (Default)
[30]	Reserved	0	R	Reserved
[31]	Rgi_standby	0	RW	Regulator stand-by mode enable bit. Allowed range 1.8 ~ 3.3 Volt 1: Stand-by mode 0: Normal operation

5.1.3 PHY0/PHY1 Status Register (PSR)

Address 0x008

Bit	Name	Default Value	R/W	Function
[0]	Speed0	1	R	PHY0 Link Speed Status 0: 100MBps 1: 10MBps
[1]	Duplex0	1	R	PHY0 Full Duplex Mode Status 0: Full Duplex Mode 1: Half Duplex Mode
[2]	Reserved	1	R	Reserved
[3]	RX0	1	R	PHY0 Receive activity 0: RX traffic passing 1: No Traffic
[4]	TX0	1	R	PHY0 Transmit activity 0: TX traffic passing 1: No Traffic
[5]	COL0	1	R	PHY0 Collision Status 0: Collision Detect 1: No Collision
[6]	Link0	0	R	PHY0 Link Status 1: Link up 0: Link Down
[7]	Reserved	1	R	Reserved
[8]	Speed1	1	R	PHY1 Link Speed Status 0: 100MBps 1: 10MBps
[9]	Duplex1	1	R	PHY1 Duplex Mode Status 0: Full Duplex Mode 1: Half Duplex Mode
[10]	Reserved	1	R	Reserved
[11]	RX1	1	R	PHY1 Receive activity 0: RX traffic passing 1: No RX Traffic
[12]	TX1	1	R	PHY1 Transmit activity 0: TX traffic passing 1: No TX Traffic
[13]	COL1	1	R	PHY1 Collision Status 0: Collision Detect 1: No Collision
[14]	Link1	0	R	PHY1 Link Status 1: Link Up 0: Link Down
[16:15]	Reserved	11	R	Reserved
[17]	Cable_Off0	0	R	PHY0 Cable Off Status 0: Normal State 1: PHY0 Cable Off
[24:18]	Reserved	0x40	R	Reserved
[25]	Cable_Off1	0	R	PHY1 Cable Off Status 0: Normal State 1: PHY1 Cable Off
[31:26]	Reserved	0x00	R	Reserved

5.1.4 Global MAC Configuration Register (GMCR)

Address 0x00C

Bit	Name	Default Value	R/W	Function
[10:0]	MPL	0x5F2	RW	Programmable maximum packet size allowed to be received range from 64 to 2047.Default value is 1522.
[11]	Reserved	0	R	Reserved
[12]	Reserved	1	RW	Always set to one
[13]	NoAbort	1	RW	Force the internal MAC never abort when exceed maximum collision limit if this bit is set to one and used only in half duplex mode
[15:14]	MaxStorm	00	RW	Broadcast Storm control. This function enables each port to drop the broadcast packet when continuously received broadcast packets exceed the following pre-define limit numbers. 00: Disable Broadcast Storm 01: 32 Broadcast frames 10: 48 Broadcast frames 11: 64 Broadcast frames
[19:16]	Reserved	0111	RW	Reserved
[20]	Reserved	0	R	Reserved
[21]	SuperMac	0	RW	Reduce back-off count and collision when MAC is in half duplex mode if set to one
[22]	PTO	0	RW	Pause Type Only. The RX MAC will only detect Ethernet Type= 0x8808 and OP code =0001 as a Pause frame if this bit is set to one.
[23]	CSJ	1	RW	Continue Send Jam: Never Stop Backpressure when set to one (Only for 10Mps)
[24]	Reserved	0	R	Reserved
[25]	Reserved	0	RW	Reserved
[26]	GenCRC	1	RW	Enable the generation of CRC. 1: MAC TX will recalculate CRC 0: Not append CRC
[27]	Int_hl	0	RW	Set Interrupt polarity. 1: Active high 0: Active low
[28]	InsSrcFromCpu	0	RW	The external CPU is able to control forwarding function by assigning PID field. This is the software switch function enable bit. Please also reference 3.22 for further detail information. 1: Enable function 0: Disable function
[29]	InsSrcToCPU	0	RW	Insert Source Port number in the end of last payload byte before CRC to CPU port for frame from Port 0 and Port 1 if this bit is set to one. If the last byte bit [1:0]=0 means this packet is from port 0. If the last byte bit [1:0]=1 means this packet is from port 1.
[30]	Cnt_Preamble	0	RW	Add 8 preamble bytes when calculate rate limit count if this bit is set to one.
[31]	Reserved	0	RW	Always set to zero.

5.1.5 Layer 2 Global Configuration Register (LGCR)

Address 0x010

Bit	Name	Default Value	R/W	Function
[0]	QoSSel	0	RW	Select lower3 bit of COS/TOS field as QoS Value when COS/TOS_En is on and this bit is set to one. Otherwise, COS/TOS upper 3 bits will be the default QoS value. 1: Select [2:0] as QoS index value 0: Select [5:3] as QoS index value
[1]	COS_En	0	RW	Enable QoS mapping table (convert from eight queues to four queues) for IPv6 frame Traffic class (TC) field. If QoSSel=1, then TC [4:2] will be the QoS entry to the mapping table. If QoSSel=0, then TC [7:5] will be the QoS entry to the mapping table. COS mapping table is located in QPTR. 1: IPv6 COS QoS mapping table enable 0: Disable
[2]	TOS_En	0	RW	Enable QoS mapping table (convert from eight queues to four queues) for IPv4 frame Type of Service (TOS) field. If QoSSel=1, then TOS [4:2] will be the QoS entry to the mapping table. If QoSSel=0, then TOS [7:5] will be the QoS entry to the mapping table. TOS mapping table is located in QPTR. 1: IPv4 TOS QoS mapping table enable 0: DIsable
[3]	DSCP_En	0	RW	Enable DSCP QoS Mapping table for IPv4/IPv6 TOS/COS [7:2] if [1] or [2] are also enabled. There are 64 QoS level start from ToS/TC [7:2]=0 to ToS/TC [7:2]=63 when DSCP is enabled. DSCP Mapping table is located in DQR. Note: QoS priority DSCP > COS/TOS > VLAN and make sure either COS_En or TOS_En is also enabled. 1: DSCP mapping enable 0: Disable
[4]	Filter_En	0	RW	Enable Filtering packet when SA or DA match in Routing Table or Security Mac. If this bit and DA filter bit in Routing Table entry both set to one then the packet will be dropped if DA MAC match. If this bit and SA filter bit in Routing Table entry both set to one then the packet will be dropped if SA MAC match. If this bit and DA filter bit in Security MAC entry both set to one then the packet will be dropped if DA MAC matches. (Please reference SM0CR ~ SM7CR Security MAC table) If this bit and SA filter bit in Security MAC entry both set to one then the packet will be dropped if SA MAC matches. (SM0CR ~ SM7CR Security MAC table) 1: Routing Table Filter Function Enable 0: Disable
[5]	Stop_Learn	0	RW	Disable Learning and Aging of Layer 2 Routing Table, If DA is not found in the Layer 2 Routing Table, then this packet will be dropped. No SA MAC will be learned and NO MAC entry will be aged out once this bit is set to one 1: Stop Learning and aging disable 0: Disable
[6]	ARPtoCPU	0	RW	Send ARP Packet to CPU port when this bit is set to one. 1: Enable ARP packet to CPU port 0: Disable
[7]	Hash	0	RW	Hashing method used in the AX88613 internal 2-way 512byte Routing Table lookup algorithm. 0: Linear hashing (Index [8:0]=MAC [8:0] as Routing table index)

				1: XOR hashing (Index [8:0] = MAC [44:36] ^ MAC [35:27] ^ MAC [26:18] ^ MAC [17:9] ^ MAC [8:0])
[8]	VLAN_QoS_En	0	RW	VLAN QoS priority will be higher than IPv4/IPv6 TOS/COS if this bit is set to one. Else QoS mapping priority will be DSCP > ToS/TC > VLAN Note: If the Flow Control bit is set to one then QoS will always be 0 (map to queue 0). 1: VLAN Tag QoS has higher priority than IPv4/IPv6/DSCP 0: Disable
[9]	En_CPIO	0	RW	Always set 0 when write GMCR register.
[10]	MCoverVLAN	0	RW	Multicast packet to transmit over VLAN boundary. Effective only when 802. is enabled. 1: Enable le
[11]	Reserved	0	RW	Reserved
[12]	CtrlPktToCPU	0	RW	CtrlPktToCPU =1, Control Packet (DA [47:0] = 0x0180_C200_0000~ 0x0180_C200_00FF) will forward to CPU Port only. CtrlPktToCPU =0, Control Packet (DA [47:0] = 0x0180_C200_0000~ 0x0180_C200_00FF) will broadcast.
[13]	IGMP_En	0	RW	Enable IGMPv4 Forwarding Table look-up process (IER0 ~ IER7 eight IGMP entry location) 1: IGMP Enable 0: Disable
[14]	IGMP_Mode	0	RW	If IGMP En=1 and IGMP_Mode=1, all IGMPv4 packets will be forwarded to CPU port. If IGMP_En=1 and IGMP_Mode=0, all IGMPv4 packet will be copied to CP
[15]	QinQ_En	0	RW	Enable 802.1 QinQ (Double-Tagging) Function. Please also configure P0MCR/P1MCR/P2MCR [15] uplink_port if necessary NOTE: Please make sure 1Q_En is set to 1 when QinQ_EN is enabled. 1: QinQ Enable 0: Disable
[16]	1X_En	0	RW	Enable 802.1X function. When enabled, all 802.1X control frame will be sent to CPU port with Port_ID attached after end of last payload. Each port's ON/OFF is defined in the Per-Port Setting: P0MCR/P1MCR/P2MCR [11]. 802.1X frame include MAC ID= 0x0180c2000003 or Ethernet Packet Type= 0x888E frames. 1: 802.1X Enable 0: Disable
[17]	GMRP_En	0	RW	Enable GMRP control packet forwarding to CPU port if set to one. Ethernet frames with DA MAC = 0x0180c2000020 are GMRP frames. 1: GMRP packet to CPU Enable 0: Disable
[18]	GVRP_En	0	RW	Enable GVRP control packet forwarding to CPU port if set to one. Ethernet frames with DA MAC = 0x0180c2000021 are GVRP frames. 1: GVRP packet to CPU Enable 0: Disable
[19]	GARP_En	0	RW	Enable GARP control packet forwarding to CPU port if set to one. Ethernet frames with DA MAC = 0x0180c2000010 are GARP frames. 1: GARP packet to CPU Enable 0: Disable
[20]	VLAN_En	0	RW	Enable non-802.1Q Port base VLAN function. Total 3 VLAN group will be support. These Port-based VLAN groups are configured in PVCR 1: Port-Based VLAN Enable 0: Disable
[21]	1P_En	0	RW	Enable 802.1P priority frame function. When enabled, the priority field [2:0] in Tag header can be re-mapping to internal 4 queues. The Mapping table is located in P0QMTR/P1QMTR/P2QMTR. 1: 802.1P priority enable

				0: Disable
[22]	1Q_En	0	RW	Enable 802.1Q port-base VLAN function. There are 16 VLAN table entries in the VLAN forwarding table. VLAN table entry is defined in VER0 ~ VER15. VID can be configured between 1 and 4094. Note: 1Q_EN and VLAN_En can't enable at the same time! 1: 802.1Q Enable 0: Disable
[23]	1D_En	0	RW	Enable Spanning Tree (802.1D) function support. The 802.1D per Port State is defined in PVCR. 1: 802.1D Enable 0: Disable
[24]	StO	0	RW	Strict Ordering function Enable. When set to one, all incoming traffic to output queue will base on following Order: Q0-Q1-Q2-Q3-Q0-Q1-Q2-Q3… when the traffic is in congestion. 1: schedule TX packet with Strict ordering 0: Disable
[25]	Q0_Ig	0	RW	Ignore Q0 when congestion detect. If switch is congested, Q0 will be scheduled last. 1: Ignore queue 0 whenever there is a congestion 0: Disable
[31:26]	JamLimit	0x3F	RW	JAM Limit count. Default value is 0x3F.

5.1.6 Layer 2 Learning/Aging/OneSA Control Register (LLCR)

Address 0x014

Bit	Name	Default Value	R/W	Function
[1:0]	Broadcast PortMap	11	RW	Define broadcast forwarding port map for broadcast packet. For example, if set BroadcastPortMap[1:0] = 10 and port 0 receives a broadcast packet, then this packet will forward to port 1 and CPU port. If port 1 received a broadcast packet, then this packet will only forward to CPU port. BroadcastPortMap[1:0] = {Port1,Port0} .
[2]	Reserved	1	RW	Reserved
[3]	Reserved	0	R	Reserved
[5:4]	Flooding PortMap	11	RW	Define Flooding packet forwarding port map. For example, if set FloodingPortMap[1:0] = 10 and port 0 receives a new unicast packet (DA address can't find within the routing table) , then this packet will flood to port 1 and the CPU port. If port 1 receives a new unicast packet whose DA doesn't match with any routing table entry, then this packet only flood to the CPU port because FloodingPortMap[0] is set 0. FloodingPortMap[1:0] = {Port1,Port0}}.
[6]	Reserved	1	RW	Reserved
[7]	Reserved	0	R	Reserved
[9:8]	Multicast PortMap	11	RW	Define multicast packet forwarding port map. For example, If set MulticastPortMap[1:0] = 10 , and port 0 receives a multicast packet , this packet will forward to port 1 and the CPU port. If port 1 received a multicast packet, then this packet will only forward to the CPU port. MulticastPortMap[1:0] = {Port1,Port0}.
[10]	Reserved	1	RW	Reserved
[11]	Reserved	0	R	Reserved
[14:12]	LearnEn	111	RW	When Set to 0, per port SA MAC learning function will be disabled.For example, if we like to achieve per port security function on port 1. Setup procedure is list below: 1. Disable Aging. (LGCR [5] Stop_learn) 2. Enabled port 1 learning enable bit. All the learned SA Mac address will store in the routing table if no hashing collision or hashing collision is less than 2. 3. Disable port 1 learning function and enabled aging. The learned SA Mac address will not aging out. 4. Exclude port 1 from default flooding register. With the above procedure, per port security function can limit the MAC address that can be only access from the specific port. Learn_En[2:0] represent {Port2,Port1,Port0}
[15]	Reserved	0	R	Reserved
[24:16]	AgingTimer	0x1FF	RW	Programmable Aging timer for flushing routing table. Default value is 0x1FF.
[25]	Reserved	0	R	Reserved
[28:26]	OneSARst	000	RW	Reset One SA function of Port N. (N=0,1,2) Set 1 to reset One SA function. When reset, Port N will clear previous learning SA MAC address and restart to learn a new SA MAC address. OneSARst[2:0] represent {Port2,Port1,Port0}.
[31:29]	OneSAEn	000	RW	Enable One SA function of Port N (N=0,1,2) One SA function means Port N will only learn and forward the first successfully received packet's SA MAC address. The switch will continue forwarding the following packets but without learning the new SA.If enable One SA function on port N, then the Learn_En bit should also set 0 for port N. OneSAEn[2:0] represent {Port2,Port1,Port0}.

5.1.7 Layer 2 Routing Table Entry Read/Write Register (LRCR0 and LRCR1)

Address 0x018 (LRCR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address [47:40]	0x00	RW	MAC address [47:40] Routing table MAC address entry
[15:8]	MAC_address [39:32]	0x00	RW	MAC address [39:32]
[23:16]	MAC_address [31:24]	0x00	RW	MAC address [31:24]
[31:24]	MAC_address [23:16]	0x00	RW	MAC address [23:16]

Address 0x01C(LRCR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address [15:8]	0x00	RW	MAC address [15:8]
[15:8]	MAC_address [7:0]	0x00	RW	MAC address [7:0]
[17:16]	SrcPort	00	RW	Source port where this Mac Address is located. 00: Source Port 0 01: Source Port 1 10: Source Port 2
[18]	Filter_SA	0	RW	Filter_SA function. Drop the receiving packet if the receiving packet's SA MAC address match with this MAC address and this bit is set to one.
[19]	Filter_DA	0	RW	Filter DA function. Drop the receiving packet if it's DA MAC address match with the MAC address and this bit is set to one.
[20]	Static	0	RW	Static bit. 1: Freeze the entry and never aging out 0: Normal (Default)
[21]	Flush_Done	0	R	Routing table flush done bit (read only) If CPU set LRCR1 [29] = 1 (Flush_RT) , then CPU will keep polling this bit to confirm if the routing table completes flushing function. 1: Routing table flush done. 0: Routing table still flushing.
[23:22]	Search_Port	00	RW	Auto-search routing table source port entry 00: search port 0 entry 01: search port 1 entry 10: search port 2 enrty 11: not allowed
[24]	RT_Valid	0	R	Entry is valid if set to one (read only) 1: valid entry 0: empty entry
[25]	RT_End	0	R	Used in Continuously search mode to designate the end of routing table is reached. Read only.
[26]	RT_N	0	RW	Routing Table Page (2–way 512 Routing Table entry) 0: page 0, 1: page 1
[27]	Conti_RD_RT	0	RW	Continue READ next valid entry inside routing table
[28]	By_Port	0	RW	Read routing table continuously. Please configure Search_port first.

[29]	Flush_RT	0	RW	Clear all 1K routing table entries to 0 if this bit is set to one.
[30]	Read_RT	0	RW	Read Routing Table. This bit needs to clear to 0 before the read start.
[31]	Write_RT	0	WC	Write entry into Routing Table. LRCR0 andLRCR1's MAC address, SrcPort, Static, Filter_DA, and Filter_SA information need to be ready before this bit set.

5.1.8 802.1D and Port-based VLAN Configuration Register (PVCR)

Address 0x020

Bit	Name	Default Value	R/W	Function
[1:0]	1Dport0St	00	RW	Port 0 1D Port State "00" = blocking, disable "01" = listening "10" = learning "11" = forwarding LGCR [23] D1_En need to enable.
[3:2]	1Dport1St	00	RW	Port 1 1D Port State "00" = blocking, disable "01" = listening "10" = learning "11" = forwarding LGCR [23] D1_En need to enable.
[5:4]	1Dport2St	00	RW	Port 2 1D Port State "00" = blocking, disable "01" = listening "10" = learning "11" = forwarding LGCR [23] D1_En need to enable.
[7:6]	Reserved	00	R	Reserved
[10:8]	IngressFilter	000	RW	When enabled, Discard non-member VLAN packets for Tag-based VLAN process. For example: if Port 1 receive a tag frame with VID=4 but the VLAN group information doesn't include Port 1 itself, then if this bit is set to one then the frame will be dropped. LGCR[22] 1Q_En need to enable.
15:11]	Reserved	0x00	R	Reserved
[18:16]	VLANgrp0	000	RW	Port 0 Port-Base VLAN configuration register is used to define non-802.1Q VLAN. Support total 3 Non-802.1Q VLAN. LGCR [20] VLAN_En need to enable first.
[19]	Reserved	0	R	Reserved
[22:20]	VLANgrp1	000	RW	Port 1 Port-Base VLAN configuration register is used to define non-802.1Q VLAN. Support total 3 Non-802.1Q VLAN. LGCR [20] VLAN_En need to enable first.
[23]	Reserved	0	R	Reserved
[26:24]	VLANgrp2	000	RW	Port 2 Port-Base VLAN configuration register is used to define non-802.1Q VLAN. Support total 3 Non-802.1Q VLAN. LGCR [20] VLAN_En need to enable first.
[31:27]	Reserved	0x00	R	Reserved

5.1.9 Sniffer Function Configuration Register (SFCR0, SFCR1, SFCR2)

Sniffer Function Configuration register provides the following sniffer functions:

(1)SP_DP_sniffer
(2)DA_SA_sniffer
(3)VLAN_VID_sniffer
(4)Packet Type_sniffer
(1), (2),(3) and (4) conditions should be all match unless any of these conditions (1 to 4) had default value zero.

5.1.9.1 Sniffer Function Configuration Register 0 (SFCR0)

Address 0x024

Bit	Name	Default Value	R/W	Function
[1:0]	SP_DP_sniffer	00	RW	00: None 01: Sniffer Source Port 10: Sniffer Destination Port 11: Sniffer Source Port & Destination Port
[3:2]	DA_SA_sniffer	00	RW	00: None 01: SA Match 10: DA Match 11: SA & DA Match
[4]	VLAN_VID_sniffer	0	RW	0: None 1: VID Match When enabled, use SFCR1 SnifferVID to sniffer packets.
[5]	Reserved	0	RW	Reserved
[6]	Packet_ype_sniffer	0	RW	0: None 1: Packet Type Match When enabled, Use L2_Type or IPv4_Type or IPv6_Type [7:0] or IP_Port with SFCR2 to sniffer Packet.
[14:7]	IP_Port_sniffer	0x00	RW	IPv4/IPv6 Port Sniffer 0x00: None 0x01: IPv4 TCP Source Port Match 0x02: IPv4 TCP Destination Port Match 0x03: IPv4 TCP Destination Port Match & Source Port Match 0x04: IPv4 UDP Source Port Match 0x08: IPv4 UDP Destination Port Match 0x0C: IPv4 UDP Destination Port Match & Source Port Match 0x10: IPv6 TCP Source Port Match 0x20: IPv6 TCP Destination Port Match 0x30: IPv6 TCP Destination Port Match & Source Port Match 0x40: IPv6 UDP Source Port Match 0x80: IPv6 UDP Destination Port Match 0xC0: IPv6 UDP Destination Port Match & Source Port Match Note: Write Port number on SFCR2
[15]	SnifferEn	0	RW	Enable sniffer function. When the incoming packet matches sniffer condition, that packet will be duplicated to sniffer port. Sniffering condition can be based on the following rule: 1. Source Port or Destination Port 2. DA or SA 3. VID 4. Ethernet Packet Type 5. IPv4 Source Port/Destination Port 6. IPv6 Source Port/Destination Port
[17:16]	SnifferPort	00	RW	The assigned sniffer port. All packets that match the Sniffer rule will duplicate to this sniffer port.
[20:18]	SniffSrcPort	000	RW	Sniffer Source Port. Sniffer Packet that received by Port N. (N=0,1,2) The user can select all 3

				ports at the same time. For example, Select Port 0,1 as Sniffer Source Port, then set the register value to 011. All the packets receive from port 0 and port 1 will duplicate to the assigned sniffer port.
[23:21]	SniffDstPort	000	RW	Sniffer Destination Port. Sniffer Packet that transmit to Port N. (N=0,1,2). The user can select up to 3 ports at the same time. For example, Select Port 0,1 as Sniffer Destination Port, Set register value to 011. And all the packets transmit to port 0 and port1 will duplicate to the assigned sniffer port.
[31:24]	Type_L2	0x00	RW	Sniffer Layer 2 Ethernet Packet Type: Type_L2 [0]: ARP (0x0806), Type_L2 [1]: RARP (0x8035) Type_L2 [2]: MPLS Packet (0x8847 unicast or 0x8848 multicast) Type_L2 [3]: 802.1X (0x888E) Type_L2 [4]: IPX/SNAP (0x8137) Type_L2 [5]: Net Bios (0x8040) Type_L2 [6]: Based on USTR User-Defined packet type (Default: PPPOE Discovery 0x8863) Type_L2 [7]: PPPOE Session (0x8864)

5.1.9.2 Sniffer Function Configuration Register 1 (SFCR1)

Address 0x028

Bit	Name	Default Value	R/W	Function
[7:0]	IPv4_Type	0x00	RW	Pkt_Type_IPV4 [0]: IP Packet (Packet_Type=0x0800 and exclude the following packet type from [1] to [7]) Pkt_Type_IPV4 [1]: TCP (Protocol=6) Pkt_Type_IPV4 [2]: UDP (Protocol=17) Pkt_Type_IPV4 [3]: OSPF (Protocol=89) Pkt_Type_IPV4 [4]: RSVP (Protocol=46) Pkt_Type_IPV4 [5]: Based on USTR User-Defined IPv4 packet type (default: L2TP Protocol=115) Pkt_Type_IPV4 [6]: ICMP (Protocol=1) Pkt_Type_IPV4 [7]: IGMP (Protocol=2)
[14:8]	IPv6_Type	0x00	RW	Pkt_Type_IPV6 [0]: IP Packet (Packet_Type= 0x86DD and exclude the following packet type from [1] to [6]) Pkt_Type_IPV6 [1]: TCP (Protocol=6) Pkt_Type_IPV6 [2]: UDP (Protocol=17) Pkt_Type_IPV6 [3]: OSPF (Protocol=89) Pkt_Type_IPV6 [4]: RSVP (Protocol=46) Pkt_Type_IPV6 [5]: Based on USTR User-Defined IPv6 packet type (default: L2TP Protocol=115) Pkt_Type_IPV6 [6]: ICMP (Protocol=1)
[15]	Reserved	0	R	Reserved
[27:16]	SnifferVID	0x000	RW	Sniffer VLAN ID (VID range from 0 to 4095)
[31:28]	Reserved	0000	R	Reserved

5.1.9.3 Sniffer Function Configuration Register 2 (SFCR2)

Address 0x02C

Bit	Name	Default Value	R/W	Function
[15:0]	Src_Port	0x0000	RW	Valid when SFCR0 IP_Port_sniffer is selected. Source Port number on Layer 3 protocol (IPv4 TCP/UDP or IPv6 TCP/UDP) matches this Src_Port value. For example, when IP_Port_sniffer == 0x01, and Sniffer condition is "IPv4 TCP Source Port Match ". When Source Port number from the incoming TCP Packet matches with this Src_Port value, then this packet will be duplicated and forward to the assigned Sniffer Port.
[31:16]	Dst_Port	0x0000	RW	Valid when SFCR0 IP_Port_sniffer is selected Destination Port number on Layer 3 protocol (IPv4 TCP/UDP or IPv6 TCP/UDP) matches this Dst_Port value For example, when IP_Port_sniffer == 0x02, and Sniffer condition is "IPv4 TCP Destination Port Match ". When Destination Port of incoming TCP Packet matches with this Dst_Port value, then this packet will be duplicated and forward to the assigned Sniffer Port.

5.1.10 QoS Priority Mapping Table Register (QPTR)

Address 0x030

Bit	Name	Default Value	R/W	Function
[1:0]	TOS0	00	RW	TOS Mapping Table. This table coverts IPv4 QoS (Type of Service [7:5] or [4:2] depend on LGCR [0] QoSSel) 3 bit QoS value to any one of the four queues within buffer management unit in the switch engine. If TOS [2:0]==0 then priority value map to TOS0 [1:0]
[3:2]	TOS1	00	RW	If TOS [2:0]==1 then priority value map to TOS1 [1:0]
[5:4]	TOS2	01	RW	If TOS [2:0]==2 then priority value map to TOS2 [1:0]
[7:6]	TOS3	01	RW	If TOS [2:0]==3 then priority value map to TO S3 [1:0]
[9:8]	TOS4	10	RW	If TOS [2:0]==4 then priority value map to TO S4 [1:0]
[11:10]	TOS5	10	RW	If TOS [2:0]==5 then priority value map to TO S5 [1:0]
[13:12]	TOS6	11	RW	If TOS [2:0]==6 then priority value map to TO S6 [1:0]
[15:14]	TOS7	11	RW	If TOS [2:0]==7 then priority value map to TO S7 [1:0]
[17:16]	COS0	00	RW	COS Mapping Table. This table converts IPv6 QoS (Traffic Class [7:5] or [4:2] depend on LGCR [0] QoSSel) 3 bit value to any one of the four queues within buffer management unit in the switch engine. If COS [2:0]==0 then priority value map to COS0 [1:0]
[19:18]	COS1	00	RW	If COS [2:0]==1 then priority value map to COS1 [1:0]
[21:20]	COS2	01	RW	If COS [2:0]==2 then priority value map to COS2 [1:0]
[23:22]	COS3	01	RW	If COS [2:0]==3 then priority value map to COS3 [1:0]
[25:24]	COS4	10	RW	If COS [2:0]==4 then priority value map to COS4 [1:0]
[27:26]	COS5	10	RW	If COS [2:0]==5 then priority value map to COS5 [1:0]
[29:28]	COS6	11	RW	If COS [2:0]==6 then priority value map to COS6 [1:0]
[31:30]	COS7	11	RW	If COS [2:0]==7 then priority value map to COS7 [1:0]

5.1.11 802.1Q-in-1Q (Double-Tagging) Setup Register (QSR)

Address 0x034

Bit	Name	Default Value	R/W	Function
[15:0]	Rgi_sptag	0x0000	RW	Service Provider Tag Register. When PVCR [15] QinQ is set to one, The Service Provider TAG will be inserted into the frame if 1. Receive Port is Access Port (P0MCR/P1MCR/P2MCR [15]=0) or 2. Receive Port is Uplink Port (P0MCR/P1MCR/P2MCR [15]=1) and rgi_tpid is not matched with VLAN Tag When Egress port is Access Port then the Service Provider TAG will be removed.
[31:16]	Rgi_tpid	0x8100	RW	VLAN Tag Register.(Default ox8100) When 1Q-in-1Q is turned ON (PVCR [15]=1), rgi_tpid (type ID) will be compared against all the incoming packets' VLAN Tag field if receive port is an Uplink_Port (P0MCR/P1MCR/P2MCR [15]=1).

5.1.12 Port Pair and MDC Control Register (PPMR)

Address 0x038

Bit	Name	Default Value	R/W	Function
[3:0]	PortPairP0	0000	RW	Define port pair 0 on PortPairP0 [3:2] and PortPairP0 [1:0]
[7:4]	PortPairP1	0000	RW	Define port pair 1 on PortPairP1 [3:2] and PortPairP1 [1:0]
[9:8]	AllBit [1:0]	00	RW	[0]: If this bit is set to one then Port Pair0 will pass all packets based on PortPairPri [1:0] queue setting [1]: if this bit is set to 1 then Port Pair1 will pass all packets based on PortPairPri [1:0] queue setting Note: [3:0] and [7:4] should set to the same port!!
[11:10]	PortPairPri[1:0]	00	RW	Pre-defined Port Pair priority queue number. Assign port pair traffic to the dedicate queue.
[14:12]	Reserved	000	R	Reserved
[15]	PortpairEn	0	RW	Enable Port Pair function
[23:16]	MDC_cyc	0x31	RW	This register is used to set MDC frequency, default value is 0x31, means MDC frequency is 1MHz. The minimum value is 0x4 and the maximum value is 0xFF.The lower the value, the higher the frequency.
[24]	Reserved	0	RW	Reserved. Always set 0 when write PPMR register.
[31:25]	Reserved	0x00	R	Reserved

5.1.13 MDIO Read/Write Control Register (MRCR)

Address 0x03C

Bit	Name	Default Value	R/W	Function
[15:0]	Mdio_Data	0x0000	RW	MDIO data [15:0] When CPU set MDIO read command register to 1, The MDC/MDIO controller will show the read data from PHY register here. When CPU set MDIO write command register to 1, The MDC/MDIO controller will write this register data to the PHY register.
[20:16]	Reg_addr	00000	RW	PHY Register address. CPU should set this register to let the MDC/MDIO controller knows which PHY register to be accessed. Please reference 5.2 PHY register address offset.
[23:21]	Reserved	000	R	Reserved
[28:24]	Phy_addr	00000	RW	PHY Physical ID. CPU should set this register to let the MDC/MDIO controller know what PHY ID to be accessed.
[29]	MDIORD_ok	0	R	MDIO data valid After CPU set the MDIO read command register to one, CPU should continue polling this bit to confirm that the MII management interface read cycle is done and Data [15:0] is also valid. After CPU set the MDIO write command register to one, CPU should continue polling this bit to confirm that the MII management interface write cycle is done. 1: MII management interface read/write cycle is done. 0: MII management interface read/write cycle is not done.
[30]	MDIORead	0	WC	MDIO Read command to PHY 1: Read command 0: Idle CPU should set this bit to one to let the MDC/MDIO controller perform MII management interface read cycle. CPU also needs to program the reg_addr and phy_addr value in MRCR first.
[31]	MDIOWrite	0	WC	MDIO Write command to PHY 1: Write command 0: Idle CPU should set this bit to one to let the MDC/MDIO controller perform MII management interface write cycle. CPU also needs to set the reg_addr , phy_addr and Data register in MRCR first.

5.1.14 TCP/IP Offload Control Register (TOCR)

Address 0x040

Bit	Name	Default Value	R/W	Function
[0]	UDP_InsCRC	0	RW	Insert Hardware calculated UDP Checksum value for packet receive from CPU port 1: Insert Calculated UDP checksum value 0: Normal (Default)
[1]	TCP_InsCRC	0	RW	Insert Hardware calculated TCP Checksum value for packet receive from CPU port 1: Insert Calculated TCP checksum value 0: Normal (Default)
[2]	IGMP_InsCRC	0	RW	Insert Hardware calculated IGMP Checksum value for packet receive from CPU port 1: Insert Calculated IGMP checksum value 0: Normal (Default)
[3]	ICMP_InsCRC	0	RW	Insert Hardware calculated ICMP Checksum value for packet receive from CPU port 1: Insert Calculated ICMP checksum value 0: Normal (Default)
[4]	IP_InsCRC	0	RW	Insert Hardware calculated IPv4 Checksum value for packet receive from CPU port 1: Insert Calculated IPv4 IP checksum value 0: Normal (Default)
[5]	PPPoE_InsCRC	0	RW	Insert Hardware calculated PPPoE Checksum value for packet receive from CPU port 1: Enable PPPoE checksum offload function on [0:4] enabled protocols. 0: Normal (Default)
[6]	Reserved	0	RW	Always assign zero
[7]	Reserved	0	R	Reserved
[8]	UDP_DropCrc	0	RW	Drop RX packet when detect UDP checksum error for packet receive from Port 0 and Port 1 1: Drop Bad UDP checksum frame 0: Normal (Default)
[9]	TCP_DropCrc	0	RW	Drop RX packet when detect TCP checksum error for packet receive from Port 0 and Port 1 1: Drop Bad TCP checksum frame 0: Normal (Default)
[10]	IGMP_DropCrc	0	RW	Drop RX packet when detect IGMP checksum error for packet receive from Port 0 and Port 1 1: Drop Bad IGMP checksum frame 0: Normal (Default)
[11]	ICMP_DropCrc	0	RW	Drop RX packet when detect ICMP checksum error for packet receive from Port 0 and Port 1 1: Drop Bad ICMP checksum frame 0: Normal (Default)
[12]	IP_DropCrc	0	RW	Drop RX packet when detect IPv4 checksum error for packet receive from Port 0 and Port 1 1: Drop Bad IPv4 IP checksum frame 0: Normal (Default)
[13]	PPPoE_DropCrc	0	RW	Drop RX packet when detect PPPoE checksum error for packet receive from Port 0 and Port 1 1: Drop Bad PPPoE checksum frame on [8:12] enabled protocols. 0: Normal (Default)
[14]	Reserved	0	R	Reserved

[15]	Clr_rxdrop_cntr	0	WC	Clear Pot 0 and Port 1's RX TCP/IP checksum drop frame counters.
[31:16]	Reserved	0x0000	R	Reserved

5.1.15 CPIO Control Register (CCR)

Address 0x04C

Bit	Name	Default Value	R/W	Function
[31:0]	CPOData [31:0]	0x0000 0000	WC	When the CPU write operation is enabled, the CPU will transfer CPU_DATA [31:0] to this register value and later copy to the internal RX FIFO. When the CPU read operation is enabled. The CPOData [31:0] value will transfer to CPU data Bus CPU_DATA [31:0].

5.1.16 Security Mac Control Registers

There are eight extra security MAC addresses in the AX88782/AX88783.Each Security MAC register can be set for the following purpose:

1. As a supplement to the limit of 2-way hashing routing table. When hashing collision happens, these security MAC registers can be set by CPU to avoid flooding.
2. Sniffer function: Duplicate packets to the assigned Sniffer Port when DA or SA or DA & SA match. Sniffer Pair bit (SnifferPair) must be enabled in pair.
   For Example, assume Security MAC0 and MAC1 are paired.
   i. Set SM0CR1 and SM1CR1 both SnifferPair[20] bits to one
   ii. Set SM0CR1 Sniffer_SA and SM1CR1 Sniffer_DA to one
   iii. Set SFCR0 DA_SA_sniffer=2'b11
   iv. Chose Sniffer port in SFCR0's SnifferPort.
   Then any packets with a SA MAC address matched with the security Mac0 and DA MAC address matched with security MAC1 will forward to the assigned sniffer port..
3. Security function: Filtering packets when DA or SA or DA & SA match. Drop Pair bit (Filter_Pair) must be enabled in pair also.
   Note1: Security MAC 0 and Security MAC 1 can be paired if SnifferPair or Filter_Pair bit is set to one. Security MAC 2 and Security MAC 3, Security MAC 4 and Security MAC 5, Security MAC 6 and Security MAC 7, can all be paired together.
   Note2: En_RT and Filter_DA/SA and DA_SA_sniffer (SnifferEn=1) can't enable at the same time!
   Note3: MAC address and source port information need to be matched!
4. Support 802.1X security function: The global 802.1X enable bit in LGCR 1X_En and Per port 802.1X enable bits in PMCR0/PMCR1/PMCR2 1XsecurityON need to enable first before turn on the X1SA_match security function within these security MAC registers.

5.1.16.1 Security Mac 0 Control Register (SM0CR0, SM0CMR1)

Address 0x050 (SM0CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 0 [47:40]	0x00	RW	Security MAC address 0 [47:40]
[15:8]	MAC_address 0 [39:32]	0x00	RW	Security MAC address 0 [39:32]
[23:16]	MAC_address 0 [31:24]	0x00	RW	Security MAC address 0 [31:24]
[31:24]	MAC_address 0 [23:16]	0x00	RW	Security MAC address 0 [23:16]

Address 0x054 (SM0CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 0 [15:8]	0x00	RW	Security MAC address 0 [15:8]
[15:8]	MAC_address 0 [7:0]	0x00	RW	Security MAC address 0 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 0.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 0.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 0 and DA MAC or SA MAC matches the security MAC address 1.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 0 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC Address 0 & DA MAC or SA MAC matches with the security MAC Address 1.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 0.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 0.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 0.

5.1.16.2 Security Mac 1 Control Register (SM1CR0, SM1CR1)

Address 0x058 (SM1CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 1 [47:40]	0x00	RW	Security MAC address 1 [47:40]
[15:8]	MAC_address 1 [39:32]	0x00	RW	Security MAC address 1 [39:32]
[23:16]	MAC_address 1 [31:24]	0x00	RW	Security MAC address 1 [31:24]
[31:24]	MAC_address 1 [23:16]	0x00	RW	Security MAC address 1 [23:16]

Address 0x05C (SM1CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 1 [15:8]	0x00	RW	Security MAC address 1 [15:8]
[15:8]	MAC_address 1 [7:0]	0x00	RW	Security MAC address 1 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 1.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 1.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 0 and DA MAC or SA MAC matches the security MAC address 1.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 1 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 0 and DA MAC or SA MAC matches with the security MAC Address 1.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 1.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 1.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 1.

5.1.16.3 Security Mac 2 Control Register (SM2CR0, SM2CR1)

Address 0x060 (SM2CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 2 [47:40]	0x00	RW	Security MAC address 2 [47:40]
[15:8]	MAC_address 2 [39:32]	0x00	RW	Security MAC address 2 [39:32]
[23:16]	MAC_address 2 [31:24]	0x00	RW	Security MAC address 2 [31:24]
[31:24]	MAC_address 2 [23:16]	0x00	RW	Security MAC address 2 [23:16]

Address 0x064 (SM2CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 2 [15:8]	0x00	RW	Security MAC address 2 [15:8]
[15:8]	MAC_address 2 [7:0]	0x00	RW	Security MAC address 2 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 2.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 2.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 2 and DA MAC or SA MAC matches the security MAC address 3.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 2 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 2 and DA MAC or SA MAC matches with the security MAC Address 3.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 2.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 2.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 2.

5.1.16.4 Security Mac 3 Control Register (SM3CR0, SM3CR1)

Address 0x068 (SM3CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 3 [47:40]	0x00	RW	Security MAC address 3 [47:40]
[15:8]	MAC_address 3 [39:32]	0x00	RW	Security MAC address 3 [39:32]
[23:16]	MAC_address 3 [31:24]	0x00	RW	Security MAC address 3 [31:24]
[31:24]	MAC_address 3 [23:16]	0x00	RW	Security MAC address 3 [23:16]

Address 0x06C (SM3CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 3 [15:8]	0x00	RW	Security MAC address 3 [15:8]
[15:8]	MAC_address 3 [7:0]	0x00	RW	Security MAC address 3 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 3.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 3.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 2 and DA MAC or SA MAC matches the security MAC address 3.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 3 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 2 and DA MAC or SA MAC matches with the security MAC Address 3.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 3.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 3.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 3.

5.1.16.5 Security Mac 4 Control Register (SM4CR0, SM4CR1)

Address 0x070 (SM4CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 4 [47:40]	0x00	RW	Security MAC address 4 [47:40]
[15:8]	MAC_address 4 [39:32]	0x00	RW	Security MAC address 4 [39:32]
[23:16]	MAC_address 4 [31:24]	0x00	RW	Security MAC address 4 [31:24]
[31:24]	MAC_address 4 [23:16]	0x00	RW	Security MAC address 4 [23:16]

Address 0x074 (SM4CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 4 [15:8]	0x00	RW	Security MAC address 4 [15:8]
[15:8]	MAC_address 4 [7:0]	0x00	RW	Security MAC address 4 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 4.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 4.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 4 and DA MAC or SA MAC matches the security MAC address 5.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 4 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 4 and DA MAC or SA MAC matches with the security MAC Address 5.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 4.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 4.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 4.

5.1.16.6 Security Mac 5 Control Register (SM5CR0, SM5CR1)

Address 0x078 (SM5CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 5 [47:40]	0x00	RW	Security MAC address 5 [47:40]
[15:8]	MAC_address 5 [39:32]	0x00	RW	Security MAC address 5 [39:32]
[23:16]	MAC_address 5 [31:24]	0x00	RW	Security MAC address 5 [31:24]
[31:24]	MAC_address 5 [23:16]	0x00	RW	Security MAC address 5 [23:16]

Address 0x07C (SM5CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 5 [15:8]	0x00	RW	Security MAC address 5 [15:8]
[15:8]	MAC_address 5 [7:0]	0x00	RW	Security MAC address 5 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 5.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 5.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 4 and DA MAC or SA MAC matches the security MAC address 5.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 5 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 4 and DA MAC or SA MAC matches with the security MAC Address 5.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 5.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 5.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 5.

5.1.16.7 Security Mac 6 Control Register (SM6CR0, SM6CR1)

Address 0x080 (SM6CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 6 [47:40]	0x00	RW	Security MAC address 6 [47:40]
[15:8]	MAC_address 6 [39:32]	0x00	RW	Security MAC address 6 [39:32]
[23:16]	MAC_address 6 [31:24]	0x00	RW	Security MAC address 6 [31:24]
[31:24]	MAC_address 6 [23:16]	0x00	RW	Security MAC address 6 [23:16]

Address 0x084 (SM6CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 6 [15:8]	0x00	RW	Security MAC address 6 [15:8]
[15:8]	MAC_address 6 [7:0]	0x00	RW	Security MAC address 6 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 6.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 6.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 6 and DA MAC or SA MAC matches the security MAC address 7.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 6 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 6 and DA MAC or SA MAC matches with the security MAC Address 7.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 6.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 6.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 6.

5.1.16.8 Security Mac 7 Control Register (SM7CR0, SM7CR1)

Address 0x088 (SM7CR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 7 [47:40]	0x00	RW	Security MAC address 7 [47:40]
[15:8]	MAC_address 7 [39:32]	0x00	RW	Security MAC address 7 [39:32]
[23:16]	MAC_address 7 [31:24]	0x00	RW	Security MAC address 7 [31:24]
[31:24]	MAC_address 7 [23:16]	0x00	RW	Security MAC address 7 [23:16]

Address 0x08C (SM7CR1)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC_address 7 [15:8]	0x00	RW	Security MAC address 7 [15:8]
[15:8]	MAC_address 7 [7:0]	0x00	RW	Security MAC address 7 [7:0]
[17:16]	Src_Port	00	RW	Source Port ID.
[18]	Sniffer_SA	0	RW	Copy the packet to the Sniffer Port if SA MAC matches with the security MAC address 7.
[19]	Sniffer_DA	0	RW	Copy the packet to the Sniffer Port if DA MAC matches with the security MAC address 7.
[20]	SnifferPair	0	RW	Copy the packet to the Sniffer Port if DA MAC or SA MAC matches with the security MAC address 6 and DA MAC or SA MAC matches the security MAC address 7.
[26:21]	Reserved	0x00	R	Reserved
[27]	X1_SAMatch	0	RW	Forward the packet if SA MAC matches with the security MAC Address 7 if the 802.1X is enabled, else drop the packet.
[28]	Filter_Pair	0	RW	Drop the packet if DA MAC or SA MAC matches with the security MAC address 6 and DA MAC or SA MAC matches with the security MAC Address 7.
[29]	Filter_SA	0	RW	Drop the packet if SA MAC matches with the security MAC address 7.
[30]	Filter_DA	0	RW	Drop the packet if DA MAC matches with the security MAC address 7.
[31]	En_RT	0	RW	Enable routing function if DA matches with the security MAC address 7.

5.1.17 VLAN Entry Registers

5.1.17.1 VLAN Entry 0 Register (VER0)

Address 0x090

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 0 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.2 VLAN Entry 1 Register (VER1)

Address 0x094

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 1 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.3 VLAN Entry 2 Register (VER2)

Address 0x098

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 2 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.4 VLAN Entry 3 Register (VER3)

Address 0x09C

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 3 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.5 VLAN Entry 4 Register (VER4)

Address 0x0A0

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 4 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.6 VLAN Entry 5 Register (VER5)

Address 0x0A4

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 5 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.7 VLAN Entry 6 Register (VER6)

Address 0x0A8

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 6 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.8 VLAN Entry 7 Register (VER7)

Address 0x0AC

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 7 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.9 VLAN Entry 8 Register (VER8)

Address 0x0B0

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 8 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.10 VLAN Entry 9 Register (VER9)

Address 0x0B4

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 9 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.11 VLAN Entry 10 Register (VER10)

Address 0x0B8

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 10 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.12 VLAN Entry 11 Register (VER11)

Address 0x0BC

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 11 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.13 VLAN Entry 12 Register (VER12)

Address 0x0C0

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 12 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.14 VLAN Entry 13 Register (VER13)

Address 0x0C4

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 13 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.15 VLAN Entry 14 Register (VER14)

Address 0x0C8

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 14 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.17.16 VLAN Entry 15 Register (VER15)

Address 0x0CC

Bit	Name	Default Value	R/W	Function
[2:0]	Forward	000	RW	VLAN group forwarding information {Port2, Port1, Port0} 1: Same VLAN group port 0: Not Same VLAN group
[5:3]	Tag	000	RW	Define output packet with Tag or without Tag control {Port2, Port1, Port0} 1: Tag frame 0: Un-Tag frame
[17:6]	VID	0x000	RW	Full range VID (1 ~ 4095)
[18]	Valid	0	RW	VLAN Entry 15 Valid bit 1: Valid 0: Not valid
[31:19]	Reserved	0x0000	R	Reserved

5.1.18 CPIO Byte Order Register (CBOR)

Address 0x0D0

Bit	Name	Default Value	R/W	Function
[1:0]	CPIOByteOrder	00	RW	Data Byte Re-Order for CPU 00: DATA [31:0] (Default) 01: {Data [7:0], Data [15:8], Data [23:16], Data [31:24]} 10: {Data [23:16], Data [31:24], Data [7:0], Data [15:8]} 11: {Data [15:8], Data [7:0], Data [31:24], Data [23:16]} The AX88782/AX88783 support different type of byte swapping on CPU interface by configured this register.
[31:2]	Reserved	0x0000 0000	R	Reserved

5.1.19 CPIO Start Command Register (CSCR)

Address 0x0D4

Bit	Name	Default Value	R/W	Function
[14:0]	Reserved	0x00	R	Reserved
[15]	CPIStart	0	RW	Set CPIStart to one before transfer packet date into the switch. CPU writes the packet data into the AX88782/AX88783 CPU data bus pins.
[30:16]	Reserved	0x00	R	Reserved
[31]	CPOStart	0	RW	Set CPOStart to one before read packet data from switch. CPU reads the packet data out from the AX88782/AX88783 CPU data bus pins.

5.1.20 IGMP Table Read/Write Control Register (ITCR)

Address 0x0D8

Bit	Name	Default Value	R/W	Function
[0]	MC_Src_Filter	0	RW	Layer 2 Multicast Source Port Filter Enable 1: Drop the multicast packet if source port isn't belong to this multicast group 0: Broadcast the multicast packet if source port is not belong to this multicast group For example, Assume the static multicast MAC address (01-00-00-00-00-01) in the routing table only register port 0 and port 1 as port map group, if port 2 receive this registered multicast packet then forwarding engine will either drop or broadcast this multicast packet depend on MC_Src_Filter setting.
[1]	MCIP_Mode	0	RW	IGMP Multicast IP Mode Enable. 0: Drop this multicast IP packet if not found in the IGMP table 1: Broadcast the unknown IP multicast packet if not found in the IGMP table
[6:2]	IPv6_Snooping [4:0]	00000	RW	IPv6 Snooping Control Register [0]: Snooping IPv6 ICMPv4 packet to CPU port The following condition need to be matched: 1. IPv6 Multicast Packet 2. Next header =1 or Next header =0 and extend Next header1=1 3. Hop limit = 1 [1]: Snooping IPv6 ICMPv6 packet to CPU port. The following condition need to be matched: 1. IPv6 Multicast Packet 2. Next header =58 or Next header =0 and extend Next header1=58 3. Hop limit = 1 [2]: Snooping all the ICMPv4/IPv6 Packets and hop limit=1 to the CPU port. [3]: Snooping all the ICMPv6/IPv6 Packets and hop limit=1 to the CPU port. [4]: Snooping all the IPv6 packets with Next header = 43, 44, 50, 51 and 60 to the CPU port.
[7]	IPv6_Snooping En	0	RW	IPv6 Snooping function Enable 1: Enable IPv6_Snooping [4:0] function 0: Normal (Default)
[9:8]	Reserved	00	RW	Reserved
[15:10]	Reserved	000000	R	Reserved
[17:16]	Reserved	00	RW	Reserved
[23:18]	Reserved	000000	R	Reserved
[25:24]	Reserved	00	RW	Reserved
[31:26]	Reserved	000000	R	Reserved

5.1.21 LED Control Register (LCR)

Address 0x0DC

Bit	Name	Default Value	R/W	Function
[7:0]	Sel_led0[7:0]	0x00	RW	Select LED PIN0 output function [7] FullDuplex/Collision [6] 10Base-T [5] Collision [4] TX activity [3] RX activity [2] Link/Act. [1] Full duplex [0] 100Base-TX NOTE: The user can turn on multiple functions at the same time.For example, Sel_led0=00011000 then any RX or TX activity will turn on the LED light on LED0 pin.
[15:8]	Sel_led1[7:0]	0x00	RW	Select LED PIN1 output function [7] Full Duplex/Collision [6] 10Base-T [5] Collision [4] TX activity [3] RX activity [2] Link/Act. [1] Full duplex [0] 100Base-TX NOTE: The user can turn on multiple functions at the same time.
[23:16]	Sel_led2[7:0]	0x00	RW	Select LED PIN2 output function [7] FullDuplex/Collision [6] 10Base-T [5] Collision [4] TX activity [3] RX activity [2] Link /Act. [1] Full duplex [0] 100Base-TX NOTE: The user can turn on multiple functions at the same time. Only AX88783 support this LED function
[25:24]	En_led	00	RW	Enable PHY0 or PHY1's LED signal output otherwise LED will stay high (turn off) 00: Turn off both PHY0 and PHY1 LED function 01: Enable PHY0 LED function 10: Enable PHY1 LED function 11: Enable both PHY0 and PHY1 LED function
[31:26]	Reserved	0x00	R	Reserved

5.1.22 RMON Control Register (RCR)

Address 0x0E0

Bit	Name	Default Value	R/W	Function
[3:0]	TxMaxCols	0000	RW	Define the collision count for RMON counter offset 0x1D TX Packet with Multiple Collision Counter. For example, TxMaxCols=0101 then the RMON offset 0x1D multiple collision counter will be based on the collision count=5 to count the collision events.
[4]	ClrAllCounter	0	WC	Write 1 to Clear all RMON counters of all ports.
[7:5]	Reserved	000	R	Reserved
[14:8]	RmonAddr [6:0]	0x00	RW	RmonAddr [6:5] is port address index 00: Port 0 01: port 1 10: port 2 RmonAddr [4:0] is the RMON counter offset address. There are 30 counters per port. Please reference RDR for each counter's function.
[15]	CpuRdRmon	0	WC	Write 1 to read RMON
[31:16]	Reserved	0x0000	R	Reserved

Note: Pause Frame will not be counted as multicast frame. RMON multicast counter will not include pause frame count.

5.1.23 RMON Data Register (RDR)

Address 0x0E4

Bit	Name	Default Value	R/W	Function
[31:0]	RmonData	0x0000 0000	R	RMON Data value [31:0]

Rmon Addr	Counter	Description
0x00	Rx Packet Counter	The total number of packets received (include bad packets)
0x01	Rx Good Packet Counter	The total number of good packets received.
0x02	Rx Byte Counter (low 32 bit)	The total number of bytes received (include bad packets).
0x03	Rx Byte Counter (high 32 bit)	
0x04	Rx Broadcast Packet Counter	The total number of good broadcast packets received.
0x05	Rx Multicast Packet Counter	The total number of good multicast packets received.
0x06	Rx PAUSE Frame Counter	The total number of PAUSE frames received.
0x07	Rx Packet Length Counter 1	The total number of packets received that length is less than 64 bytes (include bad packets).
0x08	Rx Packet Length Counter 2	The total number of packets received that length is 64 bytes (include bad packets).
0x09	Rx Packet Length Counter 3	The total number of packets received that length is between 65 bytes and 127 bytes (include bad packets).
0x0A	Rx Packet Length Counter 4	The total number of packets received that length is between 128 bytes and 255 bytes (include bad packets).
0x0B	Rx Packet Length Counter 5	The total number of packets received that length is between 256 bytes and 511 bytes (include bad packets).
0x0C	Rx Packet Length Counter 6	The total number of packets received that length is between 512 bytes and 1023 bytes (include bad packets).
0x0D	Rx Packet Length Counter 7	The total number of packets received that length is between 1024 bytes and maximum bytes (include bad packets).
0x0E	Rx Packet Length Counter 8	The total number of packets received that length is longer maximum bytes (include bad packets).
0x0F	Rx CRC Error Packet Counter	The total number of packets with CRC error received.
0x10	Rx Alignment Error Packet Counter	The total number of packets with Alignment error received and less than maximum packet size.
0x11	Fragment Error Counter	The total number of packets received that are less than 64 bytes, but has an either CRC error or Alignment Error.
0x14	TX Packet Counter	The total number of packets transmitted or aborted.
0x15	TX Good Packet Counter	The total number of good packets transmitted successfully.
0x16	TX Byte Counter (low 32 bit)	The total number of bytes transmitted or aborted.
0x17	TX Byte Counter (high 32 bit)	
0x18	TX Broadcast Packet Counter	The total number of good broadcast packets transmitted successfully.
0x19	TX Multicast Packet Counter	The total number of good multicast packets transmitted successfully.
0x1A	TX PAUSE Frame Counter	The total number of PAUSE frames transmitted.
0x1B	TX Collision Counter	The total number of collisions occurred.
0x1C	TX Packet with one Collision Counter	The total number of packets transmitted successfully which experienced one collision.
0x1D	TX Packet with Multiple Collision Counter	The total number of packets transmitted successfully which experienced multiple collisions.
0x1E	TX Excessive Collision Counter	The total number of packets aborted due to experienced excessive collisions.
0x1F	TX Late Collision Counter	The total number of packets experienced late collisions.

5.1.24 DSCP QoS mapping table Register (DQR0, DQR1, DQR2, DQR3)

Address 0x0E8 (DQR0)

Bit	Name	Default Value	R/W	Function
[31:0]	DSCP0	0x0000 0000	RW	Map DSCP [5:0] (Refer to Fig 17) 64 level into one of the internal four possible queues [1:0]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=0 [3:2]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=1 [5:4]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=2 [7:6]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=3 [9:8]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=4 [11:10]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=5 [13:12]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=6 [15:14]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=7 [17:16]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=8 [19:18]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=9 [21:20]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=10 [23:22]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=11 [25:24]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=12 [27:26]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=13 [29:28]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=14 [31:30]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=15

Address 0x0EC (DQR1)

Bit	Name	Default Value	R/W	Function
[31:0]	DSCP1	0x0000 0000	RW	Map DSCP [5:0] 64 level into internal four possible queues [1:0]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=16 [3:2]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=17 [5:4]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=18 [7:6]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=19 [9:8]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=20 [11:10]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=21 [13:12]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=22 [15:14]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=23 [17:16]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=24 [19:18]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=25 [21:20]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=26 [23:22]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=27 [25:24]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=28 [27:26]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=29 [29:28]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=30 [31:30]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=31

Address 0x0F0 (DQR2)

Bit	Name	Default Value	R/W	Function
[31:0]	DSCP2	0x0000 0000	RW	Map DSCP [5:0] 64 level into internal four possible queues [1:0]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=32 [3:2]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=33 [5:4]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=34 [7:6]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=35 [9:8]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=36 [11:10]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=37 [13:12]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=38 [15:14]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=39 [17:16]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=40 [19:18]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=41 [21:20]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=42 [23:22]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=43 [25:24]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=44 [27:26]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=45 [29:28]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=46 [31:30]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=47

Address 0x0F4 (DQR3)

Bit	Name	Default Value	R/W	Function
[31:0]	DSCP3	0x0000 0000	RW	Map DSCP [5:0] 64 level into internal four possible queues [1:0]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=48 [3:2]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=49 [5:4]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=50 [7:6]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=51 [9:8]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=52 [11:10]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=53 [13:12]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=54 [15:14]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=55 [17:16]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=56 [19:18]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=57 [21:20]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=58 [23:22]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=59 [25:24]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=60 [27:26]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=61 [29:28]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=62 [31:30]: Mapping to internal queue (0 ~ 3) when DSCP [5:0]=63

5.1.25 Interrupt Status and Mask Register (ISMR)

Address 0x0F8

Bit	Name	Default Value	R/W	Function
[0]	AgingOut_st	0	RW	Routing Table entry aging out interrupt status bit This interrupt indicates one of routing table entry was aging out. CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When one of routing table entry was aging out, the interrupt status will change to active.
[1]	NewLearn_st	0	RW	Routing Table learn new SA entry interrupt status bit This interrupt indicates the routing table learns a new source MAC address. CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When learning a new source MAC address, the interrupt status will change to active.
[2]	CPIError_st	0	RW	CPI Error detection interrupt status bit CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When CPI detects error, the interrupt status will change to active.
[3]	CPOEmpty_st	0	RW	CPO Empty interrupt status bit CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When CPO FIFO is empty then this interrupt status will change to active.
[4]	CPIFlowCtrlOn_st	0	RW	CPI Flow Control On interrupt status bit CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When CPI flow control is on then this interrupt status will change to active.
[5]	CPIFlowCtrlOff_st	0	RW	CPI Flow Control Off interrupt status bit CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When CPI flow control off is detected then this interrupt status will change to active.
[6]	LinkChange_st	0	RW	Port0~2 link change when auto-polling enable interrupt status bit. This interrupt indicate one of three ports has a link change event detected. CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When link change event occurs, the interrupt status will change to active. Auto-polling function needs to be enabled for this interrupt.
[11:7]	Reserved	00000	RW	Reserved
[12]	TimerUp_st	0	RW	General Timer up interrupt status bit This interrupt indicate General Timer (STCR) is up. CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive. When timer reaches the limit, the interrupt status will change to active.
[13]	SlaveMDIO_st	0	RW	Slave MDC/MDIO receive write command interrupt status bit When port 2 configures to Reverse MII/RMII mode, CPU needs to enable the

				Slave MDC/MDIO function to let external MII/RMII MAC to perform MII management read/write operation. If the external MII/RMII MAC performs MII management write cycle, this interrupt bit will active. CPU needs to write one to clear this interrupt. 1:interrupt active. 0:interrupt inactive. When the Slave MDC/MDIO receives write command, the interrupt status bit will become active.
[14]	GPIO_Int_st	0	R	GPIO interrupt status bit CPU needs to write one to clear this interrupt status. 1:interrupt active. 0:interrupt inactive.
[15]	Reserved	0	R	Reserved
[16]	AgingOut_mk	1	RW	Routing Table entry aging out interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out AgingOut interrupt. 1: Mask AgingOut interrupt on INT pin. 0: Unmask AgingOut interrupt on INT pin.
[17]	NewLearn_mk	1	RW	Routing Table learn new SA entry interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out the NewLearn interrupt. 1: Mask NewLearn interrupt on INT pin. 0: Unmask NewLearn interrupt on INT pin.
[18]	CPIError_mk	1	RW	CPI Error detection interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out CPI Error interrupt. 1: Mask CPIError interrupt on INT pin. 0: Unmask CPIError interrupt on INT pin.
[19]	CPOEmpty_mk	1	RW	CPO Empty interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out CPO empty interrupt. 1: Mask CPOEmpty interrupt on INT pin. 0: Unmask CPOEmpty interrupt on INT pin.
[20]	CPIFlowCtrlOn_mk	1	RW	CPI Flow Control On interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out CPIFlowCtrlOn interrupt. 1: Mask CPIFlowCtrlOn interrupt on INT pin. 0: Unmask CPIFlowCtrlOn interrupt on INT pin.
[21]	CPIFlowCtrlOff_mk	1	RW	CPI Flow Control Off interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out CPIFlowCtrlOff interrupt. 1: Mask CPIFlowCtrlOff interrupt on INT pin. 0: Unmask CPIFlowCtrlOff interrupt on INT pin.
[22]	LinkChange_mk	1	RW	Port0~2 link change when auto-polling enable interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out LinkChange interrupt. 1: Mask LinkChange interrupt on INT pin. 0: Unmask LinkChange interrupt on INT pin.
[27:23]	Reserved	11111	RW	Reserved
[28]	TimerUp_mk	1	RW	Internal Hardware Timer up interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out TimerUp interrupt. 1: Mask TimerUp interrupt on INT pin. 0: Unmask TimerUp interrupt on INT pin.
[29]	SlaveMDIO_mk	1	RW	Slave MDC/MDIO receive write command interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out SlaveMDIO interrupt.

				1: Mask SlaveMDIO interrupt on INT pin. 0: Unmask SlaveMDIO interrupt on INT pin.
[30]	GPIO_Int_mk	1	RW	GPIO interrupt mask bit When this mask bit is set to one, the hardware INT pin will mask out GPIO_Int interrupt. 1: Mask GPIO_Int interrupt on INT pin. 0: Unmask GPIO_Int interrupt on INT pin.
[31]	Reserved	1	RW	Reserved

5.1.26 User-Defined Sniffer Packet Type Register (USTR)

Address 0x100

Bit	Name	Default Value	R/W	Function
[15:0]	EthType [15:0]	0x8863	RW	User-Defined Sniffer Ethernet Packet Type register (Default: 0x8863 Seccsion Discovery) If the SFCR0 Type_L2 [6] is set to one, then the sniffer logic will copy the packet to sniffer port if the packets layer 2 protocol matches with this value.
[23:16]	IPv4Type [7:0]	0x73	RW	User-Defined Sniffer IPv4 Packet Protocol register (Default: 0x73 L2TP) If the SFCR1 Type_IPv4 [5] is set to one, then the sniffer logic will copy the packet to sniffer port if the packets IPv4 protocol matches with this value.
[31:24]	IPv6Type [7:0]	0x73	RW	User-Defined Sniffer IPv6 Packet Protocol register (Default: 0x73 L2TP) If the SFCR1 Type_IPv6 [5] is set to one, then the sniffer logic will copy the packet to sniffer port if the packets IPv6 protocol matches with this value.

5.1.27 Wake-On-LAN Configuration Register (WCR)

Address 0x104

Bit	Name	Default Value	R/W	Function
[0]	En_linkchange0	0	RW	Enable Port 0 link status change as one of the wake up condition. Wakeup condition: PHY0 link done status toggle from low to high or high to low. 1: Enable 0: Disable
[1]	En_MagicPacket0	0	RW	Enable Port 0 Magic Packet detection as one of the wake up condition. Wakeup condition: Detect 0xFFFFFFFFFFFF follow by repeated 16 times DA_MAC (P0DAR0) pattern anywhere within the payload and good CRC value present. 1: Enable 0: Disable
[2]	En_WakeUpframe0	0	RW	Enable Port 0 Microsoft wakeup frame detector as one of the wakeup condition. Wakeup condition: Calculate CRC value across all the mask bits that match the expected CRC value and the packet has a good CRC value in the end. 1: Enable 0: Disable
[4:3]	En_cascade0 [1:0]	00	RW	Enable cascade function on Port 0 01: cascade offset0 and offset1 together 10: cascade offset1 and offset2 together 11: cascade offset0, offset1, and offset2 all three pointer together 00: disable cascade function
[5]	En_linkchange1	0	RW	Enable Port 1 link status change as one of the wake up condition Wakeup condition: PHY1 link done status toggle from low to high or high to low. 1: Enable 0: Disable
[6]	En_MagicPacket1	0	RW	Enable Port 1 Magic Packet detection as one of the wake up condition. Wakeup condition: Detect 0xFFFFFFFFFFFF follow by repeated 16 times DA_MAC (P0DAR0) pattern anywhere within the payload and good CRC value present. 1: Enable 0: Disable
[7]	En_WakeUpframe1	0	RW	Enable Port 1 Microsoft wakeup frame detector as one of the wakeup condition. Wakeup condition: Calculate CRC value across all the mask bits that match the expected CRC value and the packet has a good CRC value in the end. 1: Enable 0: Disable
[9:8]	En_cascade1 [1:0]	00	RW	Enable cascade function on Port 1 01: cascade offset0 and offset1 together 10: cascade offset1 and offset2 together 11: cascade offset0-2 all three pointer together 00: disable cascade function
[10]	Wakeup_switchon	0	RW	1: Switch-ON mode enabled when this bit is set to one. During the wakeup mode, the switch will continue switching packet between port 0 and port 1. 0: Switch-OFF mode, disable switching packet when in wakeup mode.
[13:11]	Reserved	000	R	Reserved
[14]	Wake_up0	0	R	Wakeup Event detect on port 0 1: Port 0 wake up

				0: Port 0 not wake up
[15]	Wake_up1	0	R	Wakeup event detect on port 1 1: Port 1 wake up 0: Port 1 not wake up
[16]	Wakeup mode	0	RW	1: Enable Wake-On-LAN detection function 0: Disable Wakeup mode
[17]	Sleep mode	0	RW	1: Sleep/Suspend Mode. The switch will turn off all the internal clocks. And the chip is in the minimum power consumption state. 0: Disable sleep mode The user can write any value to address 0x1F4(SMER) to exit the sleep mode!
[18]	Clear_wakeup	0	RW	Clear wakeup signal when CPU is already inform to wake up by writing one to clear the wakeup status. 1: Clear the wake up mode 0: Normal (Default)
[19]	Clear_ sleep_status	0	RW	In normal mode, write one to clear the sleep mode status when back from sleep mode operation. 1: Clear sleep mode status bit 0: Normal
[20]	Wakeup_level	1	RW	1: define PME pin is level sensitive. 0: define PME pin is active low or tri-state.
[21]	Wakeup_pulse	0	RW	1: define PME pin is a pulse signal. 0: define PME pin is a level signal.
[22]	Wakeup_active	1	RW	PME pin active state 1: PME pin is active high 0: PME pin is active low Wakeup_level=1 / Wakeup_pulse=0 / Wakeup_pulse=1 Wakeup_active=0 / Low / ____ ____ |___| Wakeup_active=1 / High / ____ ____| |___ Wakeup_level=0 (Default Hi-Z, active low) / zzzzzzz zzzzzz |_____|
[23]	Reset_pme	0	RW	Reset PME pin to default value before re-start WOL detection 1: Reset PME 0: Normal
[24]	Linkchange_status[0]	0	R	Link change status on port 0 1: Link change event found on port 0 0: Idle
[25]	MagicPacket_status[0]	0	R	Magic frame detection status on port 0 1: Magic Frame found on port 0 0: Idle
[26]	WakeUpframe_status[0]	0	R	Microsoft wakeup detection status on port 0 1: Microsoft wakeup frame found on port 0 0: Idle
[27]	Linkchange_status[1]	0	R	Link change status on port 1 1: Link change event found on port 1 0: Idle
[28]	MagicPacket_status[1]	0	R	Magic frame detection status on port 1 1: Magic Frame found on port 1 0: Idle
[29]	WakeUpframe_status[1]	0	R	Microsoft wakeup detection status on port 1 1: Microsoft wakeup frame found on port 1 0: Idle
[30]	Reserved	0	R	Reserved
[31]	PME	0	R	Power Management Enable status (Read only) PME pin status

5.1.28 Wake-ON-LAN Setup Register (WSR)

Address 0x108

Bit	Name	Default Value	R/W	Function
[3:0]	P0_offset0	0000	RW	Filter 0 Double-word Offset pointer for mask0 register on Port 0. For example, if P0_offset0=3 then the mask0 index register will start from Ethernet Packet type field (byte 11 after DA and SA MAC)
[7:4]	P0_offset1	0000	RW	Filter 1 Double word Offset pointer for mask1 register on Port 0
[11:8]	P0_offset2	0000	RW	Filter 2 Double word Offset pointer for mask2 register on Port 0
[14:12]	P0_en_mask [2:0]	000	RW	Enable mask byte for 3 different possible filter rules on Port 0
[15]	En_da_cmp	0	RW	Enable DA comparison as one of the wakeup condition for Port 0. (P0DAR0, P0DAR1)
[19:16]	P0_offset0	0000	RW	Filter 0 Double word Offset pointer for mask0 register on Port 1
[23:20]	P0_offset1	0000	RW	Filter 1 Double word Offset pointer for mask1 register on Port 1
[27:24]	P0_offset2	0000	RW	Filter 2 Double word Offset pointer for mask2 register on Port 1
[30:28]	P0_en_mask [2:0]	000	RW	Enable mask byte for 3 different possible filter rules on Port 1
[31]	En_da_cmp	0	RW	Enable DA comparison as one of the wakeup condition on Port 1. (P1DAR0, P1DAR1)

5.1.29 Port 0 Wakeup Frame Mask0 ~ 2 Register (P0WMR0, P0WMR1, P0WMR2)

Address 0x10C (P0WMR0)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask0	0x0000 0000	RW	Wake-up frame masked byte for mask0 on Port 0. Each bit is represent a byte. For example, if rgi_mask0=0xc0000000 then the CRC calculation will only calculate the first and 2nd byte after the P0_offset0 pointer location.

Address 0x110 (P0WMR1)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask1	0x0000 0000	RW	Wake-up frame masked byte for mask1 on Port 0

Address 0x114 (P0WMR2)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask2	0x0000 0000	RW	Wake-up frame masked byte for mask2 on Port 0

5.1.30 Port 0 Wakeup Frame CRC Mask 0 ~ 3 Register (P0WCR0, P0WCR1, P0WCR2)

Address 0x118 (P0WCR0)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc0	0x0000 0000	RW	Wake-up frame expected CRC value for mask0 register on Port 0. This is the pre-calculated mask byte data's expected CRC value for filter rule 0.

Address 0x11C (P0WCR1)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc1	0x0000 0000	RW	Wake-up frame expected CRC value for mask1 register on Port 0. This is the pre-calculated mask byte data's expected CRC value for filter rule 1.

Address 0x120 (P0WCR2)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc2	0x0000 0000	RW	Wake-up frame expected CRC value for mask2 register on Port 0. This is the pre-calculated mask byte data's expected CRC value for filter rule 2.

5.1.31 Port 1 Wakeup Frame Mask0 ~ 2 Register (P1WMR0, P1WMR1, P1WMR2)

Address 0x124 (P1WMR0)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask0	0x0000 0000	RW	Wake-up frame masked byte for mask0 on Port 1

Address 0x128 (P1WMR1)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask1	0x0000 0000	RW	Wake-up frame masked byte for mask1 on Port 1

Address 0x12C (P1WMR2)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_mask2	0x0000 0000	RW	Wake-up frame masked byte for mask2 on Port 1

5.1.32 Port 1 Wakeup Frame CRC Mask 0 ~ 3 Register (P1WCR0, P1WCR1, P1WCR2)

Address 0x130 (P1WCR0)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc0	0x0000 0000	RW	Wake-up frame expected CRC value for mask0 register on Port 1. This is the pre-calculated mask byte data's expected CRC value for filter rule 0.

Address 0x134 (P1WCR1)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc0	0x0000 0000	RW	Wake-up frame expected CRC value for mask1 register on Port 1. This is the pre-calculated mask byte data's expected CRC value for filter rule 1.

Address 0x138 (P1WCR2)

Bit	Name	Default Value	R/W	Function
[31:0]	rgi_crc2	0x0000 0000	RW	Wake-up frame expected CRC value for mask2 register on Port 1. This is the pre-calculated mask byte data's expected CRC value for filter rule 2.

5.1.33 Auto-Polling Control Register (ACR)

Address 0x140

Bit	Name	Default Value	R/W	Function
[4:0]	P0_phy_addr [4:0]	00000	RW	Port 0 Polling internal PHY ID register
[7:5]	Reserved	000	R	Reserved
[12:8]	P1_phy_addr [4:0]	00000	RW	Port 1 Polling internal PHY ID register
[15:13]	Reserved	000	R	Reserved
[20:16]	Reserved	00000	RW	Reserved
[21]	P0_poll_sel	0	RW	1: Auto-polling logic will Check BMCR register (PHY addr. 0x0) status to make decision on port 0 speed and duplex 0: Auto-polling logic will check ANAR register (PHY address 0x4) status to make decision on port 0 speed and duplex. (default)
[22]	P1_poll_sel	0	RW	1: Auto-polling logic will Check BMCR register (PHY addr. 0x0) status to make decision on port 1 speed and duplex 0: Auto-polling logic will check ANAR register (PHY address 0x4) status to make decision on port 1 speed and duplex. (default)
[23]	Reserved	0	RW	Reserved
[24]	P0_poll_en	0	RW	Enable Port 0 Auto-polling function If set to one then hardware will auto-polling internal PHY register setting and update Port 0 Mac Control Register (P0MCR) enable, speed, and duplex information.
[25]	P1_poll_en	0	RW	Enable Port 1 Auto-polling function. If set to one then hardware will auto-polling internal PHY register setting and update Port 1 Mac Control Register (P1MCR) enable, speed, and duplex information.

[26]	Reserved	0	RW	Reserved
[27]	Reserved	0	R	Reserved

[28]	P0_poll_fc	1	RW	Enable Port 0 Auto-polling Flow control function.
				Auto-polling PHY0's register and update flow control information on Port 0 setting.
				If PHY0 is in full duplex mode then
				1: port 0 MAC Flow control depend on PHY0 and PHY0's link partner PHY pause capability
				0: port 0 MAC disable Flow control
				If PHY0 is in half duplex mode then
				1: port 0 MAC enable Flow control
				0: port 0 MAC disable Flow control

[29]	P1_poll_fc	1	RW	Enable Port 1 Auto-polling Flow control function.
				Auto-polling PHY1's register and update flow control information on Port 1 setting.
				If PHY1 is in full duplex mode then
				1: port 1 MAC Flow control depend on PHY1 and PHY1's link partner PHY pause capability
				0: port 1 MAC disable Flow control
				If PHY1 is in half duplex mode then
				1: port 1 MAC enable Flow control
				0: port 1 MAC disable Flow control

[30]	Reserved	1	RW	Reserved
[31]	Reserved	0	R	Reserved

5.1.34 EEROM Control Register (ECR)

Address 0x144

Bit	Name	Default Value	R/W	Function
[21:0]	Eeprom_data [21:0]	0x000000	RW	EEROM data [21:0] When EEROM size=”01”: EEROM data [21:0] = {0000, SB, opcode [1:0], Addr [6:0], Data [7:0]} When EEROM size=”10 or 11”: EEROM data [21:0] = {00,SB, opcode [1:0], Addr [8:0], Data [7:0]} SB means StartBit, always set to one. Please also reference your EEPROM device datasheet.
[23:22]	Reserved	00	RW	Reserved
[24]	Eeprom_Check Busy	0	RW	Enable Hardware busy state checking function when write or erase EEPROM. With write or erase command, the EEPROM needs about 10ms to finish the command. If set this bit to 1, the EEPROM controller will check the EEPROM busy state until the EEPROM return to ready state. And the EEPROM controller then set Eeprom_valid to 1. If set this bit to 0 then the EEPROM controller will never check the EEPROM busy state, CPU should wait 10ms for next command.
[26:25]	Reserved	00	R	Reserved
[28:27]	Eeprom_size [1:0]	00	RW	EEROM size 00: reserve 01: 1K Bit (93c46) 10: 2K Bit (93c56) 11: 4K Bit (93c66) When CPU sends the read or write command to the EEPROM, CPU needs to set these two bits first. So the EEPROM controller knows the address space.
[29]	Reserved	0	RW	Reserved
[30]	Eeprom_valid	0	R	EEROM valid CPU needs polling this bit to confirm the EEPROM controller has finish the read, write or erase command. In the read command, Eeprom_valid =1 means Eeprom_data [7:0] is valid data. 1: finish the read/write command. 0: not yet finish the read/write command.
[31]	Eeprom_req	0	WC	EEROM request (write one clear) CPU sets this bit to one to pass the command to the EEPROM device. The command is include in the Eeprom_data [21:0] register. If CPU wants to send the read/write command to the EEPROM, CPU needs to read the Prom_mode register in CIRR first to make sure EEPROM addressable size. CPU also needs to check the BootFinish or the ChipInitDone bits to confirm that the Boot loader module complete the loading and stay in idle state.

5.1.35 Boot Loader Control Register (BLCR)

Address 0x148

Bit	Name	Default Value	R/W	Function
[15:0]	Reserved	0x0000	R	Reserved
[29:16]	Reserved	0x0000	R	Reserved
[30]	BootFinish	0	R	Boot loader operation done (read only) After power-on or hardware reset, the boot loader module will check the Prom_mode register value inside the CIRR, if the prom_mode[1:0] is not "00" , then the boot loader module will enable the EEPROM controller to read the EEPROM data and configure all the AX88782/AX88783 internal registers. When the boot loader module finishes loading the EEPROM data, then this bit will set to 1. 1: Boot loader module has finish loading and stay in idle state. 0: Boor loader module has not finish loading or prom_mode[1:0] is "00".
[31]	Boot_En	0	RW	Software start boot loader process when set to one. CPU can set this bit to 1 to force the boot loader module reload the EEPROM data and reconfigure all the AX88782/AX88783 internal registers after ChipInitDone is set to 1. When set this bit to 1, both the BootFinish and the ChipInitDone will clear to 0 , and then CPU needs polling the BootFinish or the ChipInitDone status to confirm the Boot loader module finish the process and stay in idle state.

5.1.36 IO Pad Pull-Up/Pull-Down Control Register (IOCR)

Address 0x14C

Bit	Name	Default Value	R/W	Function
[4:0]	Rgi_pupd	00000	RW	IO Pad Pull-up and Pull-down control register. [0]: Pull down the following IO pins when set to one CPU_DATA8 ~ CPU_DATA15 [1]: Pull down the following IO pins when set to one CPU_DATA16 ~ CPU_DATA31 [2]: Pull up the following IO pins when set to one CPU_DATA16 ~ CPU_DATA31 [3]: Pull down the following port 0 MII input pins when set to one. P0_MDIO, P0_MDC, MII0_RXD0 ~ MII0_RXD3, MII0_RX_DV, MII0_RX_COL, MII0_RX_CRS, MII0_RX_CLK, MII0_TX_CLK. [4]: Pull down the following port 1 MII input pins when set to one. P1_MDIO, P1_MDC, MII1_RXD0 ~ MII1_RXD3, MII1_RX_DV, MII1_RX_COL, MII1_RX_CRS, MII1_RX_CLK, MII1_TX_CLK.
[31:5]	Reserved	0x0000000	R	Reserved

5.1.37 Multicast IP for IGMP Snooping Entry 0 - 7 Register (IER0~IER7)

5.1.37.1 Multicast IP Entry 0 Register (IER0)

Address 0x150

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.2 Multicast IP Entry 1 Register (IER1)

Address 0x154

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.3 Multicast IP Entry 2 Register (IER2)

Address 0x158

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.4 Multicast IP Entry 3 Register (IER3)

Address 0x15C

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.5 Multicast IP Entry 4 Register (IER4)

Address 0x160

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.6 Multicast IP Entry 5 Register (IER5)

Address 0x164

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.7 Multicast IP Entry 6 Register (IER6)

Address 0x168

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.37.8 Multicast IP Entry 7 Register (IER7)

Address 0x16C

Bit	Name	Default Value	R/W	Function
[27:0]	MulticastIP	0x0000000	RW	Multicast IP [27:0] (IP [31:28] should be 1110 if multicast IP)
[30:28]	Multicast_port_map	000	RW	Multicast port map [30:28] {Port 2, Port 1, Port 0} Note: LGCR [14] IGMP mode will override this mapping if DIP with IGMP protocol received.
[31]	Valid	0	RW	Valid 1: Entry valid 0: Entry invalid

5.1.38 GPIO Control Register 1 (GPIOCR1)

Address 0x170

Bit	Name	Default Value	R/W	Function
[5:0]	GPIO_In	000000	RW	GPIO5~GPIO0 Input Data Register. Store the input data when GPIO output enable is not turned on.
[7:6]	Reserved	00	R	Reserved
[12:8]	GPI_In	00000	RW	GPI4~GPI0 Input Data Register. Store the input data value.
[15:13]	Reserved	000	R	Reserved
[21:16]	GPIO_En	000000	RW	GPIO5~GPIO0 Enable Register Enable GPIO function when set to one. 1: Enable 0: Disable
[22]	GPO_En	0	RW	GPO Enable Register. Enable GPO function when set to one. 1: Enable 0: Disable
[23]	Reserved	0	R	Reserved
[28:24]	GPI_En	00000	RW	GPI4~GPI0 Enable Register Enable GPI function when set to one. 1: Enable 0: Disable
[31:29]	Reserved	000	R	Reserved

5.1.39 GPIO Control Register 2 (GPIOCR2)

Address 0x174

Bit	Name	Default Value	R/W	Function
[5:0]	GPIO_Out	000000	RW	GPIO5~GPIO0 Output Data Register. The output data register will load to the GPIO pin when output enable is set to one.
[6]	GPO_Out	0	RW	GPO Output Data Register. GPO output date register.
[15:7]	Reserved	0x000	R	Reserved
[21:16]	GPIO_OE	000000	RW	GPIO5~GPIO0 Output Enable Register. If set to one then GPIO pin is used as output pin. Otherwise, the GPIO is a input pin. 1: Output Enable 0: Disable
[22]	GPO_OE	0	RW	GPO Output Enable Register. 1: Output Enable 0: Disable
[31:23]	Reserved	0x0000	R	Reserved

5.1.40 GPIO Control Register 3 (GPIOCR3)

Address 0x178

Bit	Name	Default Value	R/W	Function
[5:0]	GPIO_IntEn	000000	RW	GPIO5~GPIO0 Interrupt Enable Register. Enable GPIO interrupt function when set to one. 1: GPIO Interrupt Enable 0: Disable
[7:6]	Reserved	00	R	Reserved
[12:8]	GPI_IntEn	00000	RW	GPI4~GPI0 Interrupt Enable Register. Enable GPI interrupt function when set to one. 1: GPI interrupt enable 0: Disable
[15:13]	Reserved	000	R	Reserved
[21:16]	GPIO_Int_HL	000000	RW	GPIO5~GPIO0 Interrupt Polarity Select Register Active high if set to one and Active low if set to zero. 1: Active high interrupt 0: Active low interrupt (Default)
[23:22]	Reserved	00	R	Reserved
[28:24]	GPI_Int_HL	00000	RW	GPI4~GPI0 Interrupt Polarity Select Register Active high if set to one and Active low if set to zero. 1: Active high interrupt 0: Active low interrupt (Default)
[31:29]	Reserved	000	R	Reserved

5.1.41 GPIO Control Register 4 (GPIOCR4)

Address 0x17C

Bit	Name	Default Value	R/W	Function
[5:0]	GPIO_Int_Status	000000	RW	GPIO5~GPIO0 Interrupt Status Register Write one to clear interrupt status bit.
[7:6]	Reserved	00	R	Reserved
[12:8]	GPI_Int_Status	00000	RW	GPI4~GPI0 Interrupt Status Register Write one to clear interrupt status bit.
[15:13]	Reserved	000	R	Reserved
[21:16]	GPIO_Int_Mask	000000	RW	GPIO5~GPIO0 Interrupt Mask Register Mask Interrupt output when set to one. 1: Interrupt Mask Enable 0: Mask disable
[23:22]	Reserved	00	R	Reserved
[28:24]	GPI_Int_Mask	00000	RW	GPI4~GPI0 Interrupt Mask Register Mask Interrupt output when set to one. 1: Interrupt Mask Enable 0: Mask disable
[31:29]	Reserved	000	R	Reserved

5.1.42 Port 0 Slave MDC/MDIO Register 0 (P0SMR0)

Address 0x180

Bit	Name	Default Value	R/W	Function
[4:0]	Slavephyaddr	00001	RW	Port 0 slave MDC/MDIO PHY address
[29:5]	Reserved	0x0000000	R	Reserved
[30]	Reserved	0	RW	Always set 0 when write P0SMR0 register.
[31]	slave_en	0	RW	Port 0 Slave MDIO Enable bit

5.1.43 Port 0 Slave MDC/MDIO Register 1 (P0SMR1)

Address 0x184

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [15:0]	0x3100	RW	PHY register address 0x0 data registers
[31:16]	Slavedata [31:16]	0x7829	RW	PHY register address 0x1 data registers

5.1.44 Port 0 Slave MDC/MDIO Register 2 (P0SMR2)

Address 0x188

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [47:32]	0x 05E1	RW	PHY register address 0x4 data registers
[31:16]	Slavedata [63:48]	0x 0DE1	RW	PHY register address 0x5 data registers

5.1.45 Port 0 Slave MDC/MDIO Register 3 (P0SMR3)

Address 0x18C

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [79:64]	0x0000	RW	PHY register address 0x10 data registers
[31:16]	Slavedata_w	0x0000	WC	Configurable PHY register address 0x11 data registers

5.1.46 Port 1 Slave MDC/MDIO Register 0 (P1SMR0)

Address 0x190

Bit	Name	Default Value	R/W	Function
[4:0]	Slavephyaddr	00001	RW	Port 1slave MDC/MDIO PHY address
[29:5]	Reserved	0x0000 000	R	Reserved
[30]	Reserved	0	RW	Always set 0 when write P1SMR0 register.
[31]	slave_en	0	RW	Port 1 slave MDIO Enable bit

5.1.47 Port 1 Slave MDC/MDIO Register 1 (P1SMR1)

Address 0x194

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [15:0]	0x3100	RW	PHY Register address 0x0 data registers
[31:16]	Slavedata [31:16]	0x7829	RW	PHY Register address 0x1 data registers

5.1.48 Port 1 Slave MDC/MDIO Register 2 (P1SMR2)

Address 0x198

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [47:32]	0x 05E1	RW	PHY Register address 0x4 data registers
[31:16]	Slavedata [63:48]	0x 0DE1	RW	PHY Register address 0x5 data registers

5.1.49 Port 1 Slave MDC/MDIO Register 3 (P1SMR3)

Address 0x19C

Bit	Name	Default Value	R/W	Function
[15:0]	Slavedata [79:64]	0x0000	RW	PHY Register address 0x10 data registers
[31:16]	Slavedata_w	0x0000	WC	Configurable PHY Register address 0x11 data registers

5.1.50 Port 2 Multicast MAC Filters Register (P2MFR0 ~ P2MFR15)

Note: Only the following pre-assigned 16 multicast packets are able to forward to Port 2 if any of these entry is enabled. All multicast packets forward to port 2 not in this table will be dropped!! If none of the Enable bit is set then this table will be disabled!!

5.1.50.1 Port 2 Multicast MAC Filters Register 0 (P2MFR0)

Address 0x1B0

Bit	Name	Default Value	R/W	Function
[7:0]	DA0 [47:40]	0x00	RW	Multicast DA0 MAC Address [47:40]
[15:8]	DA0 [39:32]	0x00	RW	Multicast DA0 MAC Address [39:32]
[22:16]	DA0 [31:25]	0x00	RW	Multicast DA0 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA0 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA0 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA0 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA0 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA0 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA0 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA0 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.2 Port 2 Multicast MAC Filters Register 1 (P2MFR1)

Address 0x1B4

Bit	Name	Default Value	R/W	Function
[7:0]	DA1 [47:40]	0x00	RW	Multicast DA1 MAC Address [47:40]
[15:8]	DA1 [39:32]	0x00	RW	Multicast DA1 MAC Address [39:32]
[22:16]	DA1 [31:25]	0x00	RW	Multicast DA1 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA1 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA1 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA1 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA1 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA1 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA1 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA1 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.3 Port 2 Multicast MAC Filters Register 2 (P2MFR2)

Address 0x1B8

Bit	Name	Default Value	R/W	Function
[7:0]	DA2 [47:40]	0x00	RW	Multicast DA2 MAC Address [47:40]
[15:8]	DA2 [39:32]	0x00	RW	Multicast DA2 MAC Address [39:32]
[22:16]	DA2 [31:25]	0x00	RW	Multicast DA2 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA2 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA2 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA2 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA2 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA2 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA2 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA2 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.4 Port 2 Multicast MAC Filters Register 3 (P2MFR3)

Address 0x1BC

Bit	Name	Default Value	R/W	Function
[7:0]	DA3 [47:40]	0x00	RW	Multicast DA3 MAC Address [47:40]
[15:8]	DA3 [39:32]	0x00	RW	Multicast DA3 MAC Address [39:32]
[22:16]	DA3 [31:25]	0x00	RW	Multicast DA3 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA3 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA3 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA3 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA3 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA3 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA3 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA3 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.5 Port 2 Multicast MAC Filters Register 4 (P2MFR4)

Address 0x1C0

Bit	Name	Default Value	R/W	Function
[7:0]	DA4 [47:40]	0x00	RW	Multicast DA4 MAC Address [47:40]
[15:8]	DA4 [39:32]	0x00	RW	Multicast DA4 MAC Address [39:32]
[22:16]	DA4 [31:25]	0x00	RW	Multicast DA4 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA4 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA4 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA4 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA4 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA4 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA4 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA4 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.6 Port 2 Multicast MAC Filters Register 5 (P2MFR5)

Address 0x1C4

Bit	Name	Default Value	R/W	Function
[7:0]	DA5 [47:40]	0x00	RW	Multicast DA5 MAC Address [47:40]
[15:8]	DA5 [39:32]	0x00	RW	Multicast DA5 MAC Address [39:32]
[22:16]	DA5 [31:25]	0x00	RW	Multicast DA5 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA5 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA5 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA5 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA5 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA5 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA5 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA5 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.7 Port 2 Multicast MAC Filters Register 6 (P2MFR6)

Address 0x1C8

Bit	Name	Default Value	R/W	Function
[7:0]	DA6 [47:40]	0x00	RW	Multicast DA6 MAC Address [47:40]
[15:8]	DA6 [39:32]	0x00	RW	Multicast DA6 MAC Address [39:32]
[22:16]	DA6 [31:25]	0x00	RW	Multicast DA6 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA6 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA6 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA6 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA6 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA6 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA6 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA6 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.8 Port 2 Multicast MAC Filters Register 7 (P2MFR7)

Address 0x1CC

Bit	Name	Default Value	R/W	Function
[7:0]	DA7 [47:40]	0x00	RW	Multicast DA7 MAC Address [47:40]
[15:8]	DA7 [39:32]	0x00	RW	Multicast DA7 MAC Address [39:32]
[22:16]	DA7 [31:25]	0x00	RW	Multicast DA7 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA7 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA7 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA7 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA7 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA7 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA7 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA7 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.9 Port 2 Multicast MAC Filters Register 8 (P2MFR8)

Address 0x1D0

Bit	Name	Default Value	R/W	Function
[7:0]	DA8 [47:40]	0x00	RW	Multicast DA8 MAC Address [47:40]
[15:8]	DA8 [39:32]	0x00	RW	Multicast DA8 MAC Address [39:32]
[22:16]	DA8 [31:25]	0x00	RW	Multicast DA8 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA8 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA8 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA8 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA8 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA8 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA8 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA8 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.10 Port 2 Multicast MAC Filters Register 9 (P2MFR9)

Address 0x1D4

Bit	Name	Default Value	R/W	Function
[7:0]	DA9 [47:40]	0x00	RW	Multicast DA9 MAC Address [47:40]
[15:8]	DA9 [39:32]	0x00	RW	Multicast DA9 MAC Address [39:32]
[22:16]	DA9 [31:25]	0x00	RW	Multicast DA9 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA9 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA9 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA9 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA9 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA9 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA9 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA9 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.11 Port 2 Multicast MAC Filters Register 10 (P2MFR10)

Address 0x1D8

Bit	Name	Default Value	R/W	Function
[7:0]	DA10 [47:40]	0x00	RW	Multicast DA10 MAC Address [47:40]
[15:8]	DA10 [39:32]	0x00	RW	Multicast DA10 MAC Address [39:32]
[22:16]	DA10 [31:25]	0x00	RW	Multicast DA10 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA10 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA10 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA10 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA10 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA10 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA10 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA10 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.12 Port 2 Multicast MAC Filters Register 11 (P2MFR11)

Address 0x1DC

Bit	Name	Default Value	R/W	Function
[7:0]	DA11 [47:40]	0x00	RW	Multicast DA11 MAC Address [47:40]
[15:8]	DA11 [39:32]	0x00	RW	Multicast DA11 MAC Address [39:32]
[22:16]	DA11 [31:25]	0x00	RW	Multicast DA11 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA11 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA11 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA11 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA11 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA11 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA11 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA11 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.13 Port 2 Multicast MAC Filters Register 12 (P2MFR12)

Address 0x1E0

Bit	Name	Default Value	R/W	Function
[7:0]	DA12 [47:40]	0x00	RW	Multicast DA12 MAC Address [47:40]
[15:8]	DA12 [39:32]	0x00	RW	Multicast DA12 MAC Address [39:32]
[22:16]	DA12 [31:25]	0x00	RW	Multicast DA12 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA12 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA12 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA12 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA12 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA12 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA12 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA12 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.14 Port 2 Multicast MAC Filters Register 13 (P2MFR13)

Address 0x1E4

Bit	Name	Default Value	R/W	Function
[7:0]	DA13 [47:40]	0x00	RW	Multicast DA13 MAC Address [47:40]
[15:8]	DA13 [39:32]	0x00	RW	Multicast DA13 MAC Address [39:32]
[22:16]	DA13 [31:25]	0x00	RW	Multicast DA13 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA13 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA13 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA13 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA13 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA13 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA13 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA13 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.15 Port 2 Multicast MAC Filters Register 14 (P2MFR14)

Address 0x1E8

Bit	Name	Default Value	R/W	Function
[7:0]	DA14 [47:40]	0x00	RW	Multicast DA14 MAC Address [47:40]
[15:8]	DA14 [39:32]	0x00	RW	Multicast DA14 MAC Address [39:32]
[22:16]	DA14 [31:25]	0x00	RW	Multicast DA14 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA14 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA14 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA14 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA14 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA14 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA14 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA14 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.50.16 Port 2 Multicast MAC Filters Register 15 (P2MFR15)

Address 0x1EC

Bit	Name	Default Value	R/W	Function
[7:0]	DA15 [47:40]	0x00	RW	Multicast DA15 MAC Address [47:40]
[15:8]	DA15 [39:32]	0x00	RW	Multicast DA15 MAC Address [39:32]
[22:16]	DA15 [31:25]	0x00	RW	Multicast DA15 MAC Address [31:25]
[23]	SourcePort0	0	RW	This multicast DA15 MAC packet is from Port 0.
[24]	SourcePort1	0	RW	This multicast DA15 MAC packet is from Port 1. {SourcePort1, SourcePort0} 01: Limit this DA15 MAC multicast packet must from port 0 otherwise will be dropped. 10: Limit this DA15 MAC multicast packet must from port 1 otherwise will be dropped. 11: This DA15 MAC multicast packet can from port 0 or port 1. 00: Always drop this DA15 MAC multicast packet
[25]	Enable	0	RW	Entry is valid. 1: Enable Port 2 Multicast DA15 MAC Filter check on this entry 0: Disable
[31:26]	Reserved	0x00	R	Reserved

5.1.51 Interface Configuration Register (ICR)

Address 0x1F0

Bit	Name	Default Value	R/W	Function
[1:0]	ClkGen_EN [1:0]	00	RW	Enable per port RMII to MII clock generator, active high [0]: Enable RMII clock generator on Port 0 [1]: Enable RMII clock generator on Port 1 1: Enable if RMII interface is also turn on 0: Disable
[2]	Reserved	0	RW	Always assign zero
[3]	Reserved	0	R	Reserved
[5:4]	RMII_EN [1:0]	00	RW	Per port RMII Interface Enable, active high [0]: Enable RMII interface on Port 0 [1]: Enable RMII interface on Port 1 1: Enable RMII IO MUX selection logic 0: Disable
[6]	Reserved	0	RW	Always assign zero
[7]	Reserved	0	R	Reserved
[9:8]	RevRMII_Option [1:0]	00	RW	Enable RevRMII ending option, active high. If the ending option is set to one then the RMII interface logic will check and make sure at the end of each frame append a pulse (high and low) on valid signal to indicate an EOF symbol. [0]: Enable RevRMII ending option on Port 0 [1]: Enable RevRMII ending option on Port 1 1: Append a EOF pattern at the end of transaction 0: Normal (Default)
[10]	Reserved	0	RW	Always assign zero
[11]	Reserved	0	R	Reserved
[13:12]	CLK50_EN [1:0]	00	RW	Output 50 MHz clock output for Reverse RMII for external chip reference clock. [0]: Output 50MHz clock on pin MII0_TX_CLK [1]: Output 50MHz clock on pin MII1_TX_CLK 1: 50MHz clock output enable 0: Disable
[14]	Reserved	0	RW	Always assign zero
[15]	Reserved	0	R	Reserved
[17:16]	MII_EN [1:0]	00	RW	Enable IO Pad select MUX for MII Interface signals, active high [0]: Enable MII Port 0 [1]: Enable MII Port 1 1: Enable MII IO MUX selection logic 0: Disable
[21:18]	Reserved	0000	RW	Always assign zero
[23:22]	Reserved	00	R	Reserved
[25:24]	RevMII_EN [1:0]	00	RW	Enable IO Pad select output MUX for TX clock and RX clock as output signal, active high. [0]: Enable RevMII Port 0 [1]: Enable RevMII Port 1 1: Enable RevMII interface logic 0: Disable
[26]	Reserved	0	RW	Always assign zero
[27]	Reserved	0	R	Reserved
[29:28]	MDC_EN	000	RW	Enable IO Pad select MUX for MDIO Interface, active high [0]: Enable MDIO interface to Port 0 MDIO pins [1]: Enable MDIO interface to Port 1 MDIO pins 1: Enable MDIO interface logic

				0: Disable
[30]	Reserved	0	RW	Always set to 0
[31]	Reserved	0	R	Reserved

5.1.52 Sleep Mode Exit Register (SMER)

Address 0x1F4

Bit	Name	Default Value	R/W	Function
[31:0]	Sleep_mode_exit	0x0000 0000	WC	Any write command to this address will cause the chip exit the sleep mode and back to normal mode operation.

5.1.53 Endian Configuration Register (ECR)

Address 0x1F8

Bit	Name	Default Value	R/W	Function
[0]	Endian_cfg	0	RW	The Endian Configuration Register 0: Little Endian(default) 1: Big Endian
[31:1]	Reserved	0x0000 0000	RW	Reserved

5.1.54 General Purpose Timer Configuration Register (GTCR)

The General Purpose Timer can be used for software to count a precise time.

Address 0x1FC

Bit	Name	Default Value	R/W	Function
[29:0]	Timer [29:0]	0x0000 0000	RW	The General Purpose Timer counter register (10ns per unit).
[31:30]	Timer_mode [1:0]	00	RW	Internal General Purpose Timer mode select 00: Disable General Purpose Timer function 01: Active the timer-up interrupts status (ISMR [12]) when the timer is done, then the timer will auto re-start the increment process. 10: Active the timer-up interrupts status (ISMR [12]) when the timer is done, then the timer will re-start only after the software clear the timer-up interrupt status. 11: Reserved

5.1.55 Port 0 MAC Configuration Register (P0MCR)

Address 0x200

Bit	Name	Default Value	R/W	Function
[0]	MAC_Enable	0	RW	Enable Port 0 MAC function When Port 0 Auto-Polling function is disabled (ACR [24] = 0), CPU is able to read or write this register and enable or disable MAC function. When Port 0 Auto-Polling function is enabled (ACR [24] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know if Port 0 MAC is being enabled or not. 1: Enable Port 0 MAC function 0: Disable Port 0 MAC function
[2:1]	Reserved	00	R	Reserved
[3]	Speed100/10	0	RW	Set Port 0 MAC Speed to 100MBps or 10MBps. When Port 0 Auto-Polling function is disabled (ACR [24] = 0), CPU is able to read or write this register and set MAC working speed. When Port 0 Auto-Polling function is enabled (ACR [24] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 0 MAC's working speed. 1: Set Port 0 MAC speed to 100MBps 0: Set Port 0 MAC speed to 10MBps
[4]	Full_Duplex	0	RW	Set Port 0 Full or Half Duplex mode When Port 0 Auto-Polling function is disabled (ACR [24] = 0), CPU is able to read or write this register and set Port 0 MAC duplex mode. When Port 0 Auto-Polling function is enabled (ACR [24] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 0 MAC's duplex mode. 1: Set Port 0 MAC working at Full Duplex mode 0: Set Port 0 MAC working at Half Duplex mode
[6:5]	Reserved	00	R	Reserved
[7]	FlowCtrl_ON	0	RW	Flow Control Enable when set to one When Port 0 Auto-Polling function is disabled (ACR [24] = 0), CPU is able to read or write this register and set Port 0 MAC flow control mode. When Port 0 Auto-Polling function is enabled (ACR [24] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 0 MAC's flow control mode. 1: Enable Port 0 MAC Flow Control function 0: Disable Port 0 MAC Flow Control function
[8]	CRC_Check	1	RW	Enable Port 0 MAC CRC check function when set to one 1: Enable Port MAC 0 CRC check function 0: Disable Port 0 MAC CRC check function
[9]	Reserved	0	RW	Reserved
[10]	AcceptAll	0	RW	1: Accept all packet even illegal (oversize, undersize, crc error..). 0: Only accept legal packet. NOTE: The undersize packet will add padding within the RX MAC.
[11]	1XsecurityON	0	RW	Enable Port 0 802.1X function when set to one 1: Enable Port 0 802.1X l function Note: LGCR [16] 1X_En also need to set to 1 0: Disable Port 0 802.1X function
[12]	RXStop	0	RW	Drop the RX MAC incoming packets when this bit is set to one 1: Drop all the receiving packets 0: Disable RXStop function.
[13]	TXStop	0	RW	Stop TX from Transmit the packets when this bit is set to one. 1: Stop transmit packets 0: Disbale TXStop function

[14]	Reserved	0	R	Reserved
[15]	Uplink_Port	0	RW	Valid only when 802.1QinQ double tagging function (LGCR [15]) is enabled. 1: Uplink_Port 0: Access_Port.
[16]	EnRXRate	0	RW	Port 0 Ingress Rate Limit Function 1: Enable Port 0 RX Rate limit function 0: Disable Port 0 RX Rate limit function
[17]	EnTXRate	0	RW	Port 0 Egress Rate Limit Function 1: Enable Port 0 TX Rate limit function 0: Disable Port 0 TX Rate limit function
[18]	DAMatch_Enable	0	RW	If this bit is set to one, any receiving packet who's DA MAC is not match with the pre-defined Register address 0x230, 0x234 MAC address, the packet will be dropped except Multicast and Broadcast packets. 1: Port 0 Only pass multicast, broadcast packet and unicast with DA match Port 0's DA MAC setting in registers P0DAR0 and P0DAR1. 0: Disable DAMatch_Enable function
[19]	Reserved	0	RW	Reserved
[31:20]	Reserved	0x000	R	Reserved

5.1.56 Port 0 802.1p QoS Mapping Table Register (P0QMTR)

Address 0x204

Bit	Name	Default Value	R/W	Function
[1:0]	RX_QoS0	00	RW	802.1p QoS Mapping Table: This table converts eight QoS value to one of the internal four queues. The AX88782/AX88783 only support 0,1, 2 and 3. Internal QoS value when RX packet's QoS = 0
[3:2]	RX_QoS1	00	RW	Internal QoS value when RX packet's QoS = 1
[5:4]	RX_QoS2	01	RW	Internal QoS value when RX packet's QoS = 2
[7:6]	RX_QoS3	01	RW	Internal QoS value when RX packet's QoS = 3
[9:8]	RX_QoS4	10	RW	Internal QoS value when RX packet's QoS = 4
[11:10]	RX_QoS5	10	RW	Internal QoS value when RX packet's QoS = 5
[13:12]	RX_QoS6	11	RW	Internal QoS value when RX packet's QoS = 6
[15:14]	RX_QoS7	11	RW	Internal QoS value when RX packet's QoS = 7
[18:16]	Reserved	000	RW	Reserved
[19]	Reserved	0	R	Reserved
[26:20]	Reserved	0x00	RW	Reserved
[27]	Reserved	0	R	Reserved
[31:28]	Reserved	0000	RW	Reserved

5.1.57 Port 0 802.1Q Configuration for UnTag Frame Register (P0QCR)

Address 0x208

Bit	Name	Default Value	R/W	Function
[11:0]	PVID	0x001	RW	VLAN ID value (1 ~ 4095, default 1)
[12]	CF	0	RW	CF Flag
[15:13]	QoS	000	RW	QoS value
[31:16]	Reserved	0x0000	R	Reserved

* This Tag information will be inserted when un-tag frame is received.

5.1.58 Port 0 RX per Queue Rate Limit Control Register 0 (P0RQR0)

Address 0x20C

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q0_rate	0xFFF	RW	Port 0 RX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q1_rate	0xFFF	RW	Port 0 RX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.59 Port 0 RX per Queue Rate Limit Control Register 1 (P0RQR1)

Address 0x210

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q2_rate	0xFFF	RW	Port 0 RX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q3_rate	0xFFF	RW	Port 0 RX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.60 Port 0 TX per Queue Rate Limit Control Register 0 (P0TQR0)

Address 0x214

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q0_rate	0xFFF	RW	Port 0 TX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q1_rate	0xFFF	RW	Port 0 TX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.61 Port 0 TX per Queue Rate Limit Control Register 1 (P0TQR1)

Address 0x218

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q2_rate	0xFFF	RW	Port 0 TX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q3_rate	0xFFF	RW	Port 0 TX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.62 Port 0 Rate Limit Control Register (P0RLR)

Address 0x21C

Bit	Name	Default Value	R/W	Function
[11:0]	ingress_rate	0xFFF	RW	Port 0 RX rate limit (4K bytes per unit) For example, if ingress_rate=16 means port 0 can receive 64K byte within P0RLTR Cycle_time window (one second). 0xFFF means disable RX per port rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	egress_rate	0xFFF	RW	Port 0 TX per port rate limit (4K bytes per unit) 0xFFF means disable TX per port rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.63 Port 0 Rate Limit Timer Register (P0RLTR)

Address 0x220

Bit	Name	Default Value	R/W	Function
[26:0]	Cycle_time	0x5F5E100	RW	Per port timer for rate limit calculation. (Default 1 sec.) Second = 10 E 8 ns = 0x5F5E100 x 10ns (100MHz core clock cycle time)
[31:27]	Reserved	00000	R	Reserved

5.1.64 Port 0 Flow Control High/Low Watermark Register (P0FCR)

Address 0x224

Bit	Name	Default Value	R/W	Function
[7:0]	FCHW	0x28	RW	Flow Control High-water mark [7:0]: RX accumulate page count high water level, once internal RX receiving page counter higher than this threshold and Flow control is enabled, then TX MAC will send Pause ON Frame out to informal remote PHY stop transmit packets.
[15:8]	FCLW	0x14	RW	Flow Control Low-water mark [7:0]: When Flow control is enabled and pause is ON, RX receiving page counter if lower than this low water mark value then TX MAC will send pause OFF frame to inform remote PHY back to normal state and re-start transmit packets.
[31:16]	Reserved	0x0000	R	Reserved

5.1.65 Port 0 Queue Weighting Configuration Register (P0QWR)

Address 0x228

Bit	Name	Default Value	R/W	Function
[3:0]	Q0_Weight	1111	RW	Q0 weighting control for BMU scheduler module usage. The default value is 1111 means disable weighting control. Otherwise buffer management unit will schedule TX output packet based on Q0/Q1/Q2/Q3 weighting distribution.
[7:4]	Q1_Weight	1111	RW	Q1 weighting control for BMU scheduler module usage
[11:8]	Q2_Weight	1111	RW	Q2 weighting control for BMU scheduler module usage
[15:12]	Q3_Weight	1111	RW	Q3 weighting control for BMU scheduler module usage For example if Q0_Weight=1, Q1_Weight=2, Q2_Weight=4 and Q3_Weight=8 then the output packets will have this ratio 8:4:2:1 if all the packets are the same size. The weighting here will based on the page count. There are 128 bytes in a page.
[31:16]	Reserved	0x0000	R	Reserved

5.1.66 Port 0 RX Bad Check-sum Drop Counter Register (P0RDCR)

Address 0x22C

Bit	Name	Default Value	R/W	Function
[31:0]	RX_drop_cntr	0x00000000	RW	Port 0 RX drop packet counter. When TOCR [13:8] any of the Drop CRC protocol is enabled, then Port 0 will accumulate the drop packet count due to the bad CRC checksum packet. Write 1 to TOCR [15] Clr_rxdrop_cntr to clear this counter.

5.1.67 Port 0 DA MAC Address Register (P0DAR0, P0DAR1)

Address 0x230 (P0DAR0)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC0 [47:40]	0x00	RW	Default DA MAC0 address for Port 0 only valid when DAMatchEn is set to one.(P0MCR [18]) DA MAC0 address [47:40]
[15:8]	DAMAC0 [39:32]	0x00	RW	DA MAC0 address [39:32]
[23:16]	DAMAC0 [31:24]	0x00	RW	DA MAC0 address [31:24]
[31:24]	DAMAC0 [23:16]	0x00	RW	DA MAC0 address [23:16]

Address 0x234 (P0DAR1)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC0 [15:8]	0x00	RW	Default DA MAC0 address for Port 0 only valid when DAMatchEn is set to one. (P0MCR [18]) DA MAC0 address [15:8]
[15:8]	DAMAC0 [7:0]	0x00	RW	DA MAC0 address [7:0]
[31:16]	Reserved	0x0000	R	Reserved

5.1.68 Port 1 MAC Configuration Register (P1MCR)

Address 0x240

Bit	Name	Default Value	R/W	Function
[0]	MAC_Enable	0	RW	Enable Port 1 MAC function When Port 1 Auto-Polling function is disabled (ACR [25] = 0), CPU is able to read or write this register and enable or disable MAC function. When Port 1 Auto-Polling function is enabled (ACR [25] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know if Port 1 MAC is being enabled or not. 1: Enable Port 1 MAC function 0: Disable Port 1 MAC function
[2:1]	Reserved	00	R	Reserved
[3]	Speed100/10	0	RW	Set Port 1 MAC Speed to 100MBps or 10MBps. When Port 1 Auto-Polling function is disabled (ACR [25] = 0), CPU is able to read or write this register and set MAC working speed. When Port 1 Auto-Polling function is enabled (ACR [25] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 1 MAC's working speed. 1: Set Port 1 MAC speed to 100MBps 0: Set Port 1 MAC speed to 10MBps
[4]	Full_Duplex	0	RW	Set Port 1 Full or Half Duplex mode When Port 1 Auto-Polling function is disabled (ACR [25] = 0), CPU is able to read or write this register and set Port 1 MAC duplex mode. When Port 1 Auto-Polling function is enabled (ACR [25] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 0 MAC's duplex mode. 1: Set Port 1 MAC working at Full Duplex mode 0: Set Port 1 MAC working at Half Duplex mode
[6:5]	Reserved	00	R	Reserved
[7]	FlowCtrl_ON	0	RW	Flow Control Enable when set to one When Port 1 Auto-Polling function is disabled (ACR [25] = 0), CPU is able to read or write this register and set Port 0 MAC flow control mode. When Port 1 Auto-Polling function is enabled (ACR [25] =1), The Auto-Polling logic take control of this register and CPU can only read this bit to know Port 1 MAC's flow control mode. 1: Enable Port 1 MAC Flow Control function 0: Disable Port 1 MAC Flow Control function
[8]	CRC_Check	1	RW	Enable Port 1 MAC CRC check function when set to one 1: Enable Port 1 MAC CRC check function 0: Disable Port 1 MAC CRC check function
[9]	Reserved	0	RW	Reserved
[10]	AcceptAll	0	RW	1: Accept all packet even illegal (oversize, undersize, crc error..). 0: Only accept legal packet. NOTE: The undersize packet will add padding within the RX MAC.
[11]	1XsecurityON	0	RW	Enable Port 1 802.1X function when set to one 1: Enable Port 1 802.1X l function Note: LGCR [16] 1X_En also need to set to 1 0: Disable Port 1 802.1X function
[12]	RXStop	0	RW	Drop the RX MAC incoming packets when this bit is set to one 1: Drop all the receiving packets 0: Disable RXStop function.
[13]	TXStop	0	RW	Stop TX from Transmit the packets when this bit is set to one. 1: Stop transmit packets 0: Disbale TXStop function

[14]	Reserved	0	R	Reserved
[15]	Uplink_Port	0	RW	Valid only when 802.1QinQ double tagging function (LGCR [15]) is enabled. 1: Uplink_Port 0: Access_Port.
[16]	EnRXRate	0	RW	Port 1 Ingress Rate Limit Function 1: Enable Port 1 RX Rate limit function 0: Disable Port 1 RX Rate limit function
[17]	EnTXRate	0	RW	Port 1 Egress Rate Limit Function 1: Enable Port 1 TX Rate limit function 0: Disable Port 1 TX Rate limit function
[18]	DAMatch_Enable	0	RW	If this bit is set to one, any receiving packet who's DA MAC is not match with the pre-defined Register address 0x230, 0x234 MAC address, the packet will be dropped except Multicast and Broadcast packets. 1: Port 1 Only pass multi-cast, broadcast packet and unicast with DA match Port 1's DA MAC setting in registers P1DAR0 and P1DAR1. 0: Disable DAMatch_Enable function
[19]	Reserved	0	RW	Reserved
[31:20]	Reserved	0x000	R	Reserved

5.1.69 Port 1 802.1p QoS Mapping Table Register (P1QMTR)

Address 0x244

Bit	Name	Default Value	R/W	Function
[1:0]	RX_QoS0	00	RW	802.1p QoS Mapping Table: This table converts eight QoS value to one of the internal four queues. The AX88782/AX88783 only support 0,1, 2 and 3. Internal QoS value when RX packet's QoS = 0
[3:2]	RX_QoS1	00	RW	Internal QoS value when RX packet's QoS = 1
[5:4]	RX_QoS2	01	RW	Internal QoS value when RX packet's QoS = 2
[7:6]	RX_QoS3	01	RW	Internal QoS value when RX packet's QoS = 3
[9:8]	RX_QoS4	10	RW	Internal QoS value when RX packet's QoS = 4
[11:10]	RX_QoS5	10	RW	Internal QoS value when RX packet's QoS = 5
[13:12]	RX_QoS6	11	RW	Internal QoS value when RX packet's QoS = 6
[15:14]	RX_QoS7	11	RW	Internal QoS value when RX packet's QoS = 7
[18:16]	Reserved	000	RW	Reserved
[19]	Reserved	0	R	Reserved
[26:20]	Reserved	0x00	RW	Reserved
[27]	Reserved	0	R	Reserved
[31:28]	Reserved	0000	RW	Reserved

5.1.70 Port 1 802.1Q Configuration for UnTag Frame Register (P1QCR)

Address 0x248

Bit	Name	Default Value	R/W	Function
[11:0]	PVID	0x001	RW	VLAN ID value (1 ~ 4095, default 1)
[12]	CF	0	RW	CF Flag
[15:13]	QoS	000	RW	QoS value
[31:16]	Reserved	0x0000	R	Reserved

* This Tag information will be inserted when untag frame is received.

5.1.71 Port 1 RX per Queue Rate Limit Control Register 0 (P1RQR0)

Address 0x24C

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q0_rate	0xFFF	RW	Port 1 RX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q1_rate	0xFFF	RW	Port 1 RX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.72 Port 1 RX per Queue Rate Limit Control Register 1 (P1RQR1)

Address 0x250

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q2_rate	0xFFF	RW	Port 1 RX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q3_rate	0xFFF	RW	Port 1 RX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.73 Port 1 TX per Queue Rate Limit Control Register 0 (P1TQR0)

Address 0x254

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q0_rate	0xFFF	RW	Port 1 TX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q1_rate	0xFFF	RW	Port 1 TX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.74 Port 1 TX per Queue Rate Limit Control Register 1 (P1TQR1)

Address 0x258

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q2_rate	0xFFF	RW	Port 1 TX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q3_rate	0xFFF	RW	Port 1 TX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.75 Port 1 Rate Limit Control Register (P1RLR)

Address 0x25C

Bit	Name	Default Value	R/W	Function
[11:0]	ingress_rate	0xFFF	RW	Port 1 RX rate limit (4K bytes per unit) For example, if ingress_rate=16 means port 0 can receive 64K byte within P0RLTR Cycle_time window (one second). 0xFFF means disable RX per port rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	egress_rate	0xFFF	RW	Port 1 TX per port rate limit (4K bytes per unit) 0xFFF means disable TX per port rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.76 Port 1 Rate Limit Timer Register (P1RLTR)

Address 0x260

Bit	Name	Default Value	R/W	Function
[26:0]	Cycle_time	0x5F5E100	RW	Per port timer for rate limit calculation. (Default 1 sec.) 1 Second = 10 ^ 8 ns = 0x5F5E100 x 10ns (100MHz clock cycle time)
[31:27]	Reserved	00000	R	Reserved

5.1.77 Port 1 Flow Control High/Low Watermark Register (P1FCR)

Address 0x264

Bit	Name	Default Value	R/W	Function
[7:0]	FCHW	0x28	RW	Flow Control High-water mark [7:0]: RX accumulate page count high water level, once internal RX receiving page counter higher than this threshold and Flow control is enabled, then TX MAC will send Pause ON Frame out to informal remote PHY stop sending packets.
[15:8]	FCLW	0x14	RW	Flow Control Low-water mark [7:0]: When Flow control is enabled and pause is ON, RX receiving page counter if lower than this low water mark value then TX MAC will send pause OFF frame to inform remote PHY back to normal state.
[31:16]	Reserved	0x0000	R	Reserved

5.1.78 Port 1 Queue Weighting Configuration Register (P1QWR)

Address 0x268

Bit	Name	Default Value	R/W	Function
[3:0]	Q0_Weight	1111	RW	Q0 weighting control for BMU scheduler module usage. The default value is 1111 means disable weighting control. Otherwise buffer management unit will schedule TX output packet based on Q0/Q1/Q2/Q3 weighting distribution.
[7:4]	Q1_Weight	1111	RW	Q1 weighting control for BMU scheduler module usage
[11:8]	Q2_Weight	1111	RW	Q2 weighting control for BMU scheduler module usage
[15:12]	Q3_Weight	1111	RW	Q3 weighting control for BMU scheduler module usage For example if Q0_Weight=1, Q1_Weight=2, Q2_Weight=4 and Q3_Weight=8 then the output packets will have this ratio 8:4:2:1 if all the packets are the same size. The weighting here will based on the page count. There are 128 bytes in a page.
[31:16]	Reserved	0x0000	R	Reserved

5.1.79 Port 1 RX Bad Checksum Drop Counter Register (P1RDCR)

Address 0x26C

Bit	Name	Default Value	R/W	Function
[31:0]	RX_drop_cntr	0x00000000	RW	Port 1 RX drop packet counter. When TOCR [13:8] any of the Drop CRC protocol is enabled, then Port 1 will accumulate the drop packet count due to bad CRC checksum. Write 1 to TOCR [15] Clr_rxdrop_cntr to clear this counter.

5.1.80 Port 1 DA MAC Address Register (P1DAR0, P1DAR1)

Address 0x270 (P1DAR0)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC1 [47:40]	0x00	RW	Default DA MAC1 address for Port 1 only valid when DAMatchEn is set to one.(P1MCR [18]) DA MAC1 address [47:40]
[15:8]	DAMAC1 [39:32]	0x00	RW	DA MAC1 address [39:32]
[23:16]	DAMAC1 [31:24]	0x00	RW	DA MAC1 address [31:24]
[31:24]	DAMAC1 [23:16]	0x00	RW	DA MAC1 address [23:16]

Address 0x274 (P1DAR1)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC1 [15:8]	0x00	RW	Default DA MAC1 address for Port 1 only valid when DAMatchEn is set to one. (P1MCR [18]) DA MAC1 address [15:8]
[15:8]	DAMAC1 [7:0]	0x00	RW	DA MAC1 address [7:0]
[31:16]	Reserved	0x0000	R	Reserved

5.1.81 Port 2 MAC Configuration Register (P2MCR)

Address 0x280

Bit	Name	Default Value	R/W	Function
[0]	Reserved	0	RW	Reserved
[2:1]	Reserved	00	R	Reserved
[3]	Reserved	0	RW	Reserved
[4]	Reserved	0	RW	Reserved
[6:5]	Reserved	00	R	Reserved
[7]	Reserved	0	RW	Reserved
[8]	Reserved	1	RW	Reserved
[9]	Reserved	0	RW	Reserved
[10]	Reserved	0	RW	Reserved
[11]	1XsecurityON	0	RW	Enable Port 2 802.1X function when set to one 1: Enable Port 2 802.1X l function Note: LGCR [16] 1X_En also need to set to 1 0: Disable Port 2 802.1X function
[12]	RXStop	0	RW	Drop the RX MAC incoming packets when this bit is set to one 1: Drop all the receiving packets 0: Disable RXStop function.
[13]	TXStop	0	RW	Stop TX from Transmit the packets when this bit is set to one. 1: Stop transmit packets 0: Disbale TXStop function
[14]	Reserved	0	R	Reserved
[15]	Uplink_Port	0	RW	Valid only when 802.1QinQ double tagging function (LGCR [15]) is enabled. 1: Uplink_Port 0: Access_Port.
[16]	EnRXRate	0	RW	Port 2 Ingress Rate Limit Function 1: Enable Port 2 RX Rate limit function 0: Disable Port 2 RX Rate limit function
[17]	EnTXRate	0	RW	Port 2 Egress Rate Limit Function 1: Enable Port 2 TX Rate limit function 0: Disable Port 2 TX Rate limit function
[18]	DAMatch_Enable	0	RW	If this bit is set to one, any receiving packet who's DA MAC is not match with the pre-defined Register address 0x230, 0x234 MAC address, the packet will be dropped except Multicast and Broadcast packets. 1: Port 2 Only pass multicast, broadcast packet and unicast with DA match Port 2's DA MAC setting in registers P2DAR0 and P2DAR1. 0: Disable DAMatch_Enable function
[19]	Reserved	0	RW	Reserved
[31:20]	Reserved	0x000	R	Reserved

5.1.82 Port 2 802.1p QoS Mapping Table Register (P2QMTR)

Address 0x284

Bit	Name	Default Value	R/W	Function
[1:0]	RX_QoS0	00	RW	802.1p QoS Mapping Table: This table converts eight QoS value to one of the internal four queues. The AX88782/AX88783 only support 0,1, 2 and 3. Internal QoS value when RX packet's QoS = 0
[3:2]	RX_QoS1	00	RW	Internal QoS value when RX packet's QoS = 1
[5:4]	RX_QoS2	01	RW	Internal QoS value when RX packet's QoS = 2
[7:6]	RX_QoS3	01	RW	Internal QoS value when RX packet's QoS = 3
[9:8]	RX_QoS4	10	RW	Internal QoS value when RX packet's QoS = 4
[11:10]	RX_QoS5	10	RW	Internal QoS value when RX packet's QoS = 5
[13:12]	RX_QoS6	11	RW	Internal QoS value when RX packet's QoS = 6
[15:14]	RX_QoS7	11	RW	Internal QoS value when RX packet's QoS = 7
[18:16]	Reserved	000	RW	Reserved
[19]	Reserved	0	R	Reserved
[26:20]	Reserved	0x00	RW	Reserved
[27]	Reserved	0	R	Reserved
[31:28]	Reserved	0000	RW	Reserved

5.1.83 Port 2 802.1 Q Configuration for UnTag Frame Register (P2QCR)

Address 0x288

Bit	Name	Default Value	R/W	Function
[11:0]	PVID	0x001	RW	VLAN ID value (1 ~ 4095, default 1)
[12]	CF	0	RW	CF Flag
[15:13]	QoS	000	RW	QoS value
[31:16]	Reserved	0x0000	R	Reserved

* This Tag information will be inserted when untag frame is received.

5.1.84 Port 2 RX per Queue Rate Limit Control Register 0 (P2RQR0)

Address 0x28C

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q0_rate	0xFFF	RW	Port 2 RX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q1_rate	0xFFF	RW	Port 2 RX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.85 Port 2 RX per Queue Rate Limit Control Register 1 (P2RQR1)

Address 0x290

Bit	Name	Default Value	R/W	Function
[11:0]	Rx_q2_rate	0xFFF	RW	Port 2 RX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Rx_q3_rate	0xFFF	RW	Port 2 RX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable RX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.86 Port 2 TX per Queue Rate Limit Control Register 0 (P2TQR0)

Address 0x294

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q0_rate	0xFFF	RW	Port 2 TX queue 0 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 0 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q1_rate	0xFFF	RW	Port 2 TX queue 1 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 1 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.87 Port 2 TX per Queue Rate Limit Control Register 1 (P2TQR1)

Address 0x298

Bit	Name	Default Value	R/W	Function
[11:0]	Tx_q2_rate	0xFFF	RW	Port 2 TX queue 2 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 2 rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	Tx_q3_rate	0xFFF	RW	Port 2 TX queue 3 rate limit (4K bytes per unit) The default value 0xFFF means disable TX queue 3 rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.88 Port 2 Rate Limit Control Register (P2RLR)

Address 0x29C

Bit	Name	Default Value	R/W	Function
[11:0]	ingress_rate	0xFFF	RW	Port 0 RX rate limit (4K bytes per unit) For example, if ingress_rate=16 means port 0 can receive 64K byte within P0RLTR Cycle_time window (one second). 0xFFF means disable RX per port rate limit.
[15:12]	Reserved	0000	R	Reserved
[27:16]	egress_rate	0xFFF	RW	Port 0 TX per port rate limit (4K bytes per unit) 0xFFF means disable TX per port rate limit.
[31:28]	Reserved	0000	R	Reserved

5.1.89 Port 2 Rate Limit Timer Register (P2RLTR)

Address 0x2A0

Bit	Name	Default Value	R/W	Function
[26:0]	Cycle_time	0x5F5E100	RW	Per port timer for rate limit calculation. (Default 1 sec.) 2 Second = 10 ^ 8 ns = 0x5F5E100 x 10ns (100MHz clock cycle time)
[31:27]	Reserved	00000	R	Reserved

5.1.90 Port 2 Flow Control High/Low Watermark Register (P2FCR)

Address 0x2A4

Bit	Name	Default Value	R/W	Function
[7:0]	FCHW	0x28	RW	Flow Control High-water mark [7:0]: RX accumulate page count high water level, once internal RX receiving page counter higher than this threshold and Flow control is enabled, then TX MAC will send Pause ON Frame out to informal remote PHY stop sending packets.
[15:8]	FCLW	0x14	RW	Flow Control Low-water mark [7:0]: When Flow control is enabled and pause is ON, RX receiving page counter if lower than this low water mark value then TX MAC will send pause OFF frame to inform remote PHY back to normal state.
[31:16]	Reserved	0x0000	R	Reserved

5.1.91 Port 2 Queue Weighting Configuration Register (P2QWR)

Address 0x2A8

Bit	Name	Default Value	R/W	Function
[3:0]	Q0_Weight	1111	RW	Q0 weighting control for BMU scheduler module usage. The default value is 1111 means disable weighting control. Otherwise buffer management unit will schedule TX output packet based on Q0/Q1/Q2/Q3 weighting distribution.
[7:4]	Q1_Weight	1111	RW	Q1 weighting control for BMU scheduler module usage
[11:8]	Q2_Weight	1111	RW	Q2 weighting control for BMU scheduler module usage
[15:12]	Q3_Weight	1111	RW	Q3 weighting control for BMU scheduler module usage For example if Q0_Weight=1, Q1_Weight=2, Q2_Weight=4 and Q3_Weight=8 then the output packets will have this ratio 8:4:2:1 if all the packets are the same size. The weighting here will based on the page count. There are 128 bytes in a page.
[31:16]	Reserved	0x0000	R	Reserved

5.1.92 Port 2 DA MAC Address Register (P2DAR0, P2DAR1)

Address 0x2B0 (P2DAR0)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC2 [47:40]	0x00	RW	Default DA MAC2 address for Port 2 only valid when DAMatchEn is set to one.(P2MCR [18]) DA MAC2 address [47:40]
[15:8]	DAMAC2 [39:32]	0x00	RW	DA MAC2 address [39:32]
[23:16]	DAMAC2 [31:24]	0x00	RW	DA MAC2 address [31:24]
[31:24]	DAMAC2 [23:16]	0x00	RW	DA MAC2 address [23:16]

Address 0x2B4 (P2DAR1)

Bit	Name	Default Value	R/W	Function
[7:0]	DAMAC2 [15:8]	0x00	RW	Default DA MAC2 address for Port 2 only valid when DAMatchEn is set to one. (P2MCR [18]) DA MAC2 address [15:8]
[15:8]	DAMAC2 [7:0]	0x00	RW	DA MAC2 address [7:0]
[31:16]	Reserved	0x0000	R	Reserved

5.1.93 GPIO Wakeup Register (GPIOWR)

Address 0x2BC

Bit	Name	Default Value	R/W	Function
[5:0]	GPIO_Wakeup_En[5:0]	000000	RW	GPIO5~GPIO0 Wakeup Enable Register When set to one will enable GPIO Wakeup Function 1: Enable GPIO Wakeup function 0: Disable
[7:6]	Reserved	00	R	Reserved
[19:8]	GPIO_Wakeup_Sel[11:0]	0x000	RW	GPI4~GPI0 Wakeup Select Register GPIO_Wakeup_Sel[1:0]:GPIO0 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[3:2]:GPIO1 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[5:4]:GPIO2 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[7:6]:GPIO3 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[9:8]:GPIO4 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[11:10]:GPIO5 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high
[23:20]	Reserved	0000	R	Reserved
[29:24]	GPIO_Wakeup_Status[5:0]	000000	R	GPIO5~GPIO0 Wakeup Status Register 1: Wakeup State 0: Normal State
[31:30]	Reserved	00	R	Reserved

5.1.94 Output Clock Select Register (OCSR)

Address 0x13C

Bit	Name	Default Value	R/W	Function
[7:0]	OCSR[7:0]	0x00	RW	0x41 : Enable internal 50 MHz clock (divider-by 2 from PHY PLL) as RMII 50MHz reference clock source. 0x00 : Default Value
[31:8]	Reserved	0x000000	RW	Reserved for debug purpose.

5.2 PHY Register Description

Address	Register Name	Function	Default Value
0x00	BMCR	Basic Mode Control Register, basic register	0x3100
0x01	BMSR	Basic Mode status registers, basic register	0x7809
0x02	PHYIDR1	PHY Identifier register 1 extended register	0x003B
0x03	PHYIDR2	PHY Identifier register 2 extended register	0x1871
0x04	ANAR	Auto negotiation advertisement register extended register	0x01E1
0x05	ANLPAR	Auto negotiation link partner ability register, extended register	0x01E0
0x06	ANER	Auto negotiation expansion register, extended register	0x0000
0x07	Reserved	Reserved and currently not supported	0x0000
0x08 – 0x13	Reserved	IEEE 802.3u reserved	0x0000

5.2.1 Basic Mode Control Register (BMCR)

Address 0x00

Bit	Name	Default Value	R/W	Function
[6:0]	Reserved	X	RO	PCI configure register: Device select timing.
[7]	Collision_test	0	RW	Collision test: 1 = Collision test enable 0 = Normal operation
[8]	Duplex_mode	1	RW	Duplex mode: 1 = Full duplex operation 0 = Normal operation
[9]	Restart_autonegotiation	0	RW	Restart auto negotiation: 1 = Restart auto negotiation 0 = Normal operation
[10]	Isolate	0	RW	Isolate: 1 = Isolate 0 = Normal operation
[11]	Powerdown	0	RW	Power down: 1 = Power down 0 = Normal operation
[12]	Auto-negotiation_enable	1	RW	Auto negotiation enable: 1 = Auto negotiation enabled Bit 8 and 13 of this register are ignored when this bit is set to one 0 = Auto negotiation disabled Bit 8 and 13 of this register determine the link speed mode.
[13]	Speed_selection	1	RW	Speed Select 1 = 100 Mb/s 0 = 10Mb/s
[14]	Loopback	0	RW	Loopback: 1 = Loopback enable 0 = Normal Operation
[15]	Reset	0	RW	Reset 1 = Software reset 0 = Normal Operation

5.2.2 Basic Mode Status Register (BMSR)

Address 0x01

Bit	Name	Default Value	R/W	Function
[0]	Extended_capability	1	RO	Extended capability: 0 = Basic register capable only 1 = Extended register capable
[1]	Jabber_detect	0	RO	Jabber detect: 0 = No Jabber condition is detected 1 = Jabber condition is detected
[2]	Link_status	0	RO	Link Status: 0 = Link is not established 1 = Valid link is established (100 Mbps or 10 Mbps operation)
[3]	Autonegotiation_ability	1	RO	Auto negotiation ability: 0 = This IP is not able to perform auto-negotiation 1 = This IP is able to perform auto-negotiation
[4]	Remote_fault	0	RO	Remote fault: 0 = No remote fault condition detected 1 = Remote fault condition detected (cleared on read or by a chip reset)
[5]	Autonegotiation_complete	0	RO	Auto negotiation complete: 0 = Auto negotiation process is not complete 1 = Auto negotiation process is complete
[6]	MF_preamble_suppression	0	RO	Management Frame (MF) preamble suppression: 0 = This IP will not accept management frames with preamble suppressed 1 = This IP will accept management frames with preamble suppressed
[10:7]	Reserved	0	RO	Reserved: Write as a 0, read as “don’t care”
[11]	10BASE-T_half-duplex	1	RO	10 BASE-T half-duplex capable: 0 = This IP is not able to perform in 10 BASE-T half-duplex mode 1 = This IP is able to perform in 10 BASE-T half-duplex mode
[12]	10BASE-T_full-duplex	1	RO	10 BASE-T full-duplex capable: 0 = This IP is not able to perform in 10 BASE-T full-duplex mode 1 = This IP is able to perform in 10 BASE-T full-duplex mode
[13]	100BASE-TX_half-duplex	1	RO	100 BASE-TX half-duplex capable: 0 = This IP is not able to perform in 100 BASE-TX half-duplex mode 1 = This IP is able to perform in 100 BASE-TX half-duplex mode
[14]	100BASE-TX_full-duplex	1	RO	100 BASE-TX full-duplex capable: 0 = This IP is not able to perform in 100 BASE-TX full-duplex mode 1 = This IP is able to perform in 100 BASE-TX full-duplex mode
[15]	100BASE-T4	0	RO	100 BASE-T4 capable: 0 = This IP is not able to perform in 100 BASE-T4 mode 1 = This IP is able to perform in 100 BASE-T4 mode

5.2.3 PHY Identifier Register 1 (PHYIDR1)

Address 0x02

Bit	Name	Default Value	R/W	Function
[15:0]	OUI_MSB	0x003B	RO	OUI's most significant bits: This register stores bits 3 to 18 of the OUI to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored. This register is programmable by setting PHYIDRG2 [15:0] and PHYIDRG3 [15:0].

5.2.4 PHY Identifier Register 2 (PHYIDR2)

Address 0x03

Bit	Name	Default Value	R/W	Function
[3:0]	MDL_REV	0x1	RO	Model revision number: Four bits of PHY revision number are mapped to bits 3 to 0 (most significant bit to bit 9) This register is programmable by setting PHYIDRG2 [15:0] and PHYIDRG3 [15:0]
[9:4]	VNDR_MDL	0x07	RO	Vendor model number.
[15:10]	OUI_LSB	0x06	RO	OUI's least significant bits: Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register respectively. This register is programmable by setting PHYIDRG2 [15:0] and PHYIDRG3 [15:0].

5.2.5 Auto-Negotiation Advertisement Register (ANAR)

Address 0x04

Bit	Name	Default Value	R/W	Function
[4:0]	Selector	00001	RW	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. 00001 indicates that this PHY supports IEEE 802.3 CSMA/CD.
[5]	10_HD	1	RW	10 BASE-T half-duplex support: 0 = 10 BASE-T half-duplex is not supported by this PHY. 1 = 10 BASE-T half-duplex is supported by this PHY.
[6]	10_FD	1	RW	10 BASE-T full-duplex support: 0 = 10 BASE-T full-duplex is not supported by this PHY. 1 = 10 BASE-T full-duplex is supported by this PHY.
[7]	TX_HD	1	RW	100 BASE-TX half-duplex support: 0 = 100 BASE-TX half-duplex is not supported by this PHY. 1 = 100 BASE-TX half-duplex is supported by this PHY.
[8]	TX_FD	1	RW	100 BASE-TX full-duplex support: 0 = 100 BASE-TX full duplex is not supported by this PHY. 1 = 100 BASE-TX full duplex is supported by this PHY.
[9]	T4	0	RO	100 BASE-T4 support: 0 = 100 BASE-T4 is not supported by this PHY. 1 = 100 BASE-T4 is supported by this PHY.
[10]	Pause	1	RW	Pause: 0 = Pause operation is not enabled 1 = Pause operation is enabled for full-duplex links
[12:11]	Reserved	X	RW	Reserved. Write as a 0, read as “don’t care”
[13]	RF	0	RW	Remote fault: (not supported) 0 = No fault detected 1 = Fault condition detected and advertised
[14]	ACK	0	RO	Acknowledge: 0 = Not acknowledged 1 = Link partner ability data reception acknowledged
[15]	NP	0	RO	Next page indication: 0 = No next page available 1 = Next page available The PHY does not support the next page function

5.2.6 Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address 0x05

Bit	Name	Default Value	R/W	Function
[4:0]	Selector	00000	RW	Protocol selection bits: Link partner's binary encoded protocol selector
[5]	10_HD	1	RW	10 BASE-T half duplex support: 0 = 10 BASE-T half duplex not supported by link partner 1 = 10 BASE-T half duplex supported by link partner
[6]	10_FD	1	RW	10 BASE-T full duplex support: 0 = 10 BASE-T full duplex not supported by link partner. 1 = 10 BASE-T full duplex supported by link partner.
[7]	TX_HD	1	RW	100 BASE-TX half duplex support: 0 = 100 BASE-TX half duplex not supported by link partner. 1 = 100 BASE-TX half duplex supported by link partner.
[8]	TX_FD	1	RW	100 BASE-TX full duplex support: 0 = 100 BASE-TX full duplex not supported by link partner. 1 = 100 BASE-TX full duplex supported by link partner.
[9]	T4	0	RO	100 BASE-T4 support: 0 = 100 BASE-T4 is not supported by link partner. 1 = 100 BASE-T4 is supported by link partner.
[10]	Pause	0	RW	Pause: 0 = Pause operation is not supported by link partner 1 = Pause operation is supported by link partner
[12:11]	Reserved	X	RW	Reserved. Write as a 0, read as "don't care"
[13]	RF	0	RW	Remote fault: (not supported) 0 = No remote fault detected by link partner 1 = Remote fault detected by link partner
[14]	ACK	0	RO	Acknowledge: 0 = Not acknowledged 1 = Link partner ability data reception acknowledged
[15]	NP	0	RO	Next page indication: 0 = Link partner is not next page enable 1 = Link partner is Next page enable

5.2.7 Auto-Negotiation Expansion Register (ANER)

Address 0x06

Bit	Name	Default Value	R/W	Function
[0]	LP_AN_AB	0	RO	Link partner auto-negotiation enable: 0 = Link partner auto-negotiation is not supported 1 = Link partner auto-negotiation is supported
[1]	Page_RX	0	RO	New page received: 0 = New page is not received 1 = New page is received
[2]	NP_AB	0	RO	PHY next page enable: 0 = PHY is not next page enable 1 = PHY is next page enable
[3]	LP_NP_AB	0	RO	Link partner next page enable: 0 = Link partner is not next page enable 1 = Link partner is next page enable
[4]	PDF	0	RO	Parallel detection fault: 0 = No fault detected 1 = Fault detected via the parallel detection function
[15:5]	Reserved	0	RO	Reserved Write as a 0, read as “don’t care”

5.3 Reverse Mode PHY Register Description

Address	Register Name	Function	Default Value
0x00	Rev_BMCR	Basic Mode Control Register, basic register	0x3100
0x01	Rev_BMSR	Basic Mode status registers, basic register	0x7809
0x04	Rev_ANAR	Auto negotiation advertisement register extended register	0x05E1
0x05	Rev_ANLPAR	Auto negotiation link partner ability register, extended register	0x01E0
0x10	Rev_LUCR	Local User-Defined Control Register	0x0000
0x11	Rev_RUCR	Remote User-Defined Control Register	0x0000

NOTE1: The AX88782/AX88783 only support MDC/MDIO write on Rev_BMCR loopback function and Rev_RUCR register

NOTE2: The Rev_BMSR Link_status will set to one when P0MCR/P1MCR/P2MCR [0] MAC_Enable is set to one.

5.3.1 Basic Mode Control Register (Rev_BMCR)

Address 0x00

Bit	Name	Default Value	R/W	Function
[6:0]	Reserved	0	RO	PCI configure register: Device select timing.
[7]	Collision_test	0	RO	Collision test: 1 = Collision test enable 0 = Normal operation
[8]	Duplex_mode	1	RO	Duplex mode: 1 = Full duplex operation 0 = Normal operation
[9]	Restart_autonegotiation	0	RO	Restart auto negotiation: 1 = Restart auto negotiation 0 = Normal operation
[10]	Isolate	0	RO	Isolate: 1 = Isolate 0 = Normal operation
[11]	Powerdown	0	RO	Power down: 1 = Power down 0 = Normal operation
[12]	Autonegotiation_enable	1	RO	Auto negotiation enable: 1 = Auto negotiation enabled Bit 8 and 13 of this register are ignored when this bit is set to one 0 = Auto negotiation disabled Bit 8 and 13 of this register determine the link speed mode.
[13]	Speed_selection	1	RO	Speed Select 1 = 100 Mb/s 0 = 10Mb/s
[14]	Loopback	0	RW	Loopback: 1 = Loopback enable 0 = Normal Operation
[15]	Reset	0	RO	Reset 1 = Software reset 0 = Normal Operation

5.3.2 Basic Mode Status Register (Rev_BMSR)

Address 0x01

Bit	Name	Default Value	R/W	Function
[0]	Extended_capability	1	RO	Extended capability: 0 = Basic register capable only 1 = Extended register capable
[1]	Jabber_detect	0	RO	Jabber detect: 0 = No Jabber condition is detected 1 = Jabber condition is detected
[2]	Link_status	0	RO	Link Status: 0 = Link is not established 1 = Valid link is established (100 Mbps or 10 Mbps operation)
[3]	Autonegotiation_ability	1	RO	Auto negotiation ability: 0 = This IP is not able to perform auto-negotiation 1 = This IP is able to perform auto-negotiation
[4]	Remote_fault	0	RO	Remote fault: 0 = No remote fault condition detected 1 = Remote fault condition detected (cleared on read or by a chip reset)
[5]	Autonegotiation_complete	0	RO	Auto negotiation complete: 0 = Auto negotiation process is not complete 1 = Auto negotiation process is complete
[6]	MF_preamble_suppression	0	RO	Management Frame (MF) preamble suppression: 0 = This IP will not accept management frames with preamble suppressed 1 = This IP will accept management frames with preamble suppressed
[10:7]	Reserved	0	RO	Reserved: Write as a 0, read as “don’t care”
[11]	10BASE-T_half-duplex	1	RO	10 BASE-T half-duplex capable: 0 = This IP is not able to perform in 10 BASE-T half-duplex mode 1 = This IP is able to perform in 10 BASE-T half-duplex mode
[12]	10BASE-T_full-duplex	1	RO	10 BASE-T full-duplex capable: 0 = This IP is not able to perform in 10 BASE-T full-duplex mode 1 = This IP is able to perform in 10 BASE-T full-duplex mode
[13]	100BASE-TX_half-duplex	1	RO	100 BASE-TX half-duplex capable: 0 = This IP is not able to perform in 100 BASE-TX half-duplex mode 1 = This IP is able to perform in 100 BASE-TX half-duplex mode
[14]	100BASE-TX_full-duplex	1	RO	100 BASE-TX full-duplex capable: 0 = This IP is not able to perform in 100 BASE-TX full-duplex mode 1 = This IP is able to perform in 100 BASE-TX full-duplex mode
[15]	100BASE-T4	0	RO	100 BASE-T4 capable: 0 = This IP is not able to perform in 100 BASE-T4 mode 1 = This IP is able to perform in 100 BASE-T4 mode

5.3.3 Auto-Negotiation Advertisement Register (Rev_ANAR)

Address 0x04

Bit	Name	Default Value	R/W	Function
[4:0]	Selector	00001	RO	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. 00001 indicates that this PHY supports IEEE 802.3 CSMA/CD.
[5]	10_HD	1	RO	10 BASE-T half-duplex support: 0 = 10 BASE-T half-duplex is not supported by this PHY. 1 = 10 BASE-T half-duplex is supported by this PHY.
[6]	10_FD	1	RO	10 BASE-T full-duplex support: 0 = 10 BASE-T full-duplex is not supported by this PHY. 1 = 10 BASE-T full-duplex is supported by this PHY.
[7]	TX_HD	1	RO	100 BASE-TX half-duplex support: 0 = 100 BASE-TX half-duplex is not supported by this PHY. 1 = 100 BASE-TX half-duplex is supported by this PHY.
[8]	TX_FD	1	RO	100 BASE-TX full-duplex support: 0 = 100 BASE-TX full duplex is not supported by this PHY. 1 = 100 BASE-TX full duplex is supported by this PHY.
[9]	T4	0	RO	100 BASE-T4 support: 0 = 100 BASE-T4 is not supported by this PHY. 1 = 100 BASE-T4 is supported by this PHY.
[10]	Pause	1	RO	Pause: 0 = Pause operation is not enabled 1 = Pause operation is enabled for full-duplex links
[12:11]	Reserved	0	RO	Reserved. Write as a 0, read as “don’t care”
[13]	RF	0	RO	Remote fault: (not supported) 0 = No fault detected 1 = Fault condition detected and advertised
[14]	ACK	0	RO	Acknowledge: 0 = Not acknowledged 1 = Link partner ability data reception acknowledged
[15]	NP	0	RO	Next page indication: 0 = No next page available 1 = Next page available The PHY does not support the next page function

5.3.4 Auto-Negotiation Link Partner Ability Register (Rev_ANLPAR)

Address 0x05

Bit	Name	Default Value	R/W	Function
[4:0]	Selector	00000	RO	Protocol selection bits: Link partner's binary encoded protocol selector
[5]	10_HD	1	RO	10 BASE-T half duplex support: 0 = 10 BASE-T half duplex not supported by link partner 1 = 10 BASE-T half duplex supported by link partner
[6]	10_FD	1	RO	10 BASE-T full duplex support: 0 = 10 BASE-T full duplex not supported by link partner. 1 = 10 BASE-T full duplex supported by link partner.
[7]	TX_HD	1	RO	100 BASE-TX half duplex support: 0 = 100 BASE-TX half duplex not supported by link partner. 1 = 100 BASE-TX half duplex supported by link partner.
[8]	TX_FD	1	RO	100 BASE-TX full duplex support: 0 = 100 BASE-TX full duplex not supported by link partner. 1 = 100 BASE-TX full duplex supported by link partner.
[9]	T4	0	RO	100 BASE-T4 support: 0 = 100 BASE-T4 is not supported by link partner. 1 = 100 BASE-T4 is supported by link partner.
[10]	Pause	0	RO	Pause: 0 = Pause operation is not supported by link partner 1 = Pause operation is supported by link partner
[12:11]	Reserved	X	RO	Reserved. Write as a 0, read as "don't care"
[13]	RF	0	RO	Remote fault: (not supported) 0 = No remote fault detected by link partner 1 = Remote fault detected by link partner
[14]	ACK	0	RO	Acknowledge: 0 = Not acknowledged 1 = Link partner ability data reception acknowledged
[15]	NP	0	RO	Next page indication: 0 = Link partner is not next page enable 1 = Link partner is Next page enable

5.3.5 Local User-Defined Control Register (Rev_LUCR)

Address 0x10

Bit	Name	Default Value	R/W	Function
[15:0]	LocalUser-Data	0x0000	RO	User-Defined Local Control Data information

5.3.6 Remote User-Defined Control Register (Rev_RUCR)

Address 0x11

Bit	Name	Default Value	R/W	Function
[15:0]	RemoteUser-Data	0x0000	RW	User-Defined Remote Control Data information

6.0 ELECTRICAL SPECIFICATION AND TIMING

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Description	Rating	Units
VCCK (Core power supply), V18(voltage regulator), P0_VCC18A, P1_VCC18A (analog power supply for oscillator, PLL, PHY)	-0.3 to 2.16	V
VCC3IO (power supply for 3.3V I/O), VCCAH(voltage regulator), P0_VCC33A, P1_VCC33A(analog power supply for bandgap)	-0.3 to 4.0	V
Storage Temperature	-40 to 150	°C
I_{IN} (DC input current)	20	mA
I_{OUT} (Output short circuit current)	20	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability

6.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
P0_VCC18A, P1_VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCCAH	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
P0_VCC33A, P1_VCC33A	Analog power supply for bandgap	2.97	3.3	3.63	V
V_{IN18}	Input voltage of 1.8 V I/O	0	1.8	1.98	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.63	V
T_j	Commercial junction operating temperature	-40	25	125	℃
T_a	Commercial operating temperature	0	-	70	℃

6.1.3 DC Characteristics of 3.3V I/O (VCC3IO = 3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	LVTTL spec.			0.8	V
Vih	Input high voltage		2.0			V
Vt-	Schmitt-trigger negative threshold voltage	LVTTL spec.	0.8			V
Vt+	Schmitt-trigger negative threshold voltage				2.0	
Vol	Output low voltage	Iol = 2 ~ 12 mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -2 ~ -12 mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-15	-45	-90	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	90	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.4 DC Characteristics of 2.5V I/O (VCC3IO = 2.5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 2.5V I/O	2.5V I/O	2.25	2.5	2.75	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.25* VCC3IO	V
Vih	Input high voltage		0.625* VCC3IO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.25* VCC3IO			V
Vt+	Schmitt-trigger negative threshold voltage				0.625* VCC3IO	
Vol	Output low voltage	Iol =1.1 ~ 6.68mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -1.1 ~ -6.6mA	1.85	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	40	110	290	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	110	290	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-7	-23	-62	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	7	23	62	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.5 DC Characteristics of 1.8 V I/O (VCC3IO = 1.8V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 1.8V I/O	1.8V I/O	1.62	1.8	1.98	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.3* VCC3IO	V
Vih	Input high voltage		0.7* VCC3IO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.3* VCC3IO			V
Vt+	Schmitt-trigger negative threshold voltage				0.7* VCC3IO	
Vol	Output low voltage	Iol = 0.7 ~ 4.2mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -0.7 ~ -4.2mA	0.7* VCC3IO	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	80	200	510	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	80	200	510	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-3	-9	-25	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	3	9	25	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCCAH	Power supply of on-chip voltage regulator.		2.7	3.3	3.6	V
Tj	Operating junction temperature.		-40	25	125	℃
Iload_v18	Driving current.	Normal operation,	-	-	300	mA
	Driving current.	Standby mode enabled,	-	-	30	mA
V18	Output voltage of on-chip voltage regulator.	VCCAH = 3.3V After trimming	1.71	1.8	1.89	V
		VCCAH = 2.7V Iload_v18=300mA	1.71	1.8	1.89	
		VCCAH=3.6V STB=1 Iload_v18_stb=30 mA Tj=25℃	1.71	1.8	1.89	
		VCCAH=3.3V STB=1 Iload_v18_stb=30 mA Tj=25℃	1.71	1.8	1.89	
Vdrop	Dropout voltage.	△V18 = -1%, Iload_v18 = 10mA	-	0.1	0.2	V
$\frac{\triangle V18}{(\triangle VCCAH \times V18)}$	Line regulation.	VCCAH = 2.7 ~ 3.6V, Iload_v18 = 50mA	-	0.2	0.4	%/V
$\frac{\triangle V18}{(\triangle Iload\_v18 \times V18)}$	Load regulation.	VCCAH = 3.3V, 1mA ≦ Iload_v18 ≦ 300mA	-	0.006	0.012	%/mA
$\frac{\triangle V18}{\triangle Tj}$	Temperature coefficient.	VCCAH = 3.3V, -40℃ ≦ Tj ≦ 125℃ Iload_v18=10mA	-	0.1	0.2	mV/℃
Iq_25℃	Quiescent current at 25 ℃.	VCCAH = 3.3V, STB = 0	-	100	165	μA
		VCCAH = 3.3V, STB = 1	-	70	100	μA
Iq_125℃	Quiescent current at 125 ℃.	VCCAH = 3.3V, STB = 0	-	125	185	μA
		VCCAH = 3.3V, STB = 1	-	85	115	μA
Idis	Disable current			1	3	μA
Cout	Output external capacitor.		0.1	1	-	μF
△Vtransient	Voltage drop due to current transient effect	VCCAH = 3.3V Cout = 1μF Tr = Tf = 10 ns		0.3		V
ESR	Allowable effective series resistance of external capacitor.		-	0.5	1	Ω

6.2 Thermal Characteristics

A. Junction to ambient thermal resistance, θ_{JA}

Symbol	Min	Typ	Max	Units
θ_{JA}	-	25.2 (AX88782) 24.4(AX88783)	-	°C/W

B. Junction to case thermal resistance, θ_{JC}

Symbol	Min	Typ	Max	Units
θ_{JC}	-	9.6(AX88782) 9.5(AX88783)		°C/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P},\ \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature
T_A: ambient or environment temperature
T_C: the top center of compound surface temperature
P: input power (watts)

6.3 Power Consumption

- **Device only**

  Power measurements base on 3.3V/25 °C condition with the help of current probe.

AX88782	Both Ports @ 10BASE-T Half-Duplex*1			Both Ports @ 100BASE-TX Full-Duplex *1			D1 RemoteWake-up Mode*2			D2 Sleep Mode*3			Both Ports in PHY Power-Down*4			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3.3V*5		58			49			32			3			~1		mA
1.8V*6		166			287			46			5			~1		mA
Total:		224			336			78			8			~1		mA
		739			1109			257			26			~1		mW

AX88783	Both Ports @ 10BASE-T Half-Duplex*1			Both Ports @ 100BASE-TX Full-Duplex *1			D1 RemoteWake-up Mode*2			D2 Sleep Mode*3			Both Ports in PHY Power-Down*4			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3.3V*5		46			46			22			3			~1		mA
1.8V*6		160			282			38			6			~1		mA
Total:		206			328			60			9			~1		mA
		680			1082			198			30			~1		mW

*1: 100% utilization on both ports.
*2: PHY0 Power-On, PHY1 Power-Down, Remote Wake-up function enable for Port 0, core clock ON
*3: Both PHY Power-Down, core clock ON, Write any data to SMER register to go back normal mode
*4: Both PHY Power-Down, core clock OFF
*5: 3.3V current include VCC3IO + P0_VCC3A3 + P1_VCC3A3
*6: 1.8V current include VCCK + P0_VCC18A + P1_VCC18A
Note: The transformer will consume additional 40mA @3.3V for 100BASE-TX and 100mA @3.3V for 10BASE-T

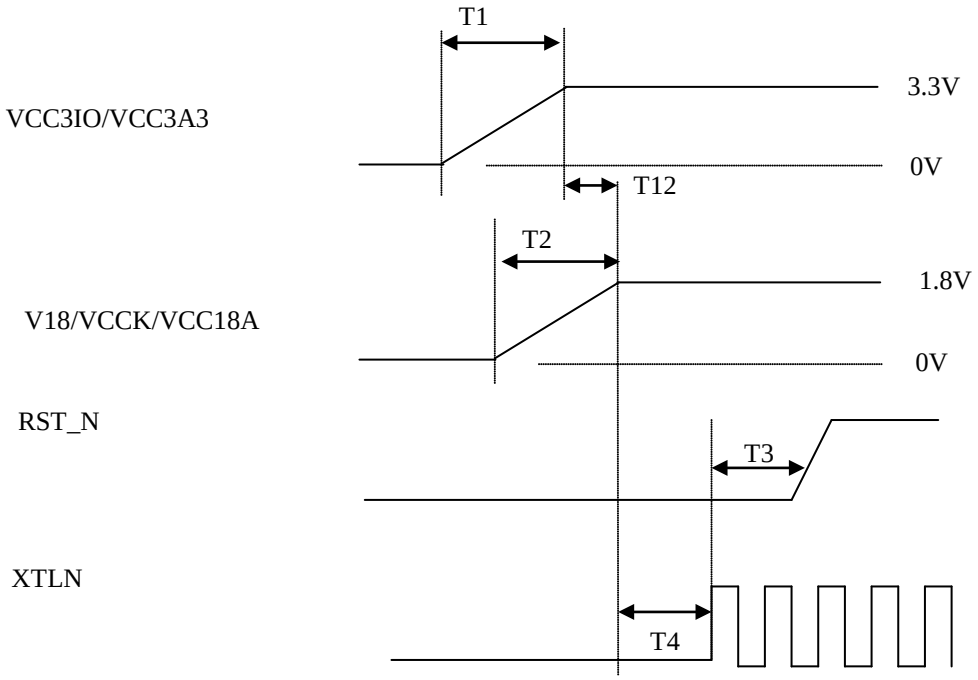
- **Device and system components**

  This is the total of Ethernet connectivity solution, which includes external components such as the Ethernet magnetic, EEPROM, etc.
  Power measurements base on 3.3V/25 °C condition.

Item	Test Conditions (Typical Condition)	AX88782/AX88783			Units
		Min	Typ	Max	
1	10BASE-T operation (Both Ports, Half-Duplex)		1399/1339		mW
2	100BASE-TX operation (Both Ports, Full-Duplex)		1372/1346		mW
3	Cable unplug under power saving mode (Both Ports)		650/660		mW
4	D1 WOL mode (Port 0 PHY Power-On, Port 1 PHY Power-Down, Remote Wake-up supported for port 0)		587/528		mW
5	D2 Sleep mode (Both Ports, Remote Wake-up not supported)		28/32		mW
6.	PHY power down (Both Ports)		<1		mW

6.4 Power-up Sequence

At power-up, the AX88782/AX88783 requires the VCC3IO/VCC3A3 power supply to rise to nominal operating voltage within Trise3 and the V18/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_1	3.3V power supply rise time	From 0V to 3.3V	0.5	-	10	ms
T_2	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
T_{12}	3.3V rise to 1.8V rise time delay		-5	-	5	ms
T3	System Reset rise time after the clock is stable	From VCCIO = 3.3V and VCCK = 1.8V to RST_N going high	200			us
T4	Oscillator stable time	From VCCK = 1.8V	805			us

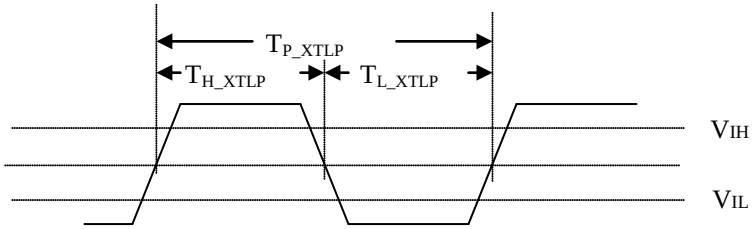
Note: Please read the register 0x000 [16] ChipInitDone to check if the chip has finish initialized process.

6.5 AC specifications

Notice that the following AC timing specifications for output pins are based on CL (Output load) = 50pF.

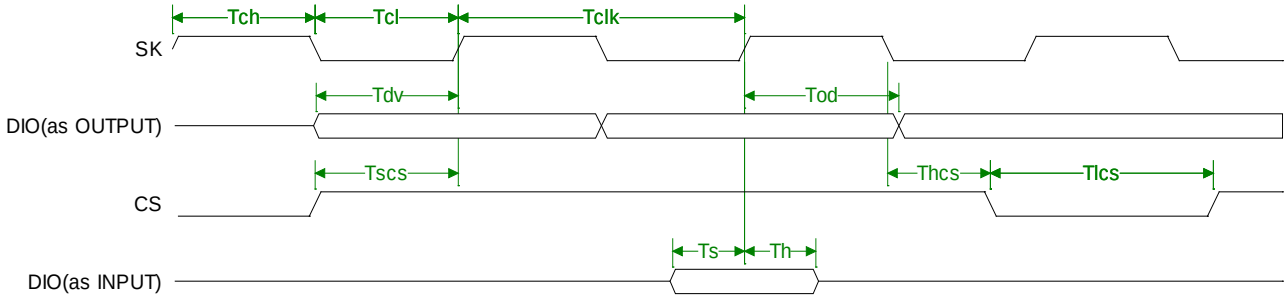
6.5.1 Clock Timing

XTLP



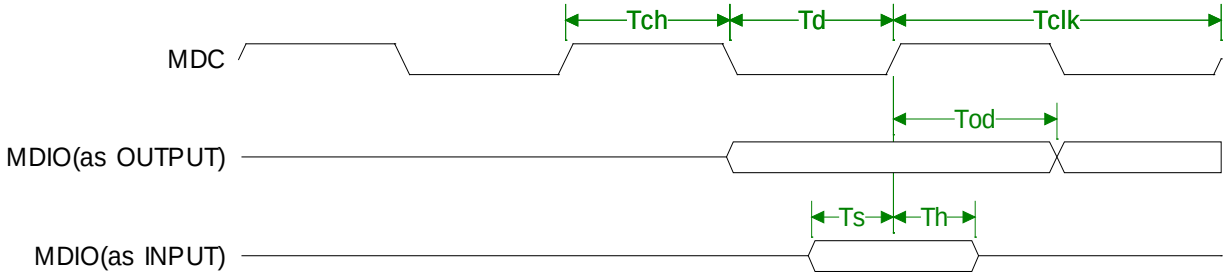
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTLP clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTLP clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTLP clock low time		-	20.0	-	ns

6.5.2 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	SK clock cycle time	-	1000	-	ns
Tch	SK clock high time	-	500	-	ns
Tcl	SK clock low time	-	500	-	ns
Tdv	DIO output valid to SK rising edge time	500	-	-	ns
Tod	SK rising edge to DIO output delay time	500	-	-	ns
Tscs	CS output valid to SK rising edge time	500	-	-	ns
Thcs	SK falling edge to CS invalid time	510	-	-	ns
Tlcs	Minimum CS low time	2050	-	-	ns
Ts	DIO input setup time	10	-	-	ns
Th	DIO input hold time	30	-	-	ns

6.5.3 Station Management Timing (MDIO)



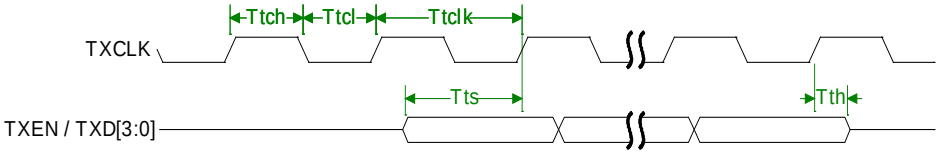
MAC mode with MII: MDC=Output

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	1000	-	ns
Tch	MDC clock high time	-	500	-	ns
Tcl	MDC clock low time	-	500	-	ns
Tod	MDC clock rising edge to MDIO output delay	0.5	-	-	Tclk
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	30	-	-	ns

PHY/Dual-PHY mode with Reverse MII/RMII: MDC=Input

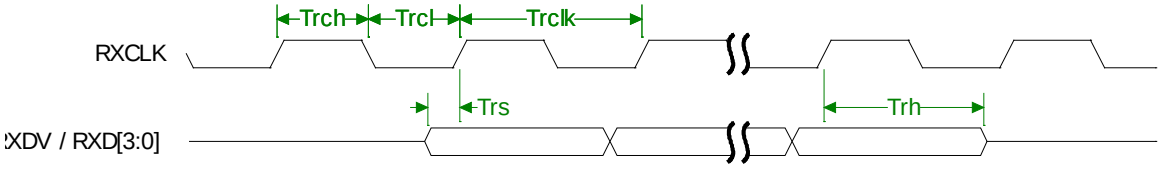
Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	1000	-	ns
Tch	MDC clock high time	-	500	-	ns
Tcl	MDC clock low time	-	500	-	ns
Tod	MDC clock rising edge to MDIO output delay	0	-	300	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	30	-	-	ns

6.5.4 MII Interface Timing



TXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII TX Data bus include MII0_TXD0, MII0_TXD1, MII0_TXD2, MII0_TXD3, MII1_TXD0, MII1_TXD1, MII1_TXD2, and MII1_TXD3.
TXEN: Port 0 and Port 1 MII Transmit Enable (MII0_TX_EN, MII1_TX_EN)

Symbol	Description	Min	Typ	Max	Unit
Ttclk	TXCLK clock cycle time *1	-	40.0	-	ns
Ttch	TXCLK clock high time *2	-	20.0	-	ns
Ttcl	TXCLK clock low time *2	-	20.0	-	ns
Tts	TXD [3:0], TXEN setup to rising TXCLK	23.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	7.0	-	-	ns

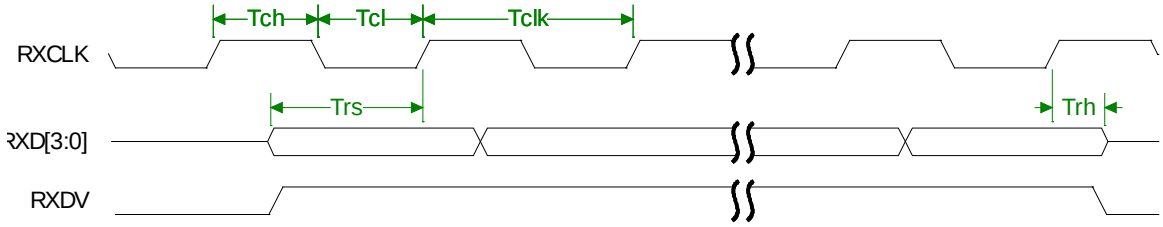


RXCLK: Port 0 and Port 1 MII Receive clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII RX Data bus include MII0_RXD0, MII0_RXD1, MII0_RXD2, MII0_RXD3, MII1_RXD0, MII1_RXD1, MII1_RXD2, and MII1_RXD3.
RXDV: Port 0 and Port 1 MII Receive Data Valid (MII0_RX_DV, MII1_RX_DV)

Symbol	Description	Min	Typ	Max	Unit
Trclk	RXCLK clock cycle time *1	-	40.0	-	ns
Trch	RXCLK clock high time *2	-	20.0	-	ns
Trcl	RXCLK clock low time *2	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	5.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising TXCLK	3.5	-	-	ns

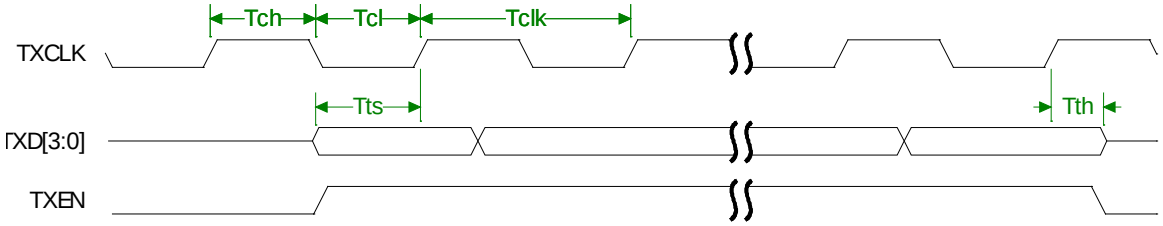
*1: For 10Mbps, the typical value of Ttclk and Trclk shall scale to 400ns.
*2: For 10Mbps, the typical value of Ttch, Ttcl, Trch, and Trcl shall scale to 200ns.

6.5.5 Reverse MII Timing



RXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII Transmit Data bus include MII0_RXD0, MII0_RXD1, MII0_RXD2, MII0_RXD3, MII1_RXD0, MII1_RXD1, MII1_RXD2, and MII1_RXD3.
RXDV: Port 0 and Port 1 MII Transmit Data Valid (MII0_RX_DV, MII1_RX_DV)

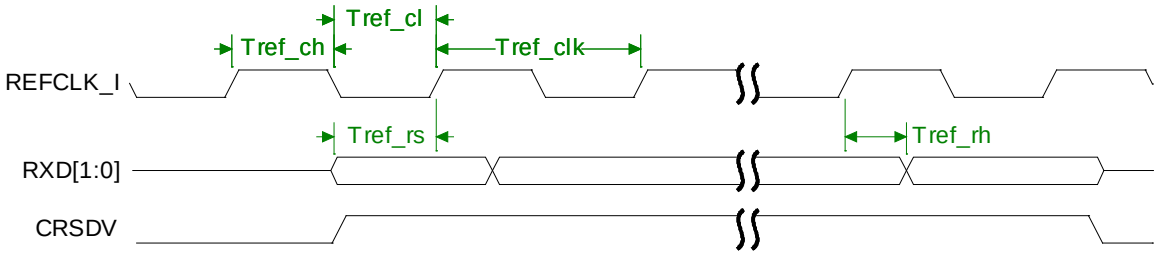
Symbol	Description	Min	Typ	Max	Unit
Tclk	Clock cycle time	-	40.0	-	ns
Tch	Clock high time	-	20.0	-	ns
Tcl	Clock low time	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	10.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising RXCLK	10.0	-	-	ns



TXCLK: Port 0 and Port 1 MII Receive clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII Receive Data bus include MII0_TXD0, MII0_TXD1, MII0_TXD2, MII0_TXD3, MII1_TXD0, MII1_TXD1, MII1_TXD2, and MII1_TXD3.
TXEN: Port 0 and Port 1 MII Receive Data Valid (MII0_TX_EN, MII1_TX_EN)

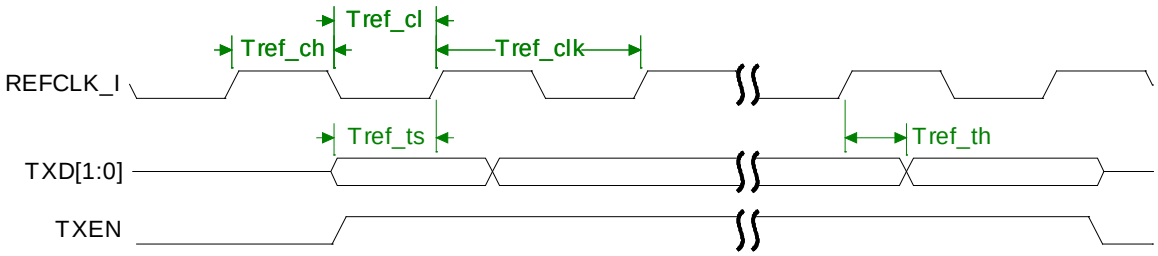
Symbol	Description	Min	Typ	Max	Unit
Tts	TXD [3:0], TXEN setup to rising TXCLK	11.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	2.0	-	-	ns

6.5.6 RMII and Reverse RMII Timing



RXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII Transmit Data bus include MII0_RXD0, MII0_RXD1, MII1_RXD0, and MII1_RXD1.
RXDV: Port 0 and Port 1 MII Transmit Data Valid (MII0_RX_DV, MII1_RX_DV)

Symbol	Description	Min	Typ	Max	Unit
Tref_clk	Clock cycle time	-	20.0	-	ns
Tref_ch	Clock high time	-	10.0	-	ns
Tref_cl	Clock low time	-	10.0	-	ns
Tref_rs	RXD [1:0], CRSDV setup to rising REFCLK_I	4.0	-	-	ns
Tref_rh	RXD [1:0], CRSDV hold from rising REFCLK_I	2.0	-	-	ns



TXCLK: Port 0 and Port 1 MII Receive clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII Receive Data bus include MII0_TXD0, MII0_TXD1, MII1_TXD0, and MII1_TXD1.
TXEN: Port 0 and Port 1 MII Receive Data Valid (MII0_TX_EN, MII1_TX_EN)

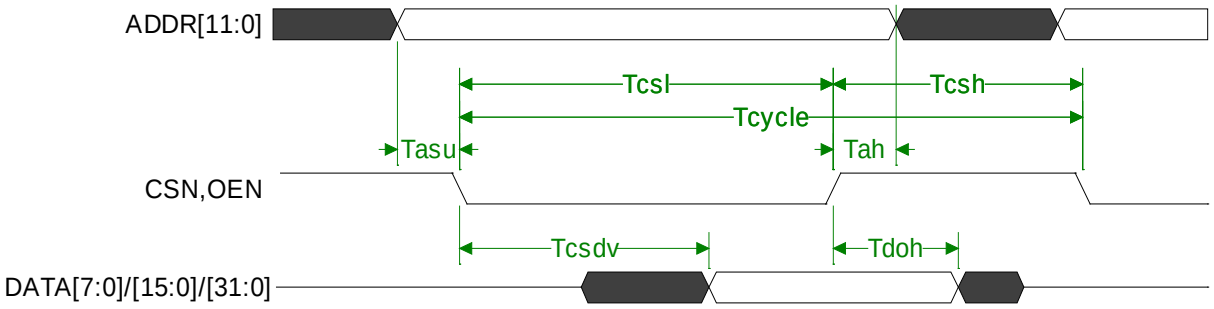
Symbol	Description	Min	Typ	Max	Unit
Tref_ts	TXD [1:0], TXEN setup to rising REFCLK_I	4.0	-	-	ns
Tref_th	TXD [1:0], TXEN hold from rising REFCLK_I	2.0	-	-	ns

6.5.7 CPU Interface Timing

ADDR [11:0]: {CPU_ADDR11, CPU_ADDR10, CPU_ADDR9, CPU_ADDR8, CPU_ADDR7, CPU_ADDR6, CPU_ADDR5, CPU_ADDR4, CPU_ADDR3, CPU_ADDR2, CPU_ADDR1, CPU_ADDR0}

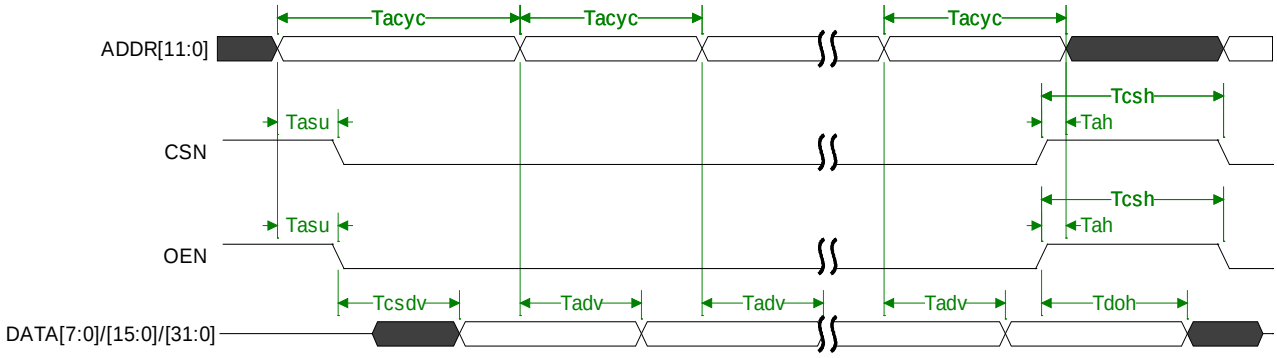
DATA [31:0]: {CPU_DATA31, CPU_DATA30, CPU_DATA29, CPU_DATA28, CPU_DATA27, CPU_DATA26, CPU_DATA25, CPU_DATA24, CPU_DATA23, CPU_DATA22, CPU_DATA21, CPU_DATA20, CPU_DATA19, CPU_DATA18, CPU_DATA17, CPU_DATA16, CPU_DATA15, CPU_DATA14, CPU_DATA13, CPU_DATA12, CPU_DATA11, CPU_DATA10, CPU_DATA9, CPU_DATA8, CPU_DATA7, CPU_DATA6, CPU_DATA5, CPU_DATA4, CPU_DATA3, CPU_DATA2, CPU_DATA1, CPU_DATA0}

CPU Single Read Cycle



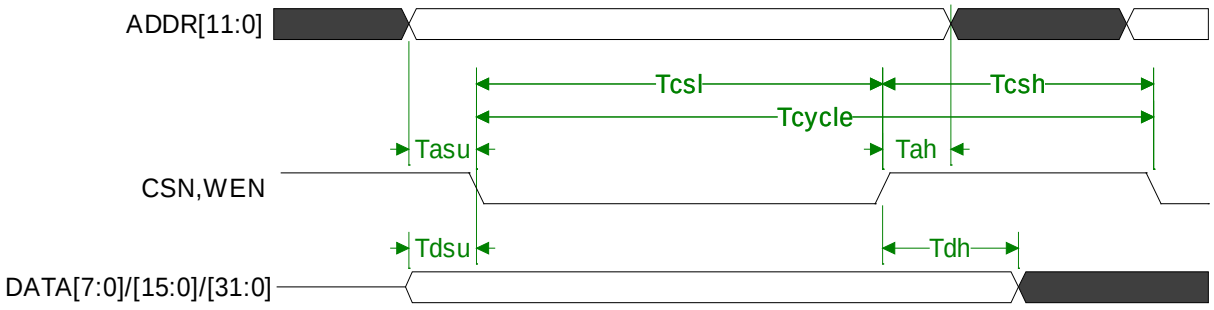
Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	45	-	-	ns
Tcsl	CSN, OEN ASSERT TIME	32	-	-	ns
Tcsh	CSN, OEN DEASSERTION TIME	15	-		ns
Tcsdv	CSN, OEN VALID TO DATA VALID			30	ns
Tasu	ADDRESS SETUP TO CSN, OEN VALID	0			ns
Tah	ADDRESS HOLD TIME	0			ns
Tdoh	DATA OUTPUT HOLD TIME	0			ns

CPU Burst Read Cycle



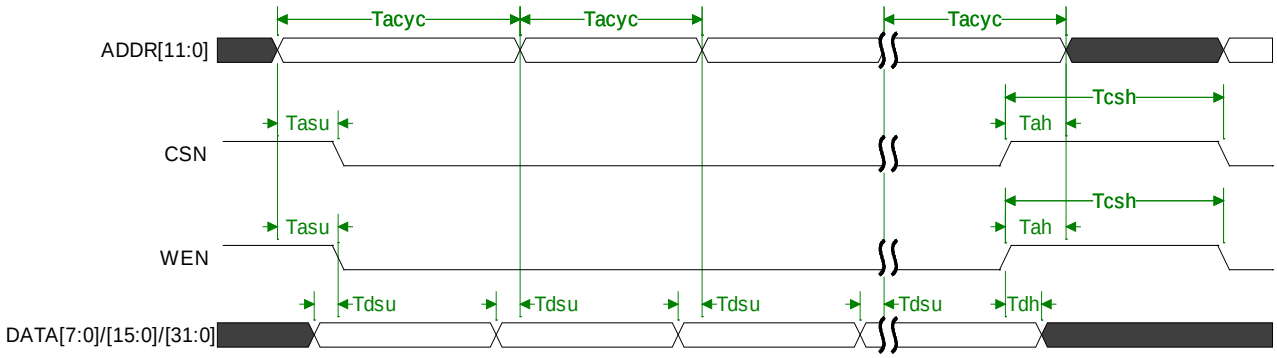
Symbol	Description	Min	Typ.	Max	Units
Tcsh	CSN, OEN DEASSERTION TIME	15			ns
Tcsdv	CSN, OEN VALID TO DATA VALID			30	ns
Tacyc	ADDRESS CYCLE TIME	45			ns
Tasu	ADDRESS SETUP TO CSN, OEN VALID	0			ns
Tadv	ADDRESS STABLE TO DATA VALID			40	ns
Tah	ADDRESS HOLD TIME	0			ns
Tdoh	DATA OUTPUT HOLD TIME	0			ns

CPU Single Write Cycle



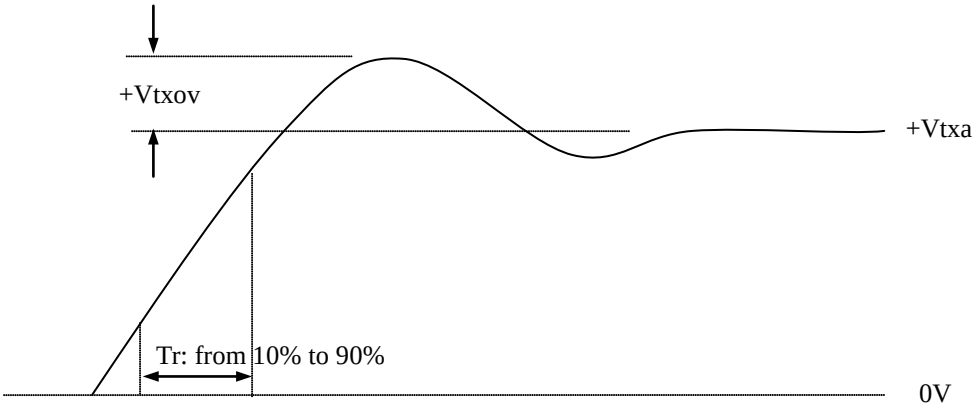
	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TO CSN, WEN ASSERTION	0	-	-	ns
Tdsu	DATA SETUP TO CSN, WEN ASSERTION	0	-	-	ns
Tcycle	WRITE CYCLE TIME	45	-		ns
Tcsl	CSN, WEN ASSERTION TIME	32	-	-	ns
Tcsh	CSN, WEN DEASSERTION TIME	15			ns
Tah	ADDRESS HOLD TIME	0			ns
Tdh	DATA HOLD TIME	0			ns

CPU Burst Write Cycle



Symbol	Description	Min	Typ.	Max	Units
Tcsh	CSN, WEN DEASSERTION TIME	0	-	-	ns
Tacyc	ADDRESS CYCLE TIME	0	-	-	ns
Tasu	ADDRESS SETUP TO CSN, WEN	45	-		ns
Tah	ADDRESS HOLD TIME	32	-	-	ns
Tdsu	DATA SETUP TO CSN, OEN ASSERTION	15			ns
Tdh	DATA HOLD TIME	0			ns

6.5.8 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

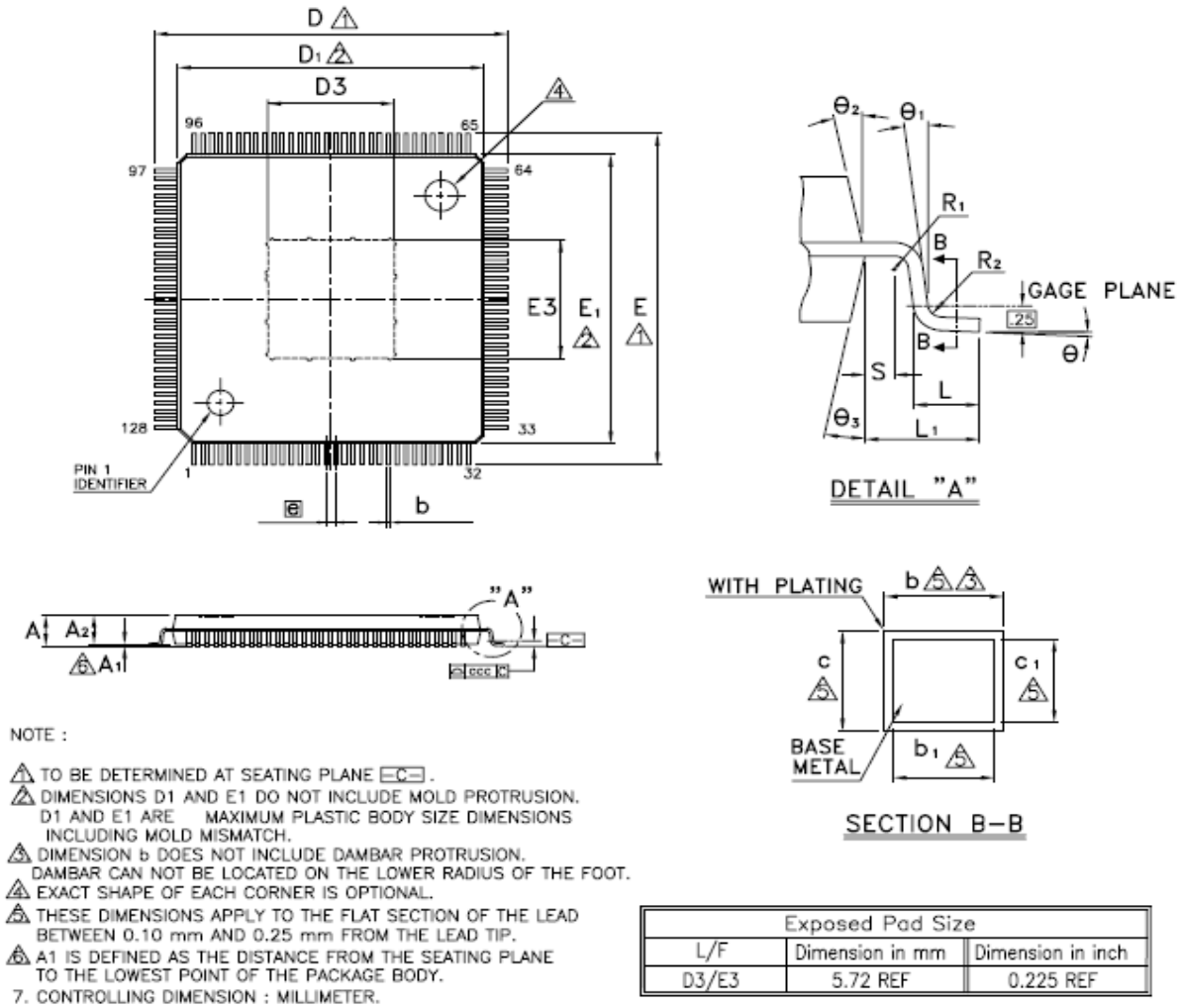
Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

7.0 PACKAGE INFORMATION

7.1 The AX88783 128 Pin LQFP/E-PAD Package



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

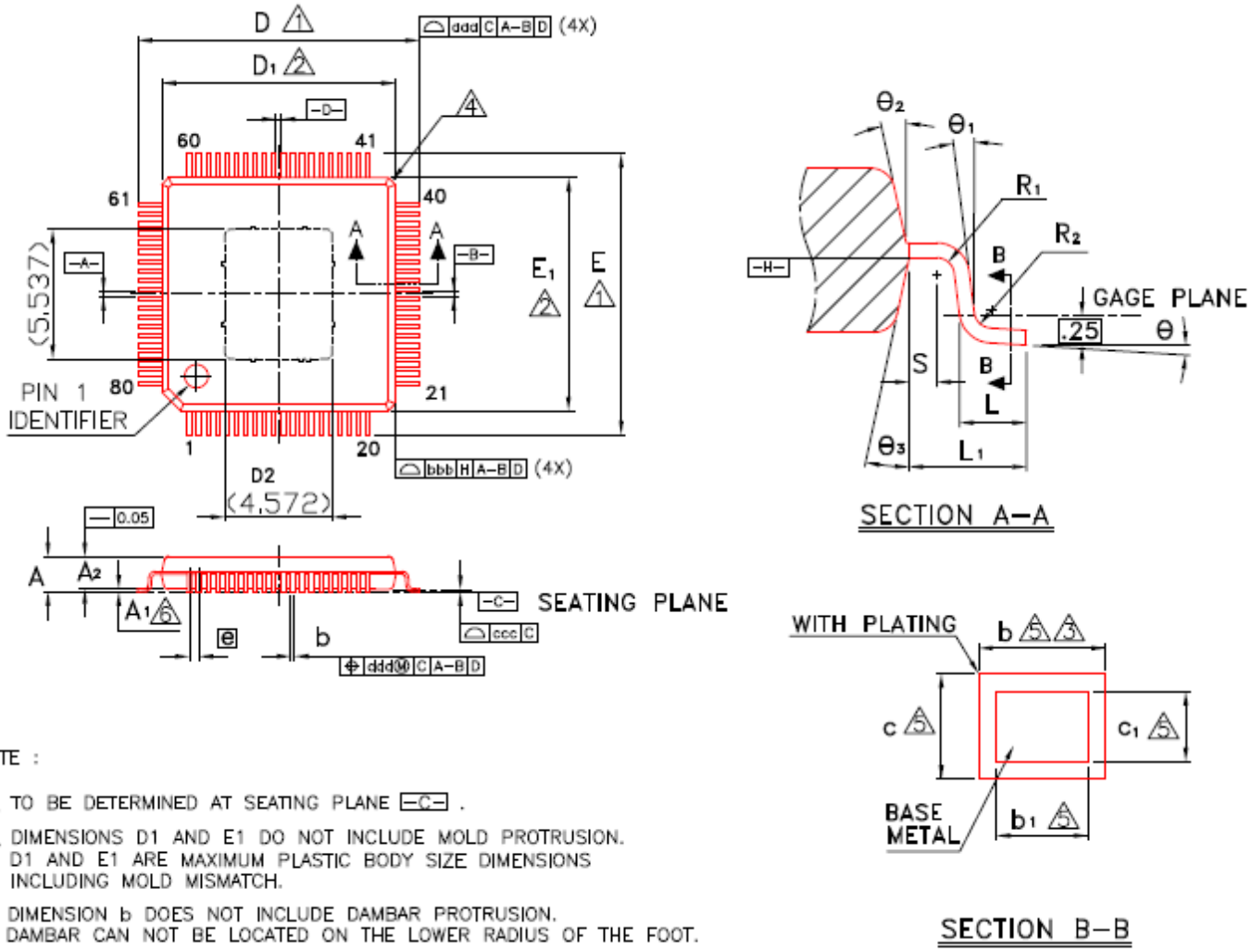
Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	5.72 REF	0.225 REF

Exposed Pad (E-PAD) Information:

The AX88783 has an exposed pad to help transfer heat from the silicon wafer to the PCB. This metallic exposed pad should be tied to ground.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		
ccc	0.08			0.003		

7.2 The AX88782 80 Pin LQFP/E-PAD Package



NOTE :

1. TO BE DETERMINED AT SEATING PLANE –C– .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Exposed Pad (E-PAD) Information:

The AX88782 has an exposed pad to help transfer heat from the silicon wafer to the PCB. This metallic exposed pad should be tied to ground. The exposed pad position is centered with reference to the body.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

8.0 Ordering Information

Part Number	Description
AX88782 LF	80 PIN, LQFP/E-PAD Package, Commercial Grade 0°C to +70 °C (Green, Lead-Free)
AX88783 LF	128 PIN, LQFP/E-PAD Package, Commercial Grade 0°C to +70 °C (Green, Lead-Free)

Revision History

Revision	Date	Comment
V0.10	2008/04/11	Preliminary Release
V0.20	2009/03/04	*Add MLD Snooping information (3.15) *Add EEPROM information (3.20) *Update pinout information (2.1 ~ 2.3) Rename P0_VCC18D to P0_VCC18A and P1_VCC18D to P1_VCC18A Rename P0_GND18D to P0_VCC18A and P1_GND18D to P1_VCC18A *Add GPIO information (3.21) *Update Power consumption table in 6.4
V1.00	2009/04/30	*Update RMON counter information (5.1.24 and 3.13) Remove unused counter on address 0x12 and 0x13 *Add 3.22 CPU Interface Protocol section *Add thermal characteristics table (6.2) *Add power-saving function description (3.5) *Add IPv6 MLD snooping function (3.15) *Add EEPROM example code (3.20) *Add PHY power-saving control bit (5.1.2) *Add PHY cable-off status information (5.1.3) *Add sniffer register IPv4/IPv6 related information (5.1.9) *Add IO pad pull-up and pull-down control register (5.1.36) *Add Endian Configuration register (5.1.53) *Add GPIO wakeup register (5.1.93) and GPIO control register (5.1.38 ~ 5.1.41) *Add multi-voltage 3.3V, 2.5V and 1.8V I/O support (6.3.1 ~ 6.3.3) *The AX88783 pin 123 need an external pull-down resistor (2.1.2 and 2.1.3) * Change bi-directional IO pad abbreviations to B (2.0) * Add bus mode select table in 2.5 MODE2,1,0 bit description * DATA12 should add a pull-down resistor when configured in 8-bit bus mode (2.3) * Add 50MHz RMII reference clock spec. on 2.1.4 and 2.1.5 MII0_REFCLK 2.2.4 and 2.2.5 MII1_REFCLK pin description.
V1.01	2009/09/18	*Modify some information in the Features page. *Modify some descriptions of RMON counter access in Section 3.13. *Modify some descriptions of RCR register in Section 5.1.22. *Add Section 5.1.94 to add the descriptions of OCSR register.
V1.02	2010/03/11	1. Corrected the typo of the MII1_TX_CLK pin's I/O type at MII mode in Section 2.2.2. 2. Added 1.8V power consumption information in Section 6.3. 3. Added the wide operating temperature range (-40 to +75°C) information in Features page.
V1.03	2010/11/25	1. Added the broadcast/flooding/multicast port mapping setting descriptions in Section 5.1.6. 2. Modified some descriptions in Section 2.1.1, 2.2.1, 5.1.33, 5.1.81. 3. Added some descriptions in Section 2.2.2, 4.1.
V1.04	2011/06/16	1. Removed the wide operating temperature range information in Features page. 2. Added copyright legal header information.
V1.05	2012/04/27	1. Updated the IC package information in Section 7.

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