ASIX AX88850
100BASE-TX/FX
Repeater Controller
Data Sheet(11/03/'97)

DOCUMENT NO. : AX850D2.DOC

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1.0 AX88850 Overview

The AX88850 series 100Mbps Repeater Controllers are designed for both low cost dumb HUB and high performance intelligent HUB applications. The AX88850 series product support up-to ten 100Mbps links with its 8 PCS (Physical coding sub-layer , also called Symbol Interface) interfaces and 2 dedicated MII interfaces or supports up-to eighteen 100Mbps links with 2 shared 8 ports MII interfaces and 2 dedicated MII interfaces. Maximum up-to 144 ports can be constructed when using expansion bus cascades 8 AX88850s. The AX88850 is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" . It is fully compatible with IEEE 802.3u standard.

1.1 General Description

The AX88850 Repeater Controller is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. The AX88850 family has two kind of interfaces to connect to PHY devices. There are Physical coding sub-layer (PCS) interface and Media Independent Interface (MII).

The AX88850 supports 8 PCS ports interface or 2 shared bus (8 ports/per bus) MII interfaces, 2 dedicated MII ports interface, an expansion port interface, a management information base IC interface, a repeater ID daisy chain interface, a serial register interface and LED display interface.

1.2 Features

- IEEE 802.3u repeater compatible
- Supports 10 or 18 network connections optional configuration.
- 8 PCS interfaces direct interface to PHY chip with PCS interface (ie.LUC3X04, KS8761, QSI6611, NWK914) to save user cost
- 16 MII interfaces to double the network connections.
- 2 dedicated MII interfaces can also support 100BASE-T4/FX PHY interfaces
- The 2 dedicated MII interfaces can also easily connect to MII interface of 100BASE MAC controller for network management purpose or other bridging devices.
- Up-to 8 repeater chips can be cascaded for large HUB application
- Low latency design supports Class II repeater implementation with large port number.
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Separate carrier integrity monitor state machines for each port to protect network from some transient fault conditions (AX88853 PCS mode only)
- Management interface for AX88856 (MIB IC) allows all repeater MIBs to be maintained
- Large per-port management counters to reduce CPU overhead
- External pins setup or automatic daisy chain channel setup repeater ID.
- Per-port LED display for Jabber, Partition, Link/Activity. Global utilization and collision (%) presentation.
- Power on LED diagnosis. All the LED display will follow the “ON-OFF-ON-OFF-Normal” operation procedure during/after power on reset.
- Dedicated collision LED display
- 208-pin PQFP

The AX88850 Family has the following members:

AX88851	16 shared MII ports + 2 dedicated MII ports
AX88852	8 shared MII ports + 2 dedicated MII ports
AX88853	8 PCS (Symbol) Interface ports + 2 dedicated MII ports
AX88854	AX88851 + AX88853 + management function
AX88856	MIB co-processor for intelligent Hub applications

Function availability list

Parts Number	16MII + 2MII	8MII + 2MII	8PCS + 2MII	Management I/F
AX88851	✓			
AX88852		✓		
AX88853			✓	
AX88854	✓	✓	✓	✓

1.3 Block Diagram

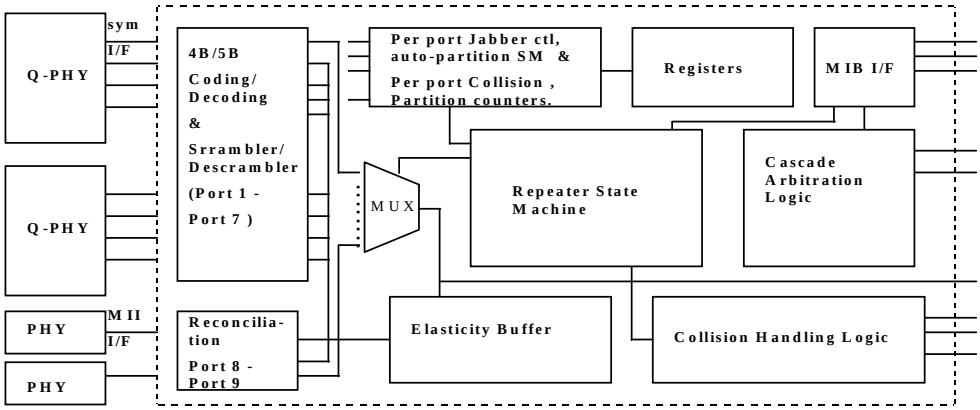


Fig - 1 Chip Block Diagram (PCS mode configuration -- 8 PCS + 2 MII)

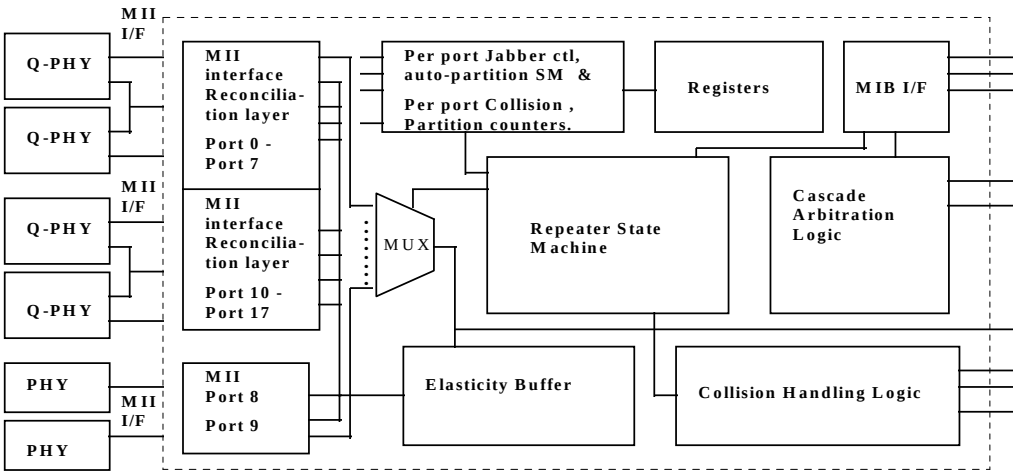


Fig - 2 Chip Block Diagram(MII mode configuration -- 16 MII + 2 MII)

1.4 Pin Connection Diagram for AX88851 (16MII + 2MII mode)

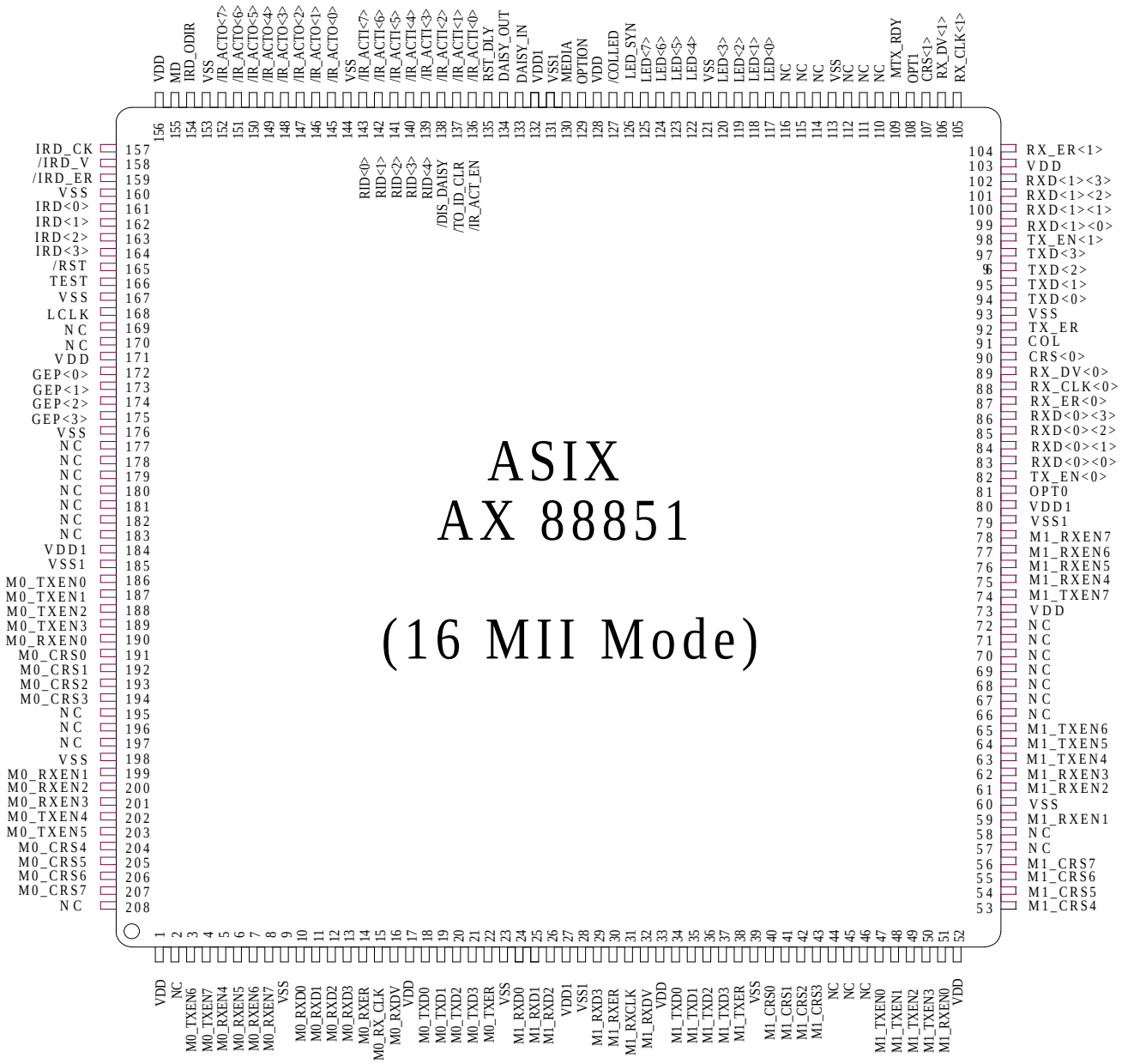


Fig - 3 Pin Connection Diagram for 16MII Mode

1.5 Pin Connection Diagram for AX88852 (8MII + 2MII mode)

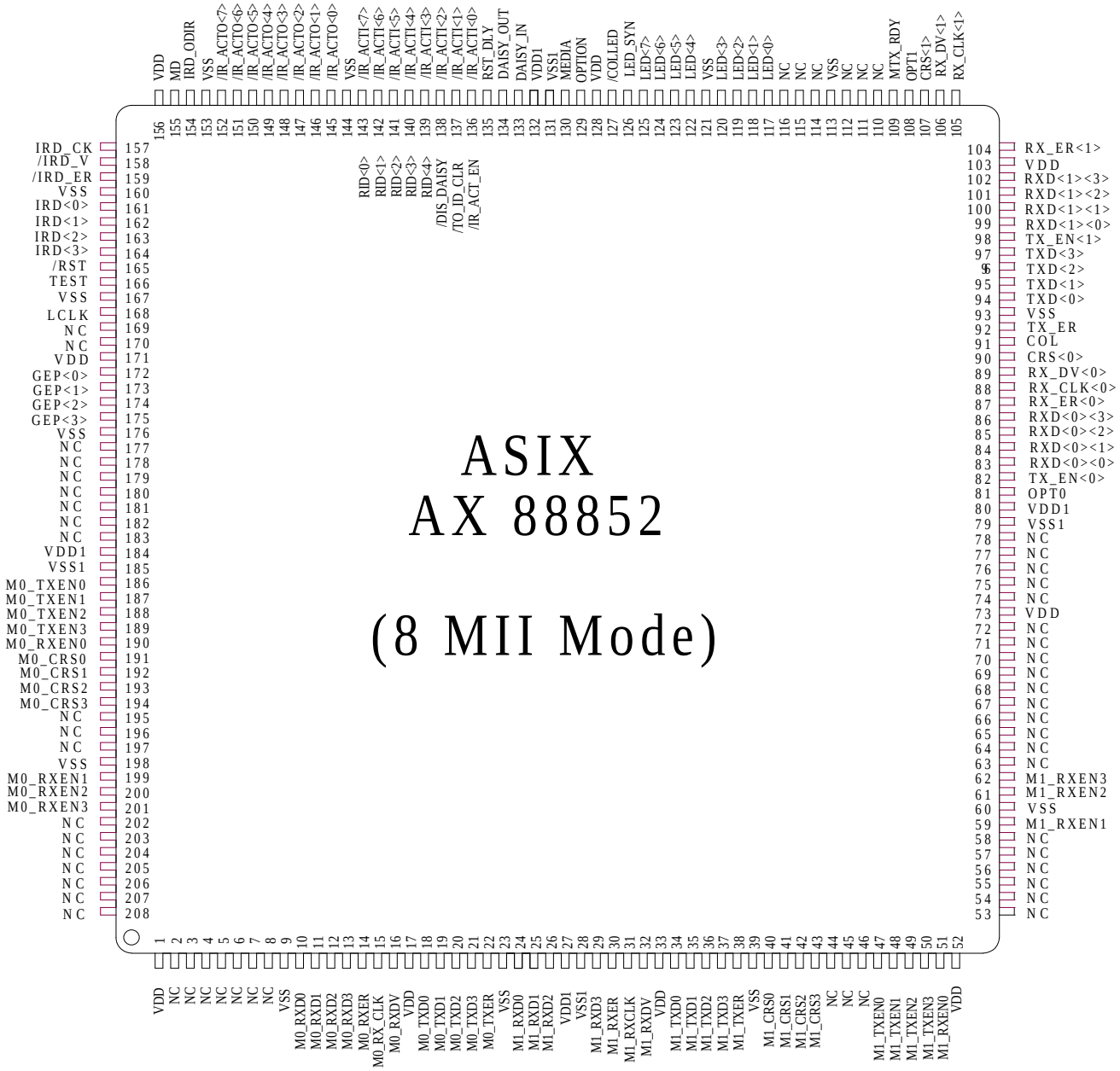


Fig - 4 Pin Connection Diagram for 8MII Mode

1.6 Pin Connection Diagram for AX88853 (8PCS + 2MII mode)

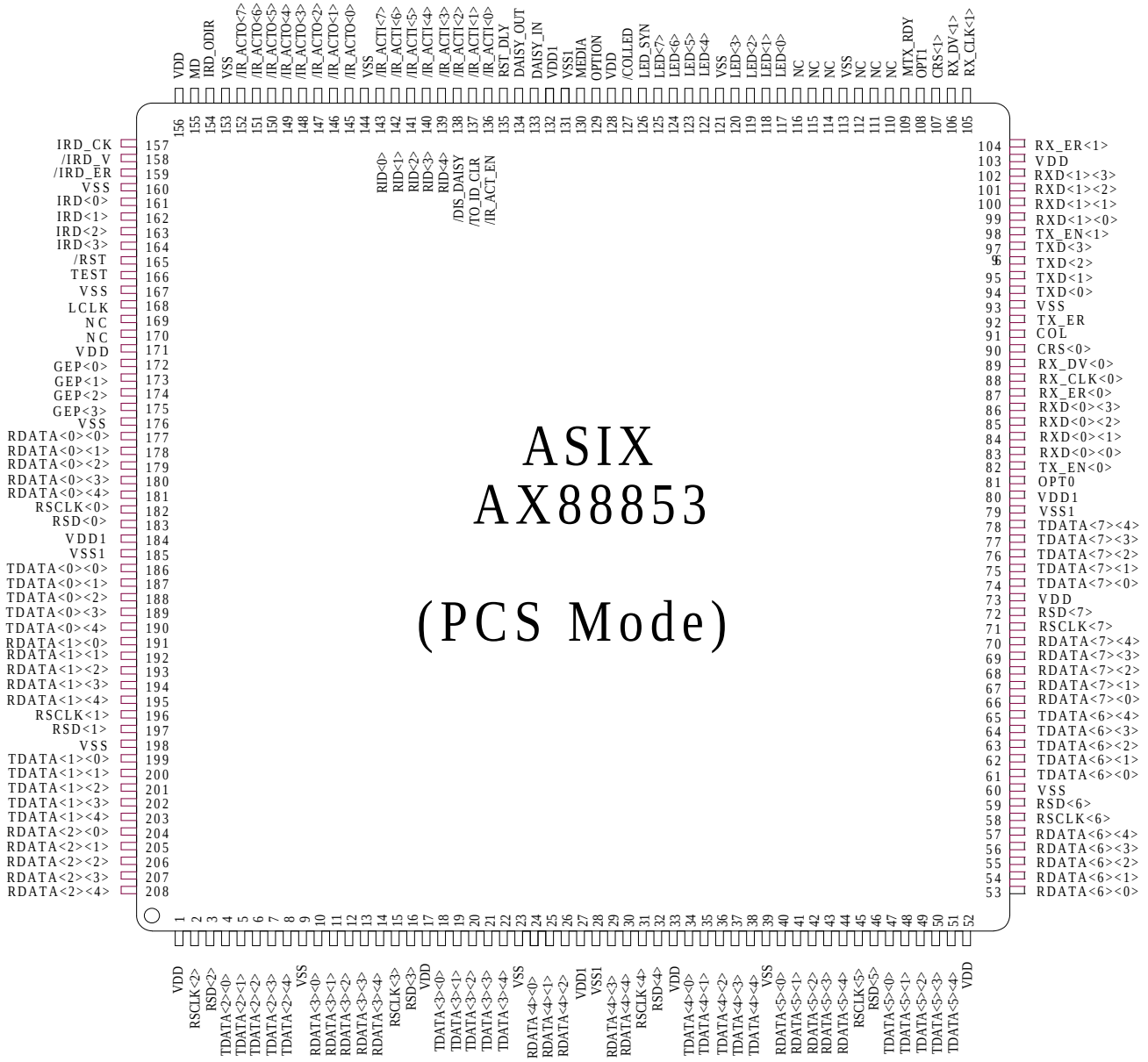


Fig - 5 Pin Connection Diagram for 8PCS Mode

1.7 Pin Connection Diagram for AX88854 (Management mode)

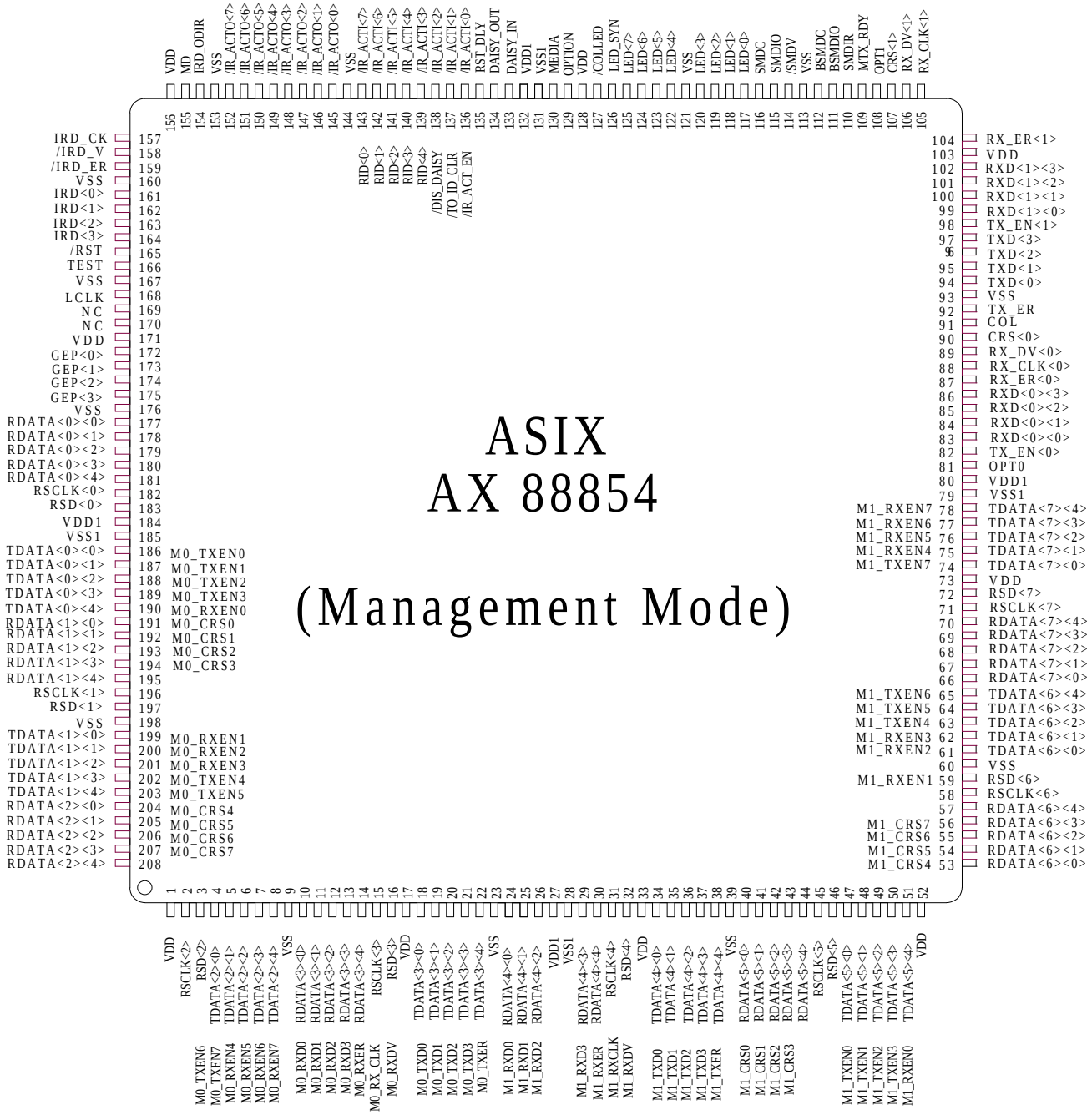


Fig - 6 Pin Connection Diagram for Management Mode

2.0 Pin Description

2.1A PCS interface

Signal Name	Type	Pin No.	Description
RDATA[0][4:0]	I/PU	181-177,	Receive Symbol Data : Data is input synchronously with the rising edge of
RDATA[1][4:0]	I/PD*	195-191	RSCLK
RDATA[2][4:0]	I/PD*	208-204	
RDATA[3][4:0]	I/PD*	14-10	
RDATA[4][4:0]	I/PD*	30,29,26-24	
RDATA[5][4:0]	I/PD*	44-40	
RDATA[6][4:0]	I/PD*	57-53	
RDATA[7][4:0]	I/PU	70-66	
RSCLK[0]	I	182	Receive Symbol Clock : This 25Mhz input signal is phase-locked to the
RSCLK[1]	I	196	incoming signal at PHY. RSCLK is used to clock in received data from the
RSCLK[2]	I	2	RDATA[4:0] data bus.
RSCLK[3]	I	15	
RSCLK[4]	I	31	
RSCLK[5]	I	45	
RSCLK[6]	I	58	
RSCLK[7]	I	71	
RSD[0]	I /PD	183	Receive Signal Detect : This asynchronous input signal indicates that the
RSD[1]	I/PD	197	receive signal is above the detection threshold and will be used for link test
RSD[2]	I/PD	3	state machine.
RSD[3]	I/PD	16	
RSD[4]	I/PD	32	
RSD[5]	I/PD	46	
RSD[6]	I/PD	59	
RSD[7]	I/PD	72	
TDATA[0][4:0]	O/L	190-186	Transmit Symbol Data : These signals are 4B/5B encoded transmit data
TDATA[1][4:0]	O/L	203-199	symbol, driven at the rising edge of local 25Mhz clock. LCLK
TDATA[2][4:0]	O/L	8-4	
TDATA[3][4:0]	O/H**	22-18	
TDATA[4][4:0]	O/H**	38-34	
TDATA[5][4:0]	O/L	51-47	
TDATA[6][4:0]	O/L	65-61	
TDATA[7][4:0]	O/L	78-74	

*** RDATA[1:6][4] are pull up.**

**** TDATA[3][4] and TDATA[4][4] drive capability are MH**

Note : "Type" has the following attributes

I : Input
O : Output
I/O : Bi-direction
PU : Pull Up
PD : Pull Down
H : Driving High Current 16mA
MH : Driving Middle High Current 12mA
ML : Driving Middle Low Current 8mA
L : Driving Low Current 4mA

2.1B MII interface (share bus MII group 0 port & MII group 1 port)
M0 -- MII group 0 ; M1 -- MII group 1

Signal Name	Type	Pin No.	Description
M0_TX_ER M1_TX_ER	O/ML O/ML	22 38	Transmit Error : TX_ER is transition synchronously with respect to the rising edge of TX_CLK . Asserted high when a code violation is request to be send
M0_TXD[3:0] M1_TXD[3:0]	O/H O/H	21-18 37-34	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.
M0_TX_EN[7:0] M1_TX_EN[7:0]	O/L O/L	4,3,203, 202, 189-186 74,65-63, 50-47	Transmit Enable : TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
M0_RXD[3:0] M1_RXD[3:0]	I/PU I/PU	13-10 29,26-24	Receive Data : RXD [3:0] is driven by the PHY synchronously with respect to RX_CLK.
M0_RX_ER M1_RX_ER	I/PD I/PD	14 30	Receive Error : RX_ER ,is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
M0_RX_CLK M1_RX_CLK	I I	15 31	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD [3:0] and RX_ER signals from the PHY to the MII port of the repeater.
M0_RX_DV M1_RX_DV	I/PD I/PD	16 32	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:1].
M0_CRS[7:0] M1_CRS[7:0]	I/PD I/PD	207-204, 194-191 56-53, 43-40	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle.
M0_RX_EN[7:0] M1_RX_EN[7:0]	O/L O/L	8-4, 201-199, 190 78-75, 62,61,59, 51	Receive Enable : Assert high to the respective PHY chip to enable its receive data.

2.2 MII interface (two individual MII ports)

Signal Name	Type	Pin No.	Description
TX_ER (share)	O/ML	92	Transmit Error : TX_ER is transition synchronously with respect to the rising edge of TX_CLK . Asserted high when a code violation is request to be send
TXD[3:0] (share)	O/ML	97-94	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TX_EN[0] TX_EN[1]	O/L O/L	82 98	Transmit Enable : TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
RXD[0][3:0] RXD[1][3:0]	I/PU I/PU	86-83 102-99	Receive Data : RXD [3:0] is driven by the PHY synchronously with respect to RX_CLK.
RX_ER[0] RX_ER[1]	I/PD I/PD	87 104	Receive Error : RX_ER ,is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
RX_CLK[0] RX_CLK[1]	I I	88 105	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD [3:0] and RX_ER signals from the PHY to the MII port of the repeater.
RX_DV[0] RX_DV[1]	I/PD I/PD	89 106	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:1].
CRS[0] CRS[1]	I/PD I/PD	90 107	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle.
COL (share)	O/ML	91	Collision Signal :This pin indicates collision(s) , that occurred at the collision domain of the hub, to MII interface devices. Both the MII port use this signal commonly.
OPT0 OPT1	I/PU I/PU	81 108	Option for external device type : Default ‘high’ is for PHY type device. Otherwise, ‘low’ for MAC type device.

2.3 Station Management Interface

Signal Name	Type	Pin No.	Description
SMDC	I	116	Station Management Data Clock : The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. MDC is limited to a maximum frequency of 2.5MHz.
SMDIO	I/O/L /PU	115	Station Management Data Input / Output : Serial data input/output transfers from/to the internal registers or PHYs . The transfer protocol conforms to the IEEE 802.3u MII specification.
/SMDV	I/PU	114	Station Management Data Valid : Asserted when a valid read/write command is present.
SMDIR	O/L	110	Station Management Data Direction : Direction signal for an external bi-directional buffer on the MDIO signal. 0 = MDIO data flows into the AX88850 1 = MDIO data flows out of the AX88850 Defaults to 0 when no register access is present.
BSMDC	O/L	112	Buffered Station Management Data Clock : Buffered MDC signal. Allow more devices to be chained on the MII serial bus.
BSMDIO	I/O/L /PU	111	Buffered Station Management Data Input /Output : Buffered MDIO signal. When the “PHY_access” bit in the CONFIG register is set High, the MDIO signal is passed through to BMDIO for accessing the physical device chips.

2.4 Management Information Base (MIB) Interface

Signal Name	Type	Pin No.	Description
MD	I/O/Z /MH /PU	155	Management Data : Outputs management information for the AX88856 MIB chip. This signal carries with RID_CH signal and port number of the in-coming packet and is synchronous to IRD_CK signal.
MTX_RDY	O/L	109	Repeated Packet Ready : Repeated packet data ready to copy to MIB chip indicator.

2.5 Expansion Bus Interface

Signal Name	Type	Pin No.	Description
IRD[3:0]	I/O/Z /MH /PU	164-161	INTER REPEATER DATA : Nibble data input/output. Transfer data from the "active" AX88850 to all other "inactive" AX88850s. The bus-master of the IRD bus is determined by IR_VECT bus arbitration.
/IRD_ER	I/O/Z /MH /PU	159	INTER REPEATER DATA ERROR: This signal reflect the RX_ER status of the active port across the inter repeater bus. Used to track receive errors from the PHY in real time.
/IRD_V	I/O/Z /MH /PU	158	INTER REPEATER DATA VALID : This signal reflect the RX_DV status of the active port across the inter repeater bus. Used to frame good packets.
IRD_CK	I/O/Z /MH	157	INTER REPEATER CLOCK VALID : All inter repeater signals are synchronized to the rising edge of this clock.
IRD_ODIR	O/L	154	INTER REPEATER DATA IN/OUT DIRECTION : This pin indicates the direction of data for external transceiver. "High" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Output. "Low" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Input.
/IR_ACTO [7:0]	I/O/OC /H	152-145	INTER REPEATER ACTIVITY IN/OUT: Then the local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as a output pin. All other pins serve as input pins but except the collision conditions. When collision occurred all of the signal of related (RID-1) pins will served as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1)=1.
/IR_ACTI[7:0] or	I/PU	143-136	INTER REPEATER ACTIVITY IN: These pins perform the same function as /IR_ACTO[7:0] when they serve as input function. Then the /IR_ACTO[7:0] insert external buffers the input function must be replaced with /IR_ACTI [7:0]. The /IR_ACTI[7:0] also serve as power-on configuration input:
RID[4:0] /IR_ACTI[4:0]	I/PU	140-136	Repeater Identification Number Parallel In RID[4:0]: When power on reset these pin as inputs to setup the repeater ID of the chip. RID[2:0] indicate the repeater ID from 0 to 7. RID[4:3] defines the group code in the cascade system and must keep difference with PHY ID address definition.
/DIS_DAISY /IR_ACTI[5]	I/PU	141	Disable RID Daisy-chain Input. No matter what kind of data input from DAISY_IN pin ,the repeater ID will never be changed from DAIST_IN.
/TO_ID_CLR /IR_ACTI[6]	I/PU	142	Time Out to Clear repeater ID : Within the time out period, if no daisy chain repeater ID input. The repeater ID will be clear to RID=0 . Otherwise, the repeater ID will remain the previous value (power on configured value , previous daisy chain reconfigured value or the configuration value written via station management port).The tome out period is about 4 to 5 second.
/IR_ACT_EN /IR_ACTI[7]	I/PU	143	/IR_ACTI[7:0] pins function is enable when IR_ACT_EN is pulled "low" when power on. Otherwise , it is disable.

2.6 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[7:0]</td><td>O/L</td><td>125-122,
120-117</td><td>LED Display Information : Those signals indicate each port‘s Partition, Jabber, Link/Activity, Utilization % (global), Collision % (global) in sequence. For detail , see the LED timing specification

The Utilization % display define as following :
Group0 [U4 :U0]
<table>
<tr><th>Utilization %</th><th>LED4</th><th>LED3</th><th>LED2</th><th>LED1</th><th>LED0</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>5</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>15</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>30</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Group1 [UU4 :UU0]
<table>
<tr><th>Utilization %</th><th>LED4</th><th>LED3</th><th>LED2</th><th>LED1</th><th>LED0</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>10</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>20</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>40</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>80</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
The Collision % display define as following :
Group0 [C4 :C0]
<table>
<tr><th>Collision %</th><th>LED4</th><th>LED3</th><th>LED2</th><th>LED1</th><th>LED0</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>10</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Group1 [CC4 :CC0]
<table>
<tr><th>Collision %</th><th>LED4</th><th>LED3</th><th>LED2</th><th>LED1</th><th>LED0</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>20</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>30</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>LED_SYN</td><td>O/L</td><td>126</td><td>LED status synchronous signal : The signal is a LED_CK period width signal and repeated every 16 cycle. When high indicate the next cycle on the LED[7:0] bus show the Partition status of port 8 to 0 respectively.</td></tr>
<tr><td>/COLLED</td><td>O/MH</td><td>127</td><td>Collision LED Display : When Collision occur, the signal will be “LOW” about 52.4 ms.</td></tr>
</table>

2.7 Miscellaneous

Signal Name	Type	Pin No.	Description
LCLK or TX_CLK	I	168	Local Clock : Must be run at 25Mhz . Used for transmit data to PHY devices,
/RST	I	165	Reset : The chip is reset when this signal is asserted Low.
RST_DLY	O/L	135	Reset Delay : The signal is active high when reset and delay /RST signal about 2 LCLK cycle. It is useful for power on configuration setup control of /IR_ACTI[7:0].
DAISY_IN	I/PU	133	Repeater Identification Number Daisy-Chain In : This pin is a daisy chain serial input for Repeater ID. A state machine always monitor the input if a correct data (RID) present at the pin, the (RID+1) will be written to RID register and override the power on setup RID for the chip.
DAISY_OUT	O/L	134	Repeater Identification Number Daisy-Chain Out : This pin is periodically shift out the RID of itself to the next chained chip to inform that this ID has already been occupied. The RID is shift out periodically every about 200us.
TEST	I/PD	166	Test Pin : The pin is just for test mode setting purpose only. Must be pull low when normal operation. When in test mode , GEP pins will be force to test input signals.
GEP[3:0]	I/O/L /PU	175-172	General Purpose I/O Pins : Those pins just for system application usage. I.e. for output control or input status report. When reset the default function is for inputs.
MEDIA	I/PD	130	Media selection : External pull-down for AX88853 with 4.7K ohm resister. External pull-up for AX88851, AX88852 and AX88854 with 4.7K ohm resister.
OPTION	I/PU	129	Option : Option for repeater state machine. User must pull this pin up.
VDD	I	1,17,27, 33,52,73, 80,103, 128,132, 156,171, 184	POWER : +5V +/-5%
VSS	I	9,23,28, 39,60,79, 93,113, 121,131, 144,153, 160,167, 176,185, 198	POWER: 0V

3.0 Functional Description

3.1 PCS interface logic

The PCS logic performs PCS / MII receiving / transmitting interface. When it receives, first deciphers the signals from RDATA<4:0>, then do symbol alignment after detecting /J/K/ codes, then data is aligned to do 5B/4B decoding. When it transmits, first do 4B/5B encoding to convert MII signals to PCS signals, then enciphers and send to TDATA<4:0>.

When RSD is high from low, then link fail counter will count for 330u sec, then the port can receive packet normally. During 330u sec that link fail counter counts, then receiving packet will be ignored. Cipher / No-cipher is selected by station management access logic.

3.2 Carrier Integrity Monitor State Machine (AX88853 PCS mode only)

For 100BASE-X systems, it is necessary that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cable disconnects, and faulty wiring.

The AX88853 support CIM state machine with self-interrupt capability to prevent a segment's spurious carrier activity from reaching the repeater unit and hence propagating through the network.

3.3 Repeater State Machine

The repeater state machine is used to control repeater behavior, generates right signal in corresponding states. The repeater state machine is in Idle state when there is no carrier **.** When there is carrier , the repeater state machine goes to Data Forwarding State to ensure correct data forwarding. If collision happens anytime, The repeater state machine detects collision then send jam pattern until collision ceases.

idle State

The idle state happens when these conditions exists:

a. /RST is low.
b. Reset emitted by station management access logic(RST_RSM).
c. There is no any carrier in M0_CRS[7:0], M1_CRS[7:0], and CRS{1:0] in MII mode. Or receive IDLE code in PCS mode. If in cascade application, repeater receive no inter repeater active signal.

In this state,M0_RXEN[7:0],M1_RXEN[7:0],M0_TXEN[7:0],M1_TXEN[7:0] are all low in MII mode.

Data Forwarding State

When there is only one carrier in M0_CRS[7:0], M1_CRS[7:0]or CRS[0], CRS[1] in MII mode, or only one of eight ports receives /J/K/ codes in PCS mode ,or only one of IR_ACTO[7:0] become low, The repeater state machine stores receiving packet and transmits to all other ports. Exception for

a. The port is jabbered.
b. The port is partitioned.
c. There exists collision.

In this state, only one of M0_RXEN[7:0] and M1_RXEN[7:0] is high, or M0_RXEN[7:0] or M1_RXEN[7:0] are all low because either packet is from two dedicated MII port or from inter-repeater cascade interface in MII mode.

The repeater send packet from receiving port to all ports exclusive of the receiving that is M0_TXEN[7:0] and M1_TXEN[7:0] all becomes high, and one may be low if that port is the receiving port in MII mode. The repeater forwards data to TDATA[7:0] except for the receiving RDATA port in PCS mode.

Collision State

The Collision State happens when these conditions exists:

a. There are two or more signals high among M0_CRS[7:0],M1_CRS[7:0],CRS[1:0]. Or receive collision messages from /IR_ACTO[7:0] in MII mode.
b. At least two ports of PCS ports receive /J/K/ code group or receive collision message from /IR_ACTO[7:0] in PCS mode.
c. Only one carrier exists but RXDV still low exceeds 5 clock cycles. The repeater sends collision pattern to all ports, that is, M0_TXEN[7:0] and M1_TXEN[7:0] all become high during collision state.

3.4 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration(64K bit times for AX88850), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber function will be clear and re-enable reception and transmission.

3.5 Partition State Machine

The partition state machine is used to protect network from be upset by a port suffering continuous collision, each port uses a partition state machine to detect and prevent this condition. When a port is suffering from continuous 32 or 64 times of collisions by CCLimits. Then it goes to Partition State. The port entering Partition State will be released until a packet without collision more than 512 bit times or after power-on reset.

Partition function is enabled by default, and CCLimits is 64 by default. Enable/Disable partition function (DIS_PART) and option of CCLimits to be 64 or 32 (COL_LIMIT32) are selected by station management access logic.

3.6 Expansion Logic(Cascade Interface)

The expansion logic is used to stack numerous repeaters. The expansion logic can be divided into two types:

Expansion Logic with Buffer (maximum mode

In this mode, use /IR_ACTO[7:0] and /IR_ACTI[7:0] to cascade repeaters. Buffers are used both in /IR_ACTO[7:0] and /IR_ACTI[7:0]. This mode is supposed to cascade repeaters on difference boards via cables. There is a configuration bit /IR_ACT_EN to decide cascade signals are judges by /IR_ACTI[7:0](/IR_ACT_EN = 0) or /IR_ACTO[7:0](/IR_ACT_EN = 1).

Expansion Logic without Buffer (minimum mode)

In this mode, use /IR_ACTO[7:0] to cascade repeaters. Just connect /IR_ACTO[7:0] without using buffer in this part. This mode is supposed to cascade repeaters on the same board.

/IR_ACTO<7:0>			
RPTR_ID<2:0>	Idle	Active	Collision
0	FFh	FEh	FBh
1	FFh	FDh	FCh
2	FFh	FBh	F9h
3	FFh	F7h	F3h
4	FFh	EFh	E7h
5	FFh	DFh	CFh
6	FFh	BFh	9Fh
7	FFh	7Fh	3Fh

In this table:

a. All /IR_ACTO[7:0] will be in open-drain state when repeater chip is idle. These signals are all high via external pull high resister.
b. One signal of /IR_ACTO[7:0] is low in data forwarding state corresponding to different RPTR_ID[2:0].
c. Two signals of /IR_ACTO[7:0] are low in collision state corresponding to different RPTR_ID[2:0].

3.7 Management Logic

AX88850 provides the required management information associated with a packet for management chip which statistics processed on a per packet basis. Transmit ready signal TX_RDY is used as a framing signal for management data MD. Then management chip uses this data to determine the source of the current packet. MD data is synchronized to the rising edge of IRD_CK. When collision occur, MD will be tri-state and becomes invalid.

MD frame format

idle	start bit	data0	data1	data2	data3	data4	data5	data6
1	0	PID[0]	PID[1]	PID[2]	PID[3]	PID[4]	RID_CH	PARITY

Notes:

a. PID[4:0] is the number of the receiving port.
b. RID_CH indicates change in RID.
c. PARITY = 1 when sum of 1‘s among PID[4:0] and RID_CH is even
PARITY = xnor (PID[4],PID[3],PID[2],PID[1],PID[0],RID_CH)

3.8 Management Counters

There are four management counters in each port. These 16-bit-wide management counters keep track of the following events:

Collision Event Counter
It indicates the number of times that collision occurrences on a port.
Partition Event Counter
It indicates the number of times that a port has been partition.
Short Event Counter
It indicates the number of packets that is shorter than 76 BT.
Late Event Counter
It indicates the number of collision occurrences time after 512 BT when carrier presents.
Fault Carrier Event Counter (AX88853 only)
It indicates the number of times that fault carrier occurrences on a port.

These counters can be read out by MIB serial access interface and will be clear after read operation.

3.9 Station Management Access Interface

The AX88850 provides 128 registers held in 4 pages of 32(Page 0 ~ 3 Register).These registers are 16 bits wide. Only one register of one page can be access at the same time through the MII serial management bus. After power on reset, Page 0 Register is the default setting. Change the value of PAGE REGISTER which exists in all pages, then switches to any page. For example: Page 3 Register can be accessed by writing 03h to the PAGE REGISTER. AX88850 can thus be managed through SMDC and SMDIO pins. The SMDC clock with maximum 2.5M Hz is used to sample data train on SMDIO. The interface follows the serial management protocol defined by IEEE 802.3u clause 22.

Management frame format

	PREAM	START	OPCODE	DEV_AD	REG_AD	TA	DATA	IDLE
READ	1.....1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1.....1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

For the protocol to work, all serial data must be “synchronized” to incoming data. To ensure data locked, a preamble of 32 consecutive 1‘s present before the start code, then the receive logic know the beginning of the data frame.

With the setting of PHY_ACCESS = 1(stored in CONFIGURATION REGISTER), the target access device may be physical layer devices. In this mode, SMDIO is gated to BSMDIO. SMDIO and BSMDIO must turn on in the appropriate direction for read/write access. In the cascade system, only one repeater chip has the set of PHY_ACCESS at a time to avoid contention problems.

3.10 RID Receive-Transmit Interface(Daisy Chain Logic)

In the cascade system, repeater ID of each chip will be re-arranged by serial in/out daisy chain logic. The DAISY_IN pin always monitor RID of the previous chained chip, and the value of (RID+1) will override the original RID of the current chip. Then the DAISY_OUT pin will periodically (about 200us) send out the exact RID of current chip to inform the next chained chip. By this way, each repeater chip in 8 AX88850 hub (maximum application) will keep unique ID of itself. The RID is used in inter repeater bus arbitration and uniquely identify station management accesses.

Note that only RID[2:0] can be changed and RID[4:3] must be the same value for all repeaters in the cascade system. In this way, repeater ID won‘t be confused with PHY device ID during station management access.

DAISY_IN/OUT frame format

idle	start bit	data0	data1	data2	data3
1	0	RID[0]	RID[1]	RID[2]	PARITY

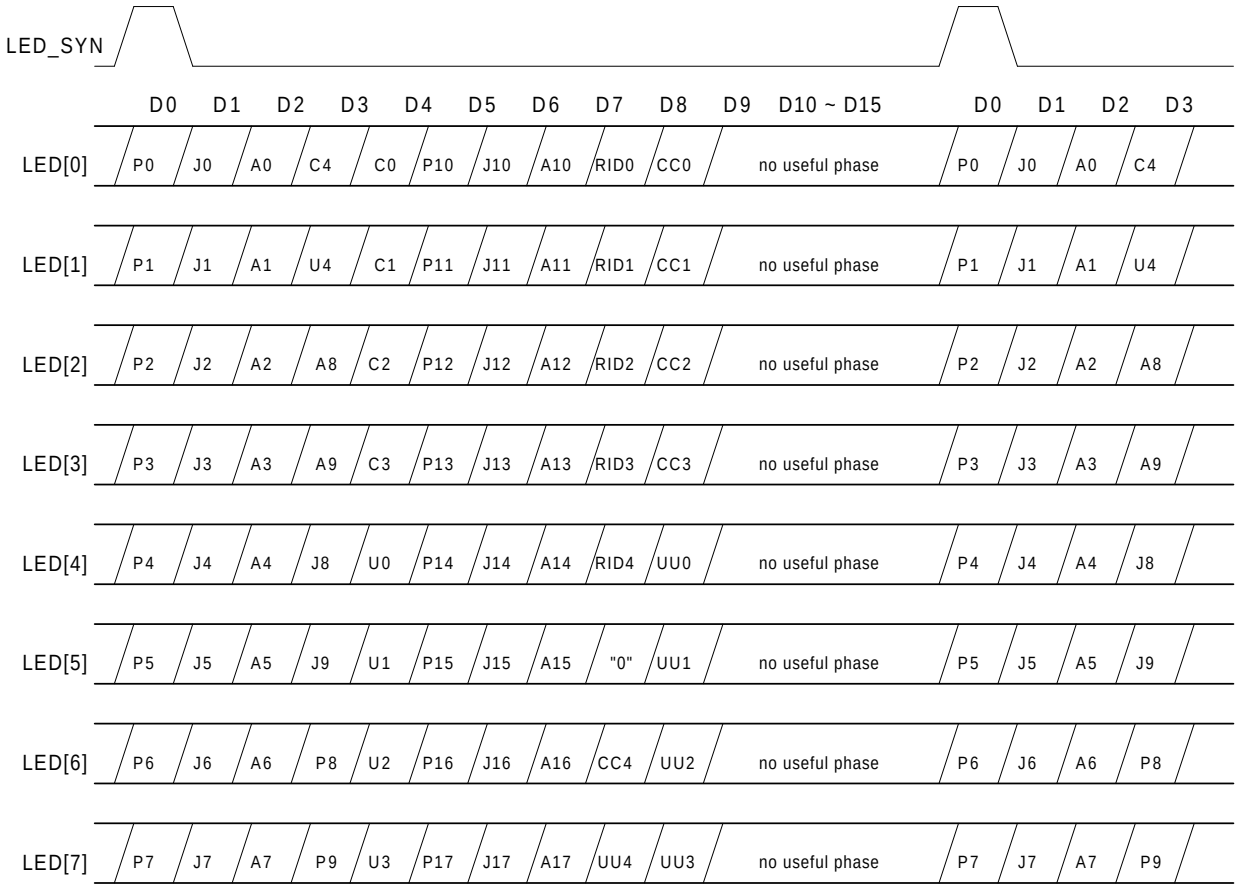
Notes: PARITY = 1 when sum of 1‘s in RID[2:0] is even

There are two flag : /DIS_DAISY and /TO_ID_CLR which control daisy-chain access. If disable daisy-chain input (/DIS_DAISY = 0), the RID of current chip can‘t be override and don‘t care the present data on DAISY_IN. If no daisy-chain input, the RID of current chip can be clear to 0 during time out period with the setting of /TO_ID_CLR = 0. The timer is done about 4sec.

3.11 LED Interface

AX88850 provides per-port LED status indication for partition, jabber, link/activity and support rate-based LED for global utilization (%) and global collision frequency (%). Detail function is described on previous pin description (LED interface). LED[7:0] are all active low.

3.11.1 LED Status Driver wave-form for AX88851



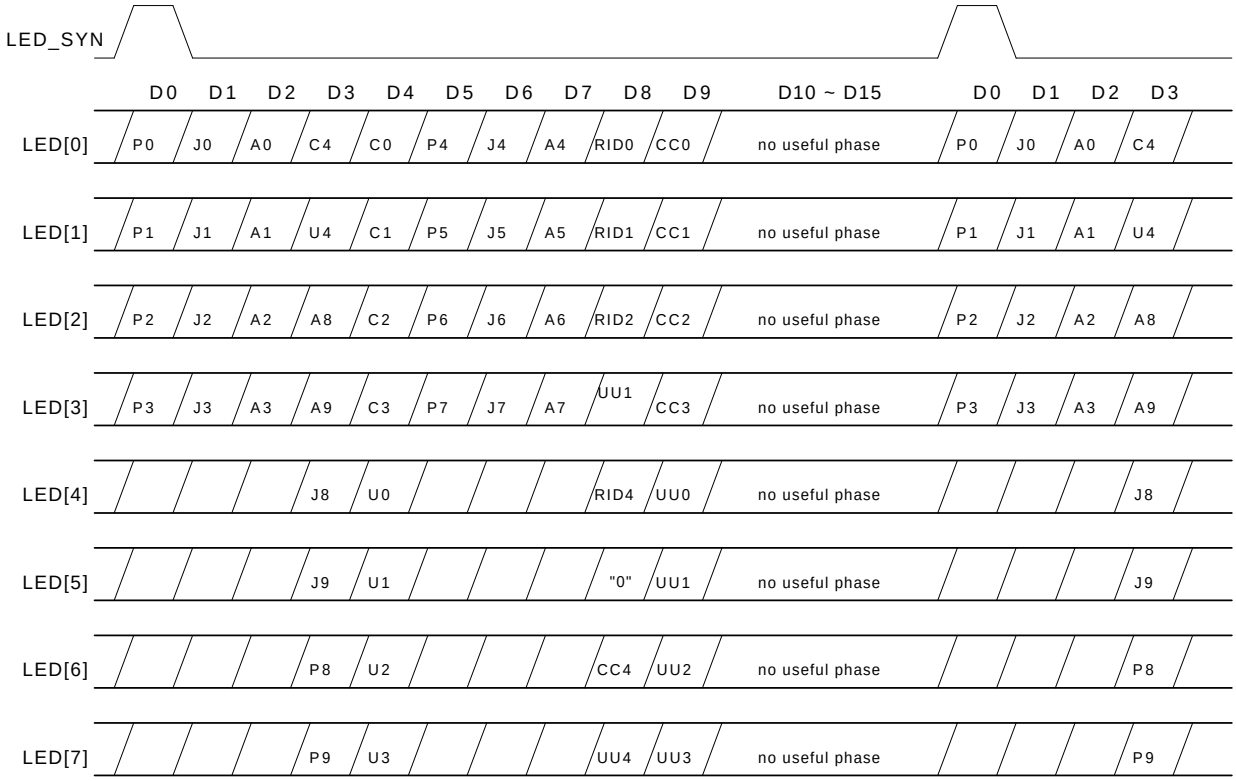
Note 1 :

a. P17~0 indicates partition status for each port
b. J17~0 indicates jabber status for each port
c. L17~0 indicates link status for each port
d. A17~0 indicates activity status for each port
e. RID4~0 is the ID number of repeater chip
f. The LED display support two estimations:C4~0 and CC4~0 which indicate global collision rate for each 104.8ms sampling period. Users can choose any one presentation.
g. The LED display support two estimations:U4~0 and UU4~0 which indicate global utilization rate for each 104.8ms sampling period. Users can choose any one presentation.

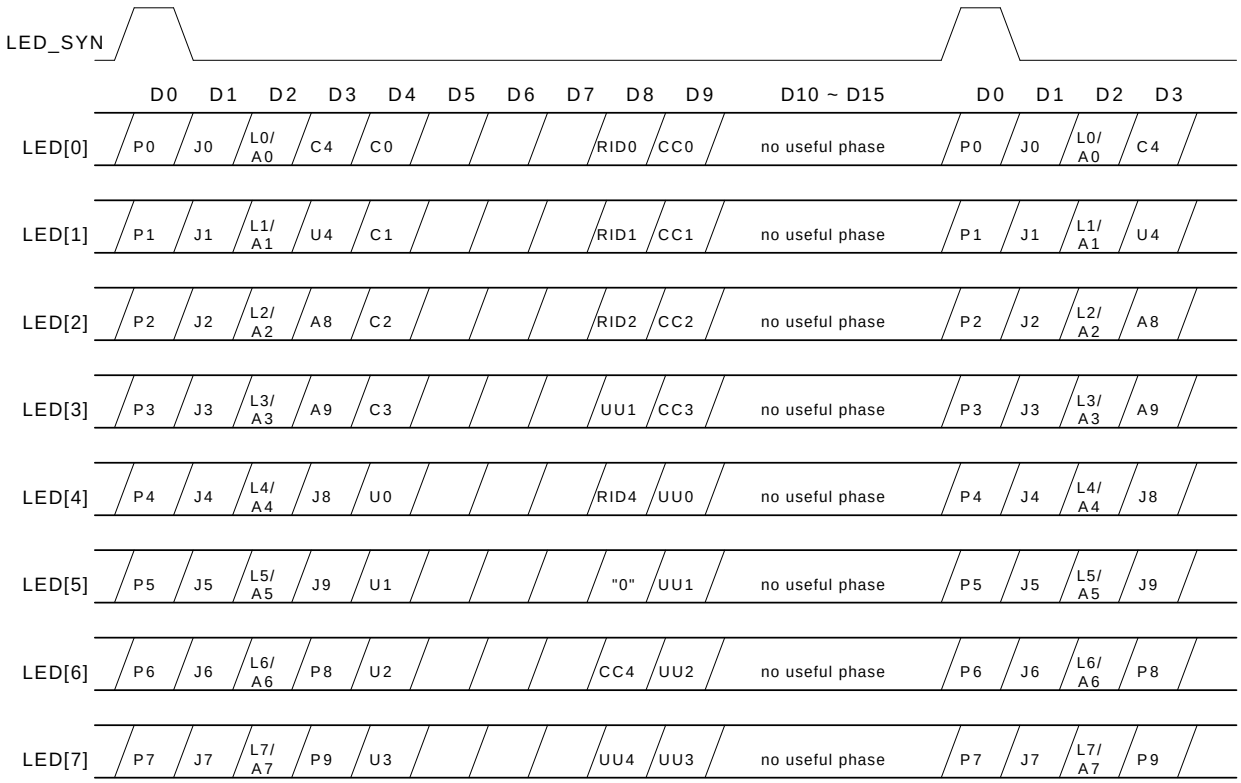
Note 2 : Reference port map as following table (Using per port Carrier Sense / Receive Signal Detect to identify port number).

AX88851	Port[7:0] == M0_CRS[7:0]	Port[9:8] == CRS[1:0]	Port[17:10] == M1_CRS[7:0]
AX88852	Port[3:0] == M0_CRS[3:0]	Port[9:8] == CRS[1:0]	Port[7:4] == M1_CRS[3:0]
AX88853	Port[7:0] == RSD[7:0]	Port[9:8] == CRS[1:0]	
AX88854	Reference to AX88851/AX88853 depended on MEDIA setting.		

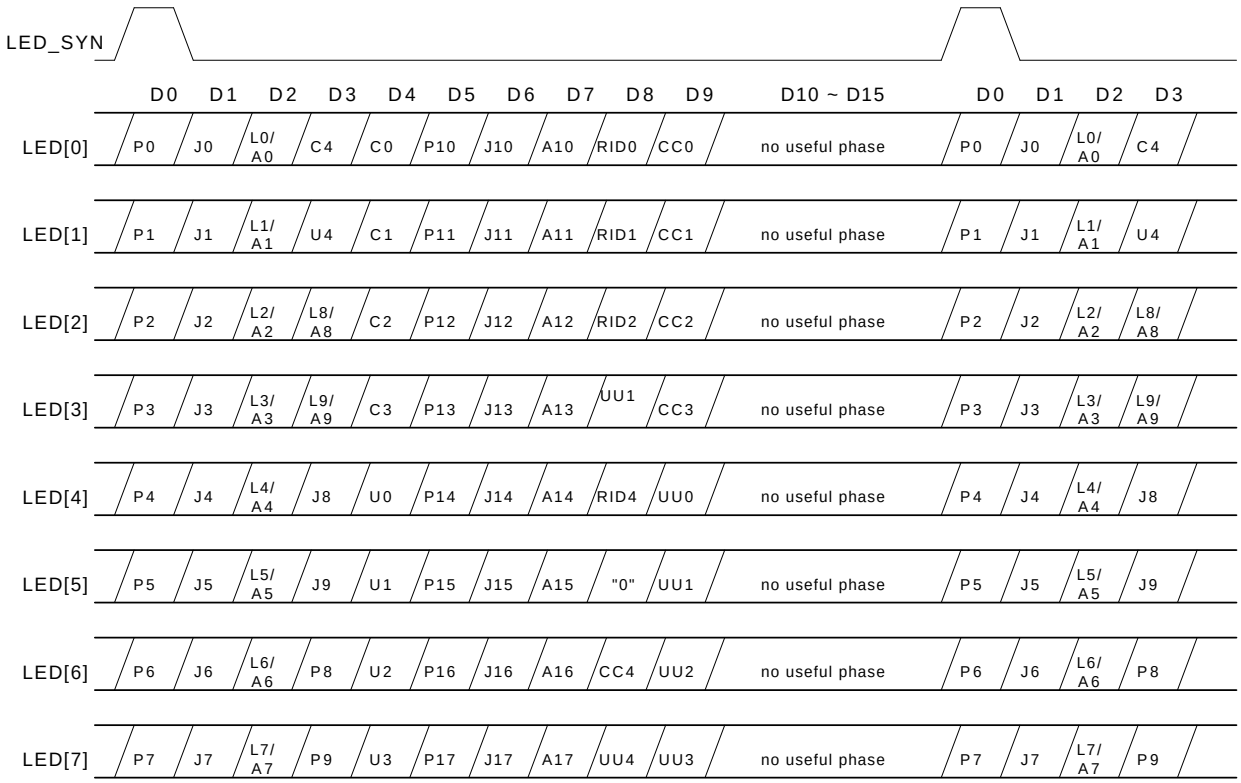
3.11.2 LED Status Driver wave-form for AX88852



3.11.3 LED Status Driver wave-form for AX88853



3.11.4 LED Status Driver wave-form for AX88854



3.12 Power on Configuration(Initial Setting)

During power-on reset, /IR_ACTI[[7:0] are used as some configuration setting. These include inter repeater active input pin enable/disable (/IR_ACT_EN); time out to clear repeater ID(/TO_ID_CLR); daisy-chain input disable/enable (/DIS_DAISY); and repeater ID(RPTR_ID[4:0]). Detail function is described on previous pin description (expansion bus interface). After reset, these setting are stored in DEVICE ID REGISTER which can be modified by station management write commands.

Default setting	Function
/IR_ACT_EN pull high	DISABLE inter repeater active in
/TO_ID_CLR pull high	DISABLE time out to clear repeater ID
/DIS_DAISY pull high	ENABLE daisy-chain input
RPTR_ID pull high	RPTR_ID = 11111

4.0 REGISTERS

The AX88850 has 128 16-bit registers which are separated into four pages with each page 32 words. At power-on or reset , the default value is page 0 registers. The register page can be changed by writing to the register address 1 on all the four pages .

4.1 Page 0 Register MAP

Address (hex)	Name	Access	Description
0	CONFIG	R/W	Set AX88850 configuration
1	PAGE	R/W	Selects register from page 0 to page 3.
2	PARTITION	RO	Indicates Auto-Partitioning status.(port0 - port9)
3	JABBER	RO	Indicates Jabber status. (port0 - port9)
4	ADMIN	R/W	Port enable / disable, administration control/status(port0 - port9)
5	DEVICE-ID	R/W	Accesses 1) the AX88850 ID number configured externally on the RID[4:0] pins. 2) the last receiving port number. The device number of AX88850 may be overwritten after it has been latched at the end of reset.
6			Reserved
7			Reserved
8	P8-SE	R/W	Port 8 : 16-bit ShortEvent Counter (dedicated MII port 0)
9	P8-LE	R/W	Port 8 : 16-bit LateEvent Counter
A	P8-COL	R/W	Port 8 : 16-bit Collision Counter
B	P8-PART	R/W	Port 8 : 16-bit Auto-partition Counter
C	P9-SE	R/W	Port 9 : 16-bit ShortEvent Counter (dedicated MII port 1)
D	P9-LE	R/W	Port 9 : 16-bit LateEvent Counter
E	P9-COL	R/W	Port 9 : 16-bit Collision Counter
F	P9-PART	R/W	Port 9 : 16-bit Auto-partition Counter
10-13	P0-SE … P0-PART	R/W	Port 0 management counters (as per ports 8,9 as above)
14-17	P1-SE … P1-PART	R/W	Port 1 management counters (as per ports 8,9 as above)
18-1B	P2-SE … P2-PART	R/W	Port 2 management counters (as per ports 8,9 as above)
1C-1F	P3-SE … P3-PART	R/W	Port 3 management counters (as per ports 8,9 as above)

4.2 Page 1 Register MAP

Address (hex)	Name	Access	Description
0	CONFIG	R/W	Set AX88850 configuration (same as page 0)
1	PAGE	R/W	Selects register from page 0 to page 3. (same as page 1)
2	PARTITION	RO	Indicates Auto-Partitioning status.(port10 - port17)
3	JABBER	RO	Indicates Jabber status. (port10 - port17)
4	ADMIN	R/W	Port enable / disable, administration control/status(port10 - port17)
5	SI_REV	RO	Silicon revision code.
6-7			Reserved
8-F	P0-FCRS … P7-FCRS	R/W	Port 0 false carrier counters (address 8) to Port 7 false carrier counters (address F) Those counters are valid just for PCS mode port 0 to port 7. As for MII mode , the false carrier counter will be available on PHY, but some PHY chip manufacturer not support those functions.
10-13	P4-SE … P4-PART	R/W	Port 4 management counters (as per ports 8,9 as above)
14-17	P5-SE … P5-PART	R/W	Port 5 management counters (as per ports 8,9 as above)
18-1B	P6-SE … P6-PART	R/W	Port 6 management counters (as per ports 8,9 as above)
1C-1F	P7-SE … P7-PART	R/W	Port 7 management counters (as per ports 8,9 as above)

4.3 Page 2 Register MAP

Address (hex)	Name	Access	Description
0	CONFIG	R/W	Set AX88850 configuration
1	PAGE	R/W	Selects register from page 0 to page 3.
2-F			Reserved
10-13	P10-SE … P10-PART	R/W	Port 10 management counters (as per ports 8,9 as above)
14-17	P11-SE … P11-PART	R/W	Port 11 management counters (as per ports 8,9 as above)
18-1B	P12-SE … P12-PART	R/W	Port 12 management counters (as per ports 8,9 as above)
1C-1F	P13-SE … P13-PART	R/W	Port 13 management counters (as per ports 8,9 as above)

4.4 Page 3 Register MAP

Address (hex)	Name	Access	Description
0	CONFIG	R/W	Set AX88850 configuration (same as page 0)
1	PAGE	R/W	Selects register from page 0 to page 3.. (same as page 1)
2-F			Reserved
10-13	P14-SE … P14-PART	R/W	Port 14 management counters (as per ports 8,9 as above)
14-17	P15-SE … P15-PART	R/W	Port 15 management counters (as per ports 8,9 as above)
18-1B	P16-SE … P16-PART	R/W	Port 16 management counters (as per ports 8,9 as above)
1C-1F	P17-SE … P17-PART	R/W	Port 17 management counters (as per ports 8,9 as above)

4.5 Configuration Register (CONFIG)

Page 0 to Page 3 Address 0h

Bit	Bit Name	Access	Bit Description
D15-D8	Reserved		Written as "0" for future compatibility concern. Undefined by read.
D7	RST_FLAG	RO	Reset Flag : The bit is set when power on reset and is clear after read CONFIG register.
D6	RID_CH	RO	Repeater ID Changed : The bit is set when Daisy-Chain RID input override the current RID or after power on reset. When read CONFIG register will clear the bit.
D5	DIS_CIPHER	R/W	Disable Cipher Function : Then set the bit at PCS mode, the 5bit symbol scramble and descrambler function are disable. Default is enable.
D4	MGTEN	R/W	Management Enable : This bit enable all the management counters. 0 : Management Counters disabled. (default) 1 : Management Counters enabled.
D3	COL_LIMIT32	R/W	Collision limit : This bit configures the collision limit for Auto-Partitioning. 0 : Consecutive Collision limit set to 64 (default). A port will be partitioned on the 65th consecutive collision. 1 : Consecutive Collision limit set to 32 . A port will be partitioned on the 33rd consecutive collision.
D2	DIS_PART	R/W	Disable Auto-Partition : Set this bit disable the Auto-Partition algorithm. 0 : Auto-Partition is not disabled (default) 1 : Auto-Partition is disabled .
D1	PHY_ACCESS	R/W	PHY access enable : This bit enable to access PHY register via MII serial protocol. 0 : PHY access disabled (default) 1 : PHY access enabled .
D0	RST_RSM	R/W	Reset Repeater State Machines : Setting the bit holds the RSM in reset. The management event flags and counters are unaffected by this bit. Setting this bit while a reception is in progress may truncate the packet. 0 : AX88850 in normal operation (default) 1 : AX88850 held in reset .

4.6 Page Register (PAGE)

Page 0 to Page 3 Address 1h

Bit	Bit Name	Access	Bit Description
D15-D8	GEP[3:0]	R/W	D11-D8 : GEP I/O control. Default = 0h for input mode. Otherwise, =1h, enable output. D15-D12 : GEP Data . Default = 0h. When write, D15-D12 value present to GEP[3:0] if enabled. When read, D15-D12 reflect the GEP[3:0] value.
D7-D2	Reserved		Written as "0" for future compatibility concern. undefined by read.
D1-D0	PAGE[1:0]	R/W	Those bits setting the register page to be accessed. PAGE[1:0] PAGE 0h 0 (default) 1h 1 2h 2 3h 3

4.7 Partition Status Register (PARTITION)

Page 0 Address 2h

Bit	Bit Name	Access	Bit Description
D15-D10	Reserved		undefined when read.
D9-D0	PART[9: 0]	RO	The respective port's PART bit is set to "1" when Partitioning is sensed on that port. After reset, these bits are cleared to "0".

Page 1 Address 2h

Bit	Bit Name	Access	Bit Description
D15-D8	Reserved		undefined when read.
D7-D0	PART[17: 10]	RO	The respective port's PART bit is set to "1" when Partitioning is sensed on that port. After reset, these bits are cleared to "0".

4.8 Jabber Status Register (JABBER)

Page 0 Address 3h

Bit	Bit Name	Access	Bit Description
D15-D10	Reserved		undefined when read.
D9-D0	JAB[9: 0]	RO	The respective port's JAB bit is set to "1" when Jabber condition is detected on that port. After reset, these bits are cleared to "0".

Page 1 Address 3h

Bit	Bit Name	Access	Bit Description
D15-D8	Reserved		undefined when read.
D7-D0	JAB[17: 10]	RO	The respective port's JAB bit is set to "1" when Jabber condition is detected on that port. After reset, these bits are cleared to "0".

4.9 Administration Register (ADMIN)

Page 0 Address 4h

Bit	Bit Name	Access	Bit Description
D15-D10	Reserved		Written as "0" for future compatibility concern. undefined by read.
D9-D0	ADMIN[9: 0]	R/W	Administration Disable : Setting these bits to "0" enable the respective port (TX and RX). Writing a 1 to any bit will disable that port. After reset, these bits default to "0" (all ports enable). Note that port enable/disable action will occur at the next network idle period.

Page 1 Address 4h

Bit	Bit Name	Access	Bit Description
D15-D8	Reserved		Written as "0" for future compatibility concern. undefined by read.
D7-D0	ADMIN[17: 10]	R/W	Administration Disable : Setting these bits to "0" enable the respective port (TX and RX). Writing a 1 to any bit will disable that port. After reset, these bits default to "0" (all ports enable). Note that port enable/disable action will occur at the next network idle period.

4.10 Device ID Register (DEVICEID)

Page 0 Address 5h

Bit	Bit Name	Access	Bit Description
D15-D13	Temp	R/W	Temporary Registers : reserved for system programer used.
D12-D8	PORT_NUM	*R/W	Port Number : These bit indicate the last or current receiving port number.
D7	/IR_ACT_EN	*R/W	Inter Repeater Active Input Pin Enable : This bit active low to enable /IR_ACTI[7:0] pin as inter-repeater carrier sense detection input. Otherwise, /IR_ACTI[7:0] pins is disable and only perform power-on configuration inputs.
D6	/TO_ID_CLR	R/W	Time Out to Clear repeater ID : Within the time out period, if no daisy chain repeater ID input. The repeater ID will be clear to RID=0 . Otherwise, the repeater ID will remain the previous value (power on configured value or previous daisy chain reconfigured value).The tome out period is about 4 to 5 second.
D5	/DIS_DAISY	R/W	Disable RID Daisy-chain Input: No matter what kind of data input from DAISY_IN pin the RPTR_ID can't be override.
D4-D0	RPTR_ID	R/W	Repeater ID : At the rising edge of /RST , the value of RID[4:0] are latched in this register as D[4:0]. The setting of RID[2:0]can be override according to the data from serial daisy-chain DAISY_IN pin input except /DIS_DAISY is configured to "low" . Note that in system application, the maximum of 8 devices can be cascade. Therefore only RID[2:0] can be variation and the RID[4:3] must be keep the same value in the same system and avoid conflicted with PHY device ID.

* Note : Host can't override these signals.

4.11 Silicon Revision Register

Page 1 Address 5h

Bit	Bit Name	Access	Bit Description
D15-D0	SI_REV[15:0]	RO	Silicon Reversion : Currently reads all 1's

4.12 Port Management Counter Registers

Each of the 18 ports of the AX88850 has a set of 4 event counters whose values can be read or pre-set (written) through the Port Management Counter Registers. When PCS (symbol) mode is selected, there is a set of false carrier counter / per port build-in on the chip. As for MII mode , the false carrier counter will be available on PHY, note that some PHY chip manufacturer not support those functions.

4.12.1 Short Event Counter Registers

Per port (“n” =port number) counters that indicate the number of Carrier Events that were active for less than the ShortEventMaxTime, which is defined as between 74 and 82 (76 nominal) bit times.

Bit	Bit Name	Access	Bit Description
D15-D0	P“n”_SE[15:0]	R/W	P“n”_SE[15:0]

4.12.2 Late Event Counter Registers

Per port (“n”= port number) counters that indicate the number of collision that occurred after the LateEventThreshold, , which is defined as between 480 and 565 (512 nominal) bit times. Both the Late Event and collisions will be incremented when this event occurs.

Bit	Bit Name	Access	Bit Description
D15-D0	P“n”_LE[15:0]	R/W	P“n”_LE[15:0]

4.12.3 Collision Counter Registers

Per port (“n”= port number) counters that indicate the number of collisions (COL asserted) .

Bit	Bit Name	Access	Bit Description
D15-D0	P“n”_CO[15:0]	R/W	P“n”_CO[15:0]

4.12.4 Auto-Partition Counter Registers

Per port (“n”= port number) counters that indicate the number of times the port was auto-partitioned.

Bit	Bit Name	Access	Bit Description
D15-D0	P“n”_PART[15:0]	R/W	P“n”_PART[15:0]

4.12.5 False Carrier Counter Registers

Per port (“n”= port number) counters that indicate the number of times the port was false carrier occurred. Those counters are valid just for PCS mode port 0 to port 7. As for MII mode , the false carrier counter will be available on PHY, but some PHY chip manufacturer not support those functions.

Bit	Bit Name	Access	Bit Description
D15-D0	P“n”_FCRS[15:0]	R/W	P“n”_FCRS[15:0]

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.5	+7	V
Input Voltage	Vin	Vss-0.5	Vdd+0.5	V
Output Voltage	Vout	Vss-0.5	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+250	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+4.75	+5.25	V

5.3 DC Characteristics

(Vdd=4.75V to 5.25V, Vss=0V, Ta=0°C to 70°C)

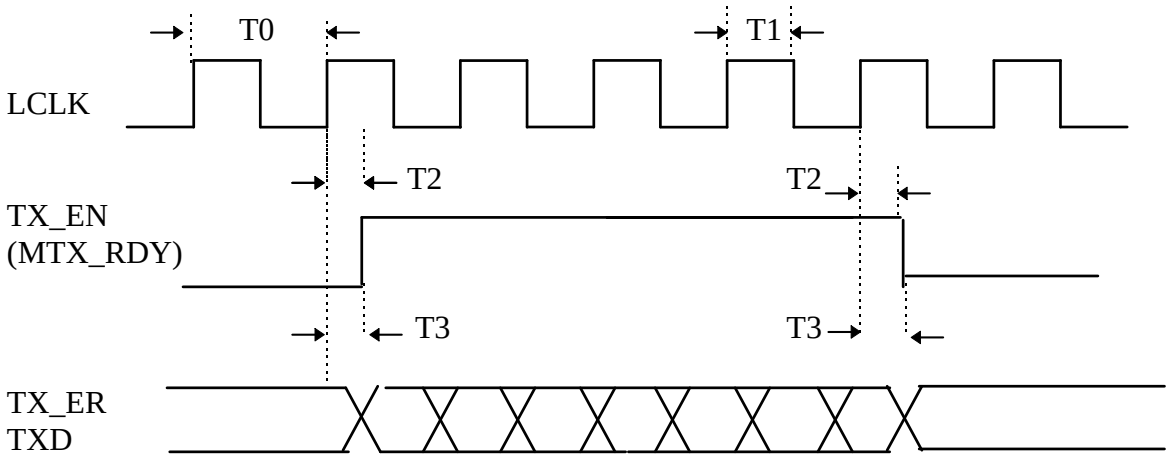
Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.5	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

Note :

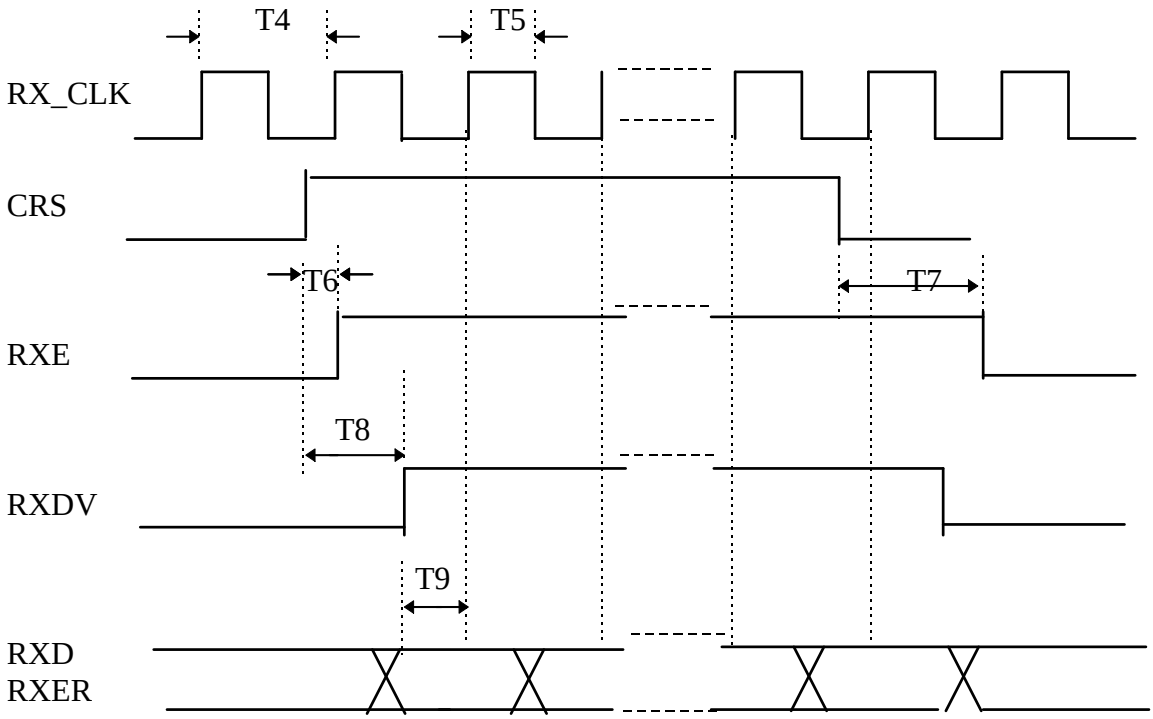
1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

5.4 AC specifications

5.4.1 MII Interface Timing Tx & Rx

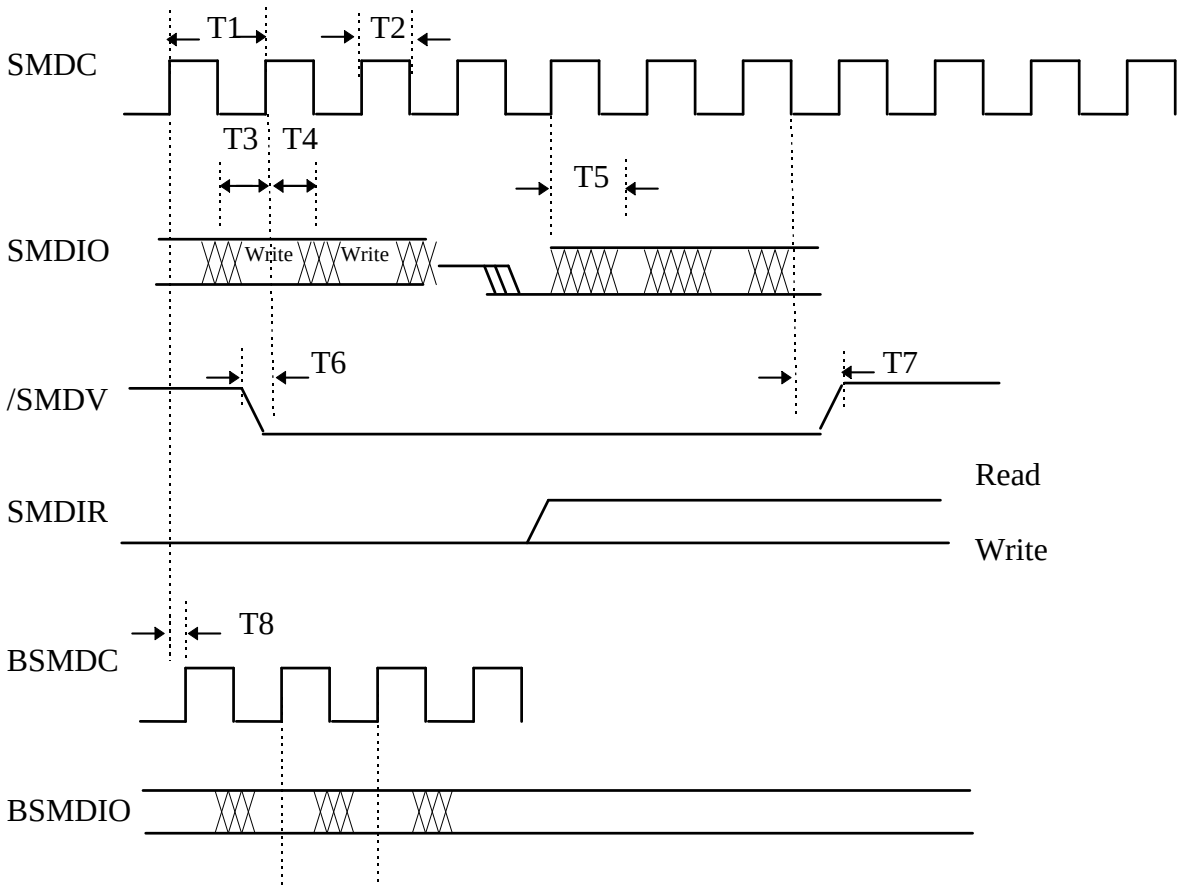


Symbol	Description	Min	Typ.	Max	Units
T0	Local Clock Cycle Time	39.996	40	40.004	ns
T1	Local Clock High Time	14	20	26	ns
T2	TX_EN or MTX_RDY Delay from LCLK High	4	14	19	ns
T3	TX_ER or TXD Delay from LCLK High	4	14	19	ns



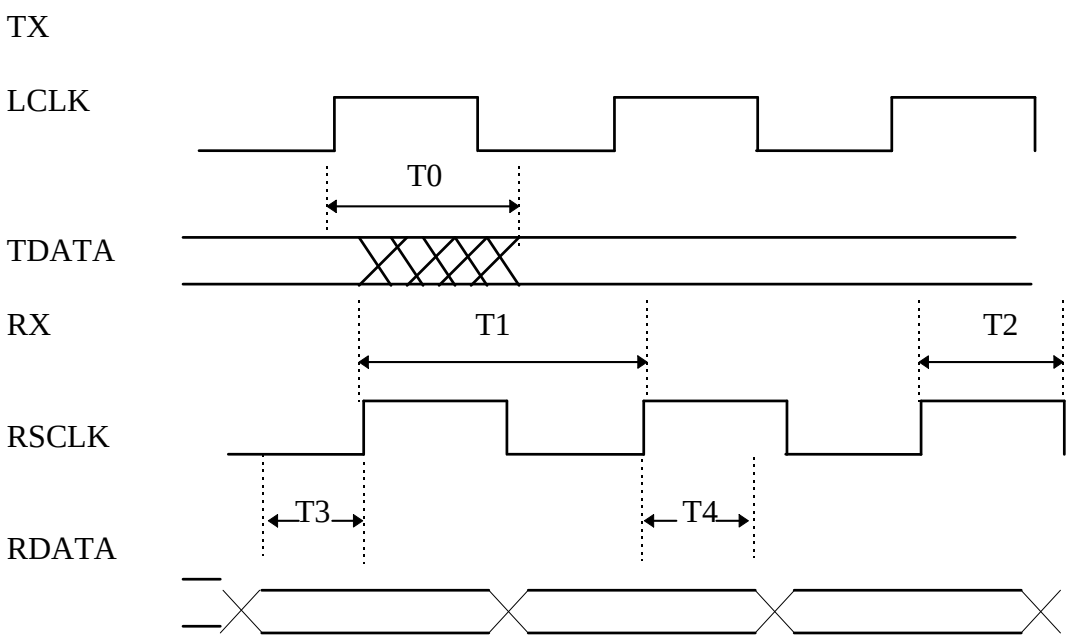
Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXE Assertion Delay			20	ns
T7	CRS to RXE De-assertion Delay	120		200	ns
T8	CRS to RXDV Delay Requirement	40		160	ns
T9	RXD or RXDV setup to RX_CLK rise time	10		-	ns

5.4.2 Station Management



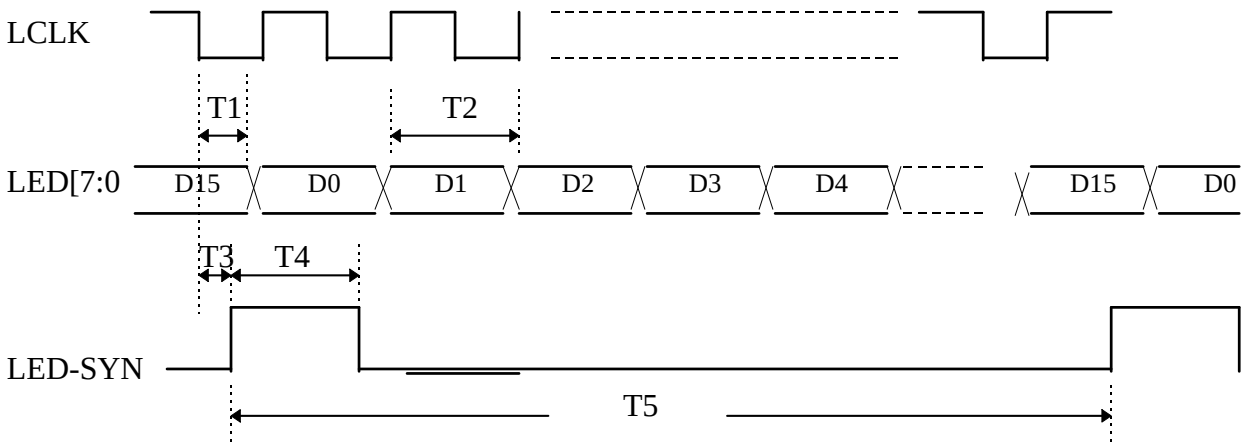
Symbol	Description	Min	Typ.	Max	Units
T1	SMDC Period	400		-	ns
T2	SMDC High Time	40		-	ns
T3	SMDIO Setup Time to SMDC High(Write)	10		-	ns
T4	SMDIO Hold Time to SMDC High(Write)	10		-	ns
T5	SMDIO Valid from SMDC High(Read)			50	ns
T6	/SMDV Setup Time to SMDC High	10		-	ns
T7	/SMDV Hold Time to SMDC High	10		-	ns
T8	BSMDIO Buffer Delay Time			20	ns

5.4.3 PCS Interface Timing



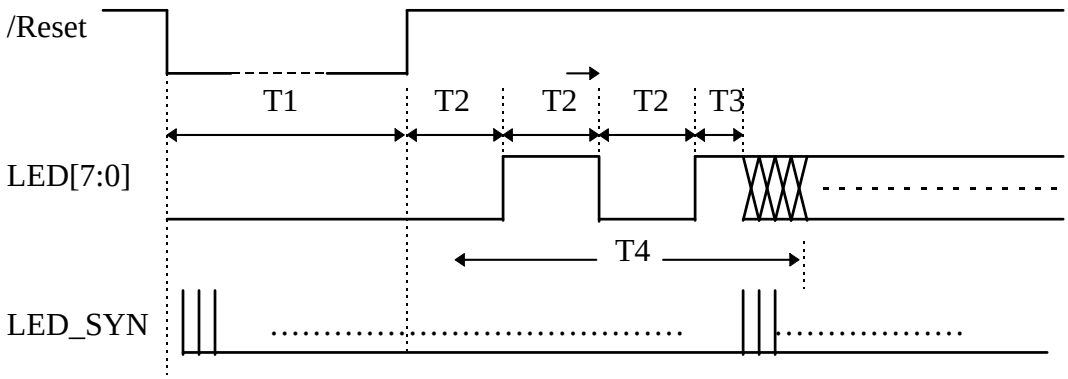
Symbol	Description	Min	Typ.	Max	Units
T0	TDATA Valid From LCLK High	12		35	ns
T1	RSCLK Clock Cycle Time	39.996	40	40.004	ns
T2	RSCLK Clock High Time	14	20	26	ns
T3	RDATA Setup Time	13		-	ns
T4	RDATA Hold Time	10		-	ns

5.4.4 LED DISPLAY



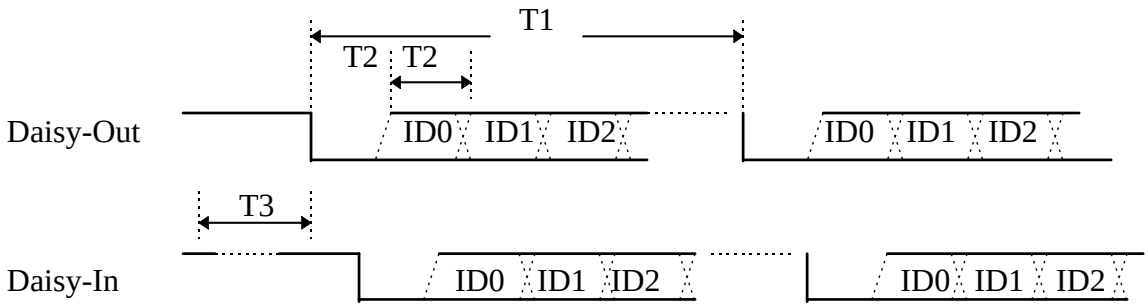
Symbol	Description	Min	Typ.	Max	Units
T1	LED Valid from LCLK Low	7		24	ns
T2	LED Data Width		40		ns
T3	LED_SYN Valid from LCLK Low	6		13	ns
T4	LED-SYN Pulse Width		40		ns
T5	LED-SYN Cycle Time		640		ns

5.4.5 LED Display After Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

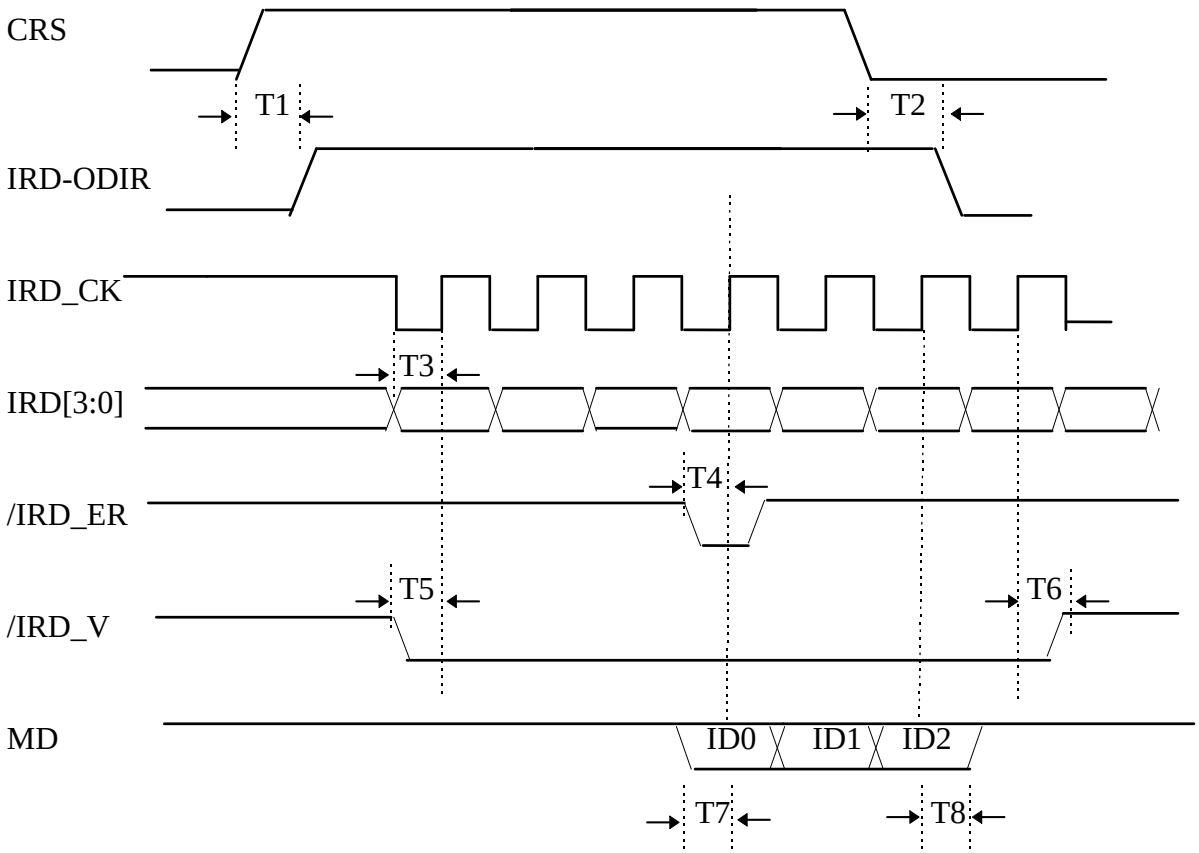
5.4.6 Repeater ID Daisy Chain



Symbol	Description	Min	Typ.	Max	Units
T1	Daisy Chain One Burst period		204.8		us
T2	Start Bit Period or Data Width		12.8		us
T3	Daisy Chain Data In Time-out *		3.8		s

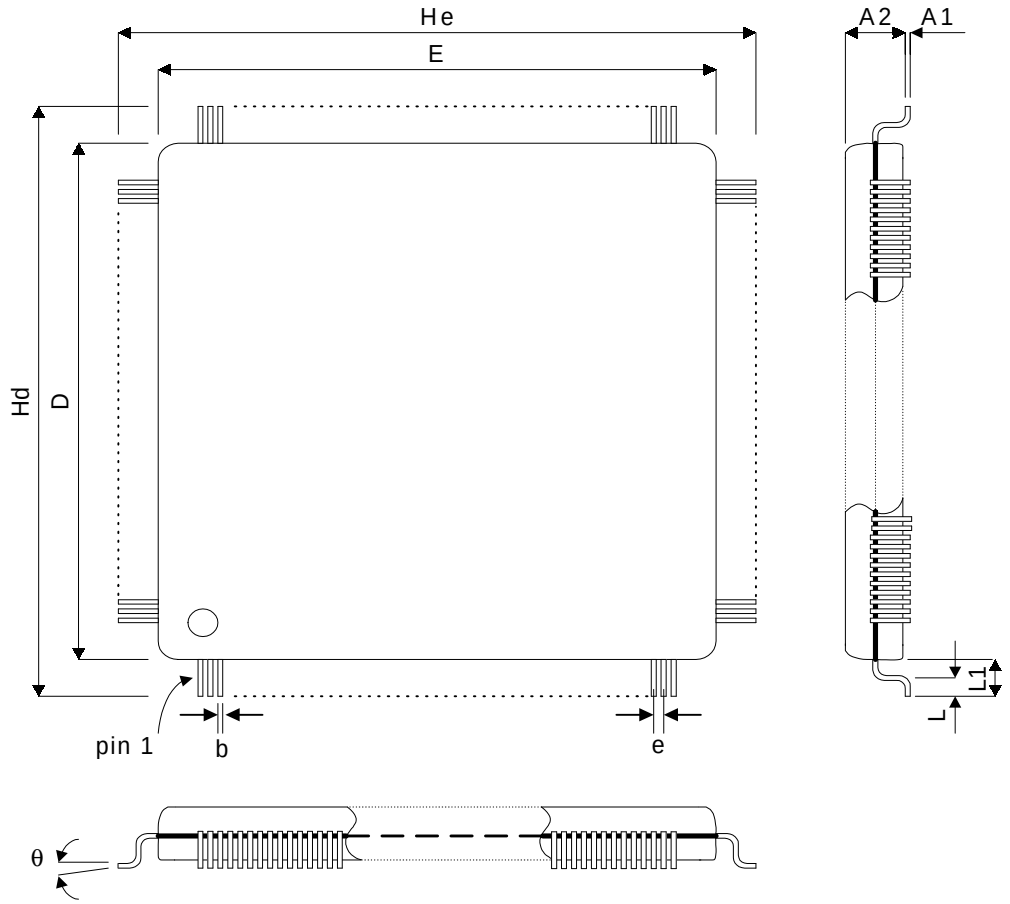
Note : Daisy-Chain Data-In Time-out stands for no input data (always high level) for the specific time.

5.4.7 Expansion Bus



Symbol	Description	Min	Max	Units
T1	CRS Assertion to IRD-ODIR Assertion	-	42	ns
T2	CRS De-Assertion to IRD-ODIR De-Assertion	160	240	ns
T3	IRD[3:0] Setup Time to IRD-CK High	10	-	ns
T4	/IRD_ER Setup Time to IRD-CK High	10	-	ns
T5	/IRD_V Setup Time to IRD-CK High	5	-	ns
T6	/IRD_V Hold Time from IRD-CK High	5	-	ns
T7	MD Setup Time to IRD-CK High	3	13	ns
T8	MD Hold Time from IRD-CK High	3	13	ns

6.0 PACKAGE INFORMATION



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.25	0.5
A2	3.17	3.32	3.47
b	0.10	0.20	0.30
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e		0.50	
Hd	30.35	30.60	30.85
He	30.35	30.60	30.85
L	0.45	0.60	0.75
L1		1.30	
θ	0		10