AX99100
PCIe to Multi I/O Controller

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Features

PCI Express

- Single-lane (X1) PCI Express End-point Controller with PHY integrated
- Compliant with PCI Express 2.0 Gen 1
- Compliant with PCI Express card specifications
- Compliant with PCI Power Management 1.2
- Supports four PCI Express functions
- Supports both legacy and MSI Interrupts
- Supports ASPM Power Management

Serial Port Interface

- Dual or Quad UARTs
- Supports RS-232/RS-422/RS-485 multiprotocol
- Bi-directional speeds up to 25 Mbps per port
- Full Serial Modem Control
- Supports Hardware, Software Flow Control
- Supports 5, 6, 7, 8 and 9-bit Serial format
- Supports Even, Odd, None, Space and Mark parity
- Supports Custom baud rate by internal PLL or external clock
- Supports On Chip 256 Byte depth FIFOs in Transmit, Receive path of each Serial Port
- Supports remote wakeup and power management features
- Serial Port transceiver shutdown support
- Supports Slow IrDA mode (up to 115200bps) on all Serial Ports
- Supports multi-drop application for 9-bit mode
- Supports DMA burst transfer

Parallel Port

- Compatible with IEEE 1284 – SPP/Byte/ECP Mode

SPI Master Interface

- Programmable SPI clock frequency up to 42MHz
- Supports Mode 0, Mode 1, Mode 2 and Mode 3 timing modes
- Supports MSB/LSB first transfer fashion
- Programmable peripheral chip select, selecting up to 7 SPI devices
- Supports Non-Burst-Type transfer up to 8 bytes and/or Burst-Type transfer via DMA mode for high performance
- Supports to fragment large data block into several smaller transfers on SPI bus to reduce software loading
- Supports programmable transfer 0 ~ 8 bytes OP-Code field in each transfer automatically to reduce software loading
- Supports wakeup by SWAKEn pin from Slave

Local Bus Interface

- Supports memory or I/O access through PCIe BAR0/1 to local bus interface, each BAR mapping to local bus' chip select (CS0n and CS1n)
- Supports direct access and bus master access (auto-increment and fixed address)
- Supports 8-bit or 16-bit data bus width (little and big endian bus swap)
- Supports up to 2 Kbytes address space and 2 chip select outputs when separated address/data bus style
- Supports up to 64 Kbytes address space and 2 chip select outputs when multiplexed address/data bus style
- Supports programmable local chip select region
- Supports “Slave Request based DMA” access for interfacing with external device with bus master
- Supports clock out, CLKO, up to 62.5MHz
- Supports asynchronous or synchronous Local Bus with required clock output, CLKO
- Supports programmable bus access cycles, self-terminated bus access cycles and back-to-back turnaround cycles
- Supports programmable RSTO, ALE, RDY, DREQ0/1, DACK0/1, CLKO polarity, and INT0/1 level/edge trigger
- Supports wakeup by INT0/1 and DREQ0/1 pins

- Supports I^2C Master Interface
- Up to 24 bi-directional GPIO lines including 8 dedicated GPIO and 16 multi-function GPIO
- Integrates on-chip power-on reset circuit
- On Chip 3.3 to 1.2V Regulator
- 68-pin QFN RoHS compliant package
- Operating temperature range: 0 to 70℃ or -40 to +85℃

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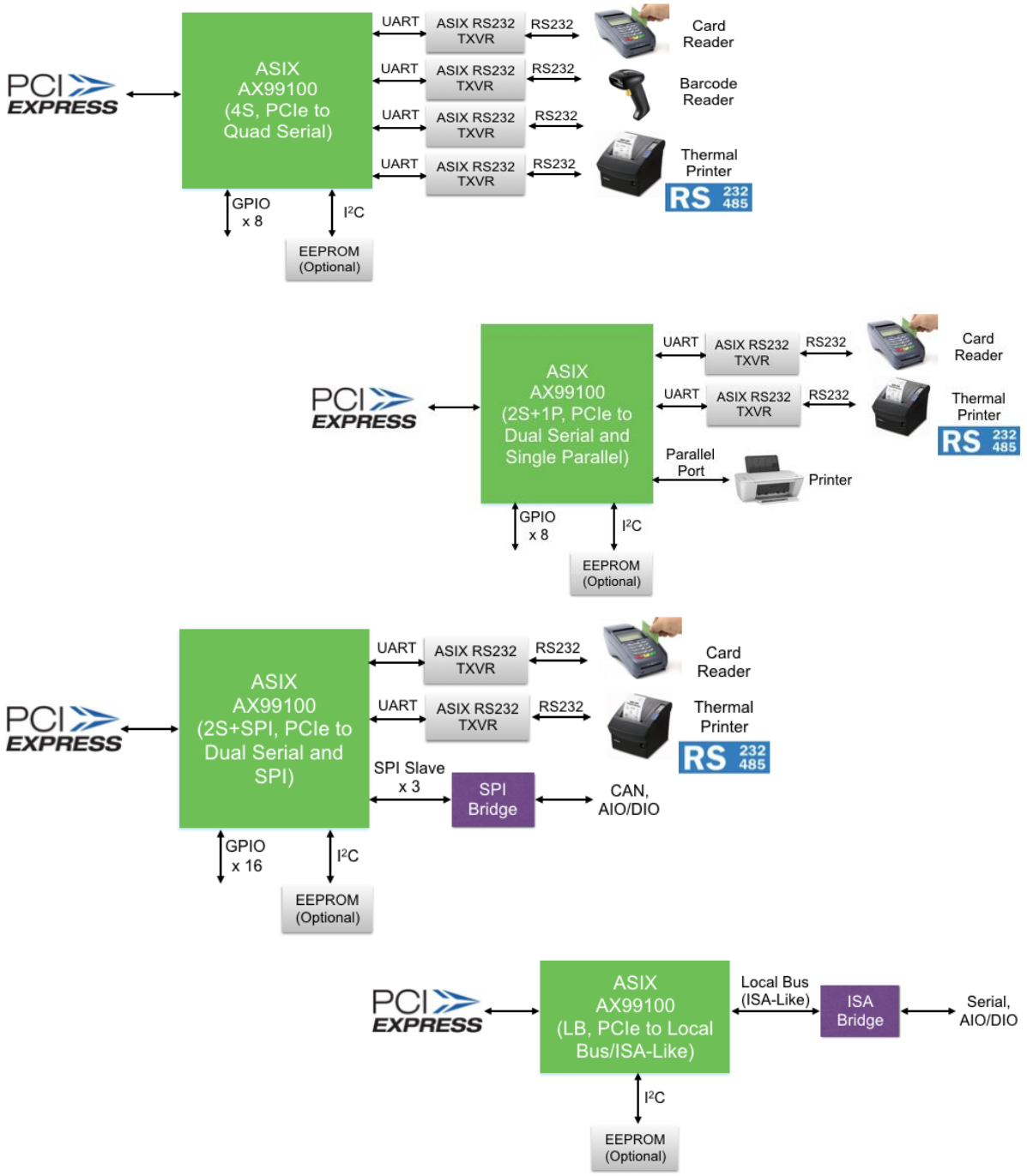
Product Description

The AX99100 is a single chip solution that fully integrates PCIe 2.0 Gen 1 end-point controller and SerDes with a variety of peripherals such as four High Speed Serial Ports, one Parallel Port, I^2C Master, High Speed SPI, Local Bus (ISA-Like), and GPIOs. It consists of four main configurations such as 4S (PCIe to Quad Serial), 2S+1P (PCIe to Dual Serial and Single Parallel), 2S+SPI (PCIe to Dual Serial and SPI), and LB (PCIe to Local Bus/ISA-Like) for different kinds of applications.

The AX99100, in 68-pin QFN, are available with RoHS compliant package and supports commercial grade operating temperature range from 0 to 70℃ and industrial grade from -40 to 85℃.

Target Applications



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1 Introduction

1.1 General Description

AX99100, PCI Express to Multi-I/O Controller, is a single chip solution for PCI express-based high performance Serial, Parallel port, SPI and Local Bus connectivity. It provides rich features and highly configurability for variety products.

AX99100 is a fully integrated, single-lane PCI express end-point controller and SerDes with rich high performance peripherals such as four High Speed Serial Ports, one Parallel Port, I^2C Master, one High Speed SPI and Local Bus interface. AX99100 also provides rich GPIO ports can be controlled by software driver for some automation control applications.

The High Speed Serial Ports with the throughput up to 25Mbps, it can works with RS-232/RS-422/RS-485 multi-protocol transceivers and allow easy reconfigured Full/Half-duplex, Loopback and Termination resistors by software. The Parallel Port is compatible with IEEE 1284 and supports SPP, Nibble, Byte and ECP modes. An I^2C interface is provided to configure AX99100 device options through an external EEPROM after chip reset and also supports to access other I^2C device. SPI master provides a full-duplex, synchronous serial communication interface (4 wires) to flexibly work with numerous SPI peripheral devices. Local Bus interface provides configurable asynchronous or synchronous, 8 or 16 bits data bus width with specified endian type and address/data multiplexed or separated bus type access mode to support variety slave interface access types. All the GPIO pins are programmable and can be used as Input or Output. AX99100 supports 8 dedicated GPIO and every serial port pins can be configured as GPIO by software.

Generally, the clock source of AX99100 is from PCIe slot. AX99100 don't need any other clock source for the main operations. But AX99100 still supports a clock input from external oscillator for those special baud rate generated for UART, SPI and Local Bus used. AX99100 also integrates power-on reset circuit and 3.3V to 1.2V voltage regulator on-chip to provide simplifies reset and power supply for the core power of the chip. It supports single power operation and reduces the overall BOM cost.

AX99100 is available in 68-pin QFN RoHS compliant package and supports commercial grade operating temperature range from 0 to 70℃ and Industrial grade operating temperature range from -40 to 85℃.

AX99100 provides cost effective solution to enable simple, easy, and low cost integration capability for PCIe to rich interface conversion applications. It could also provide highly programmable flexibility and compatibility for many applications such as serial, parallel and Bridge for home automation and Industrial control.

1.2 AX99100 Block Diagram

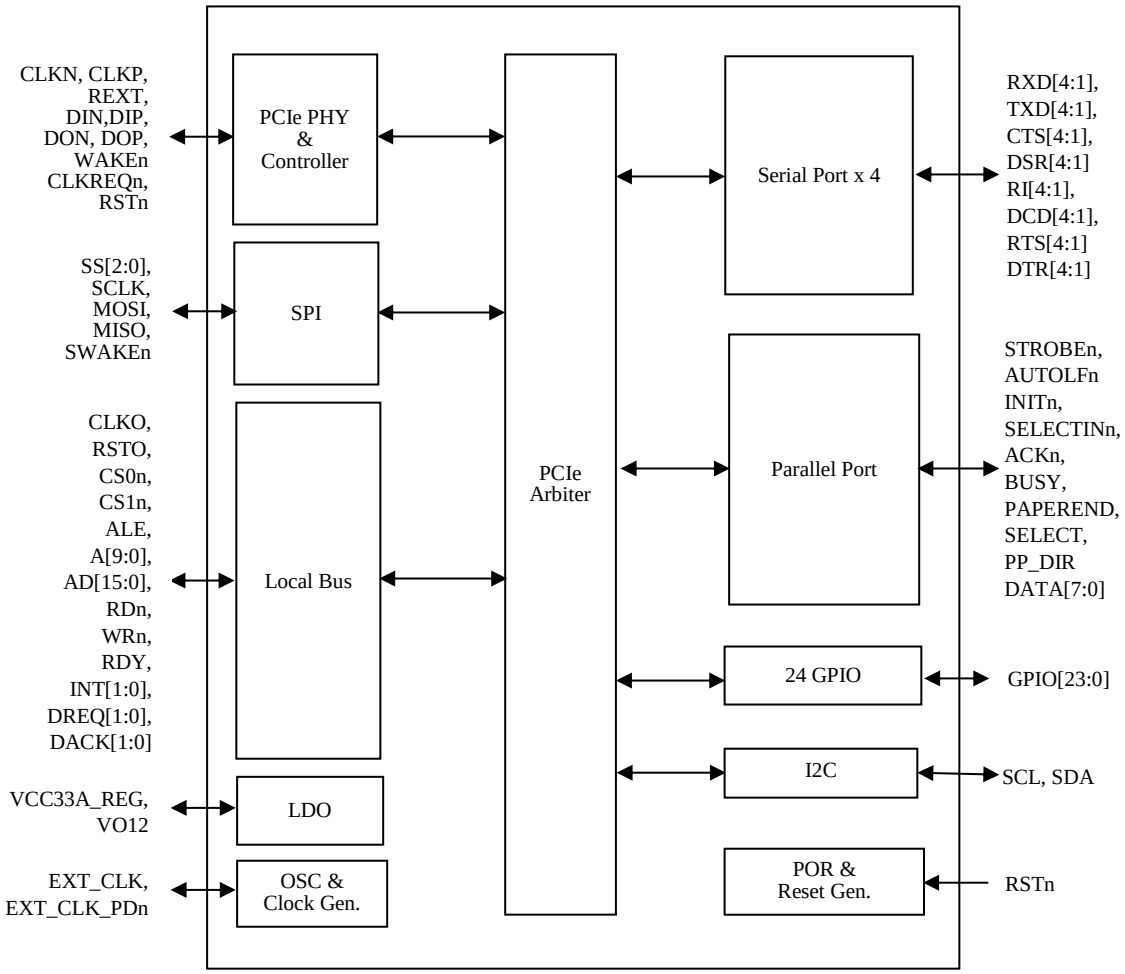


Figure 1-1: AX99100 Block Diagram

1.3 AX99100 Pinout Diagram

AX99100 is housed in a 68-pin QFN package.

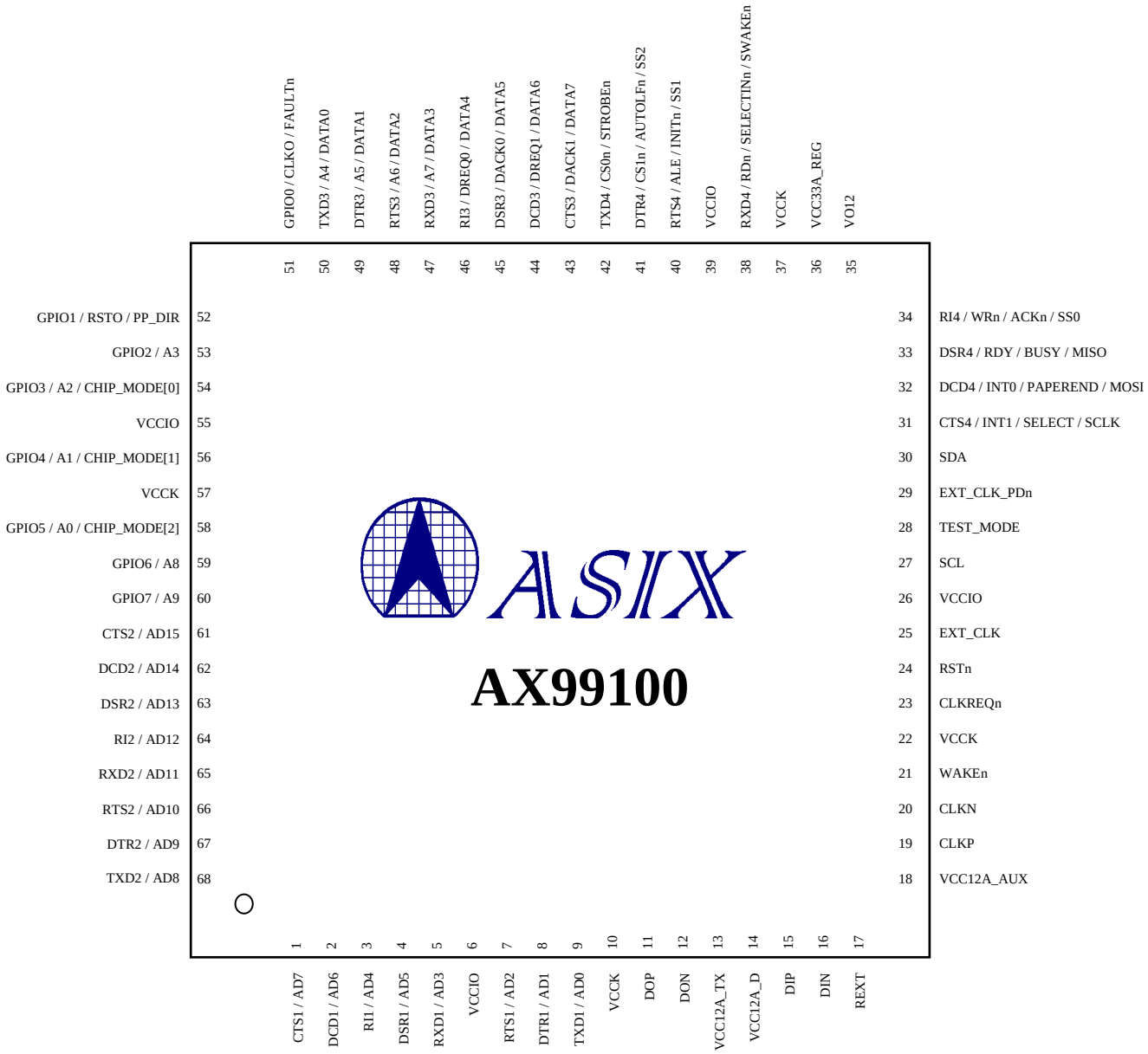


Figure 1-2: AX99100 Pinout Diagram

1.4 Signal Description

Following abbreviations are used in "Type" column of following pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attribute in "Type" column for different signal definition.

AB	Analog Bi-directional I/O
AI	Analog Input
AO	Analog Output
B3	Bi-directional I/O, 3.3V
B5	Bi-directional I/O, 3.3V with 5V tolerant
I3	Input, 3.3V
I5	Input, 3.3V with 5V tolerant
O3	Output, 3.3V
O5	Output, 3.3V with 5V tolerant
PU	Internal Pull-Up (75K)
PD	Internal Pull-Down (75K)
CU	Controllable internal Pull-Up
P	Power and ground pin
S	Schmitt Trigger
T	Tri-state
4m	4mA driving strength
8m	8mA driving strength

For example, pin 5 in AX99100 package can be RXD1 or AD3. If RXD1 is selected, its Type is I5/PU; if AD3 is selected, its Type is B5/4m. In other words, the PU (internal pull-up) only takes effect in RXD1 signal mode while AD3 signal mode doesn't. User should refer to the table specific to desired function for exact pin type definition.

The multi-function pin settings are configured by pin 54, 56 and 58 to decide the chip operating mode. Please reference to Section 3 in detailed. The following abbreviations are used in pin description tables.

HWCFGEE I^2C Hardware Configuration EEPROM
CHIP_MODE Chip Operating Mode, Setting by external pull the pin 54, 56 and 68

Table 1-1: Common Pin Description

Common Pins			
Pin Name	**Type**	**Pin No**	**Pin Description**
TEST_MODE	I5/PD	28	Test Mode enable. For normal operation, please always tie to logic low or NC.
EXT_CLK	I5	25	External Clock Input from external Oscillator.
EXT_CLK_PDn	B5	29	External Clock Power Down enable. 0: Power down external Oscillator. 1: Enable external Oscillator. Note: When external Oscillator existed, this pin should be pull down by external resistor for boot strapping latch. Otherwise, please pull-up by external resistor to indicate NO external Oscillator existed.
SCL	O5/T/4m	27	I^2C Serial Clock line for I^2C master controller. SCL is a tri-stateable output, which requires an external pull-up resistor.
SDA	B5/T/4m	30	I^2C Serial Data line for I^2C master controller. SDA is a tri-stateable output, which requires an external pull-up resistor.

Table 1-2: PCIe Pin Description

PCIe interface			
Pin Name	**Type**	**Pin No**	**Pin Description**
CLKN	AI	20	PCIe PHY differential PLL reference clock.
CLKP	AI	19	PCIe PHY differential PLL reference clock.
REXT	AO	17	Bandgap External Resistor Connect this pin to ground through an external resistor of 20KΩ, ±1%. The total parasitic capacitor of this pin to ground must be less than 10 pF
DIN	AI	16	PCIe PHY differential negative serial data input.
DIP	AI	15	PCIe PHY differential positive serial data input.
DOP	AO	11	PCIe PHY differential positive serial data output.
DON	AO	12	PCIe PHY differential negative serial data output.
WAKEn	O5/T/4m	21	An open-drain, active low signal that is driven low by a PCI Express function to reactivate the PCI Express Link hierarchy's main power rails and reference clocks.
CLKREQn	O5/T/4m	23	Reference clock request signal This pin is an open drain, active low signal that is driven low by the PCI Express Mini Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.
RSTn	I5/PU/S/ 4m	24	Active low asynchronous reset from PCIe. Indicates when the applied main power is within the specified tolerance and stable.

Table 1-3: Power/Ground Pin Description

Power/Ground Pins			
Pin Name	**Type**	**Pin No**	**Pin Description**
VCCIO	P	6, 26, 39, 55	Digital Power for I/O pins, 3.3V Please add a 0.1uF bypass capacitor between each VCCIO and GND.
VCCK	P	10, 22, 37, 57	Digital Power for core, 1.2V Please add a 0.1uF bypass capacitor between each VCCK and GND.
GND	P	EPAD	Ground for all Analog and Digital Power.
VCC33A_REG	P	36	Analog Power for Regulator, 3.3V
VO12	P	35	1.2V Power Output of on-chip 3.3V to 1.2V Regulator. The regulator requires an external capacitor (at least 3.3 µF) with low ESR for frequency compensation and stability maintenance.
VCC12A_TX	P	13	Analog Power for PCIe Transmitter, 1.2V. Please add a 0.1 and 10 uF bypass capacitor between VCC12A_TX and GND.
VCC12A_D	P	14	Analog Power for PCIe Transceiver, 1.2V. Please add a 0.1 and 10 uF bypass capacitor between VCC12A_D and GND.
VCC12A_AUX	P	18	Analog Power for PCIe Auxiliary, 1.2V. Please add a 0.1 and 10 uF bypass capacitor between VCC12A_AUX and GND.

1.4.1 GPIO and Mode Setting

Table 1-4: GPIO and Mode Setting Pin Description

GPIO and Mode Setting Pins			
Pin Name	**Type**	**Pin No**	**Pin Description**
GPIO[23:8]	B5/CU/4m	31, 32, 33, 34, 38, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50	General Purpose I/O signal GPIO[15:8] are only valid when **CHIP_MODE** = 100 and 110. GPIO[23:16] are only valid when **CHIP_MODE** = 100 and 110 and Port 4 was disabled by **HWCFGEE**. Please reference to Section 3.
GPIO7	B5/CU/8m	60	General Purpose Output signal GPIO7 has an optional function is external wakeup pin in input direction. When AX99100 entered to L2 mode, this pin can be used to wakeup AX99100 also.
GPIO6	B5/CU/8m	59	General Purpose Output signal GPIO6 has an optional function is a power-down control signal to power down the external transceiver when AX99100 entered to L2 mode. This function can be enabled by setting bit1 and the polarity selection is bit0 in configuration EEPROM, offset 0x55.
GPIO5/ CHIP_MODE[2]	O5/ 8m	58	General Purpose Output signal when chip exited reset and operating in normal functional mode. These pins are input direction during chip reset use to bootstrap the mode setting to decide the chip operation mode. Please reference to Section 3.1.
GPIO4/ CHIP_MODE[1]	O5/8m	56	
GPIO3/ CHIP_MODE[0]	O5/8m	54	
GPIO2	O5/8m	53	General Purpose Output signal when chip exited reset and operating in normal functional mode. This pin should be connected to the AUX 3.3V in PCIe slot via an external pull-up resistor. It is used to detect the 3.3V AUX is existed or not.
GPIO1	B5/CU/8m	52	General Purpose I/O signal
GPIO0	B5/CU/8m	51	General Purpose I/O signal

Note: Above GPIO[7:0] are only valid when **CHIP_MODE** ≠ 000.

1.4.2 Serial Interface for COM Port

Table 1-5: Serial Interface for COM Port Pin Description

Serial Interface for COM Port			
Pin Name	**Type**	**Pin No**	**Pin Description**
TXD1 TXD2 TXD3 TXD4	O5/4m	9 68 50 42	Transmit data output to transceiver or IrDA data output to IR LED
DTR1 DTR2 DTR3 DTR4	B5/PD/4m	8 67 49 41	Data Terminal Ready These pins have internal pull-down during reset. If there is the external pull-up resisters connected to these pins separately, it will work for RS-232 function with active low. Otherwise, it will work for RS-485 function (DXEN) with active high and the output can be enabled by register (the default is disabled). Please reference to Section 3.2.
RTS1 RTS2 RTS3 RTS4	O5/4m	7 66 48 40	Request to send (Active Low) Note: These pins will be changed to RXEN when Software enabled RS-485 function for the corresponding ports.
RXD1 RXD2 RXD3 RXD4	I5/PU	5 65 47 38	Serial received data input from transceiver or IrDA data input from IrDA detector.
RI1 RI2 RI3 RI4	I5	3 64 46 34	Ring Indicator (Active Low)
DSR1 DSR2 DSR3 DSR4	I5	4 63 45 33	Data Set Ready (Active Low)
DCD1 DCD2 DCD3 DCD4	I5	2 62 44 32	Data Carrier Detect (Active Low)
CTS1 CTS2 CTS3 CTS4	I5	1 61 43 31	Clear to send (Active Low)

Note 1: Serial Port 1 and 2 are only valid when **CHIP_MODE** = 001, 011, 101 and 110.
Note 2: Serial Port 3 and 4 are only valid when **CHIP_MODE** = 011.

1.4.3 Serial Interface for Multi-Protocol Transceiver

Table 1-6: Serial Interface for Multi-Protocol Transceiver Pin Description

Serial interface for Multi-Protocol Transceiver			
Pin Name	**Type**	**Pin No**	**Pin Description**
TXD1 TXD2 TXD3 TXD4	O5/4m	9 68 50 42	Transmit data output to transceiver or IrDA data output to IR LED
DXEN1 DXEN2 DXEN3 DXEN4	B5/PD/4m	8 67 49 41	Driver Enable These pins have internal pull-down during reset. If there is the external pull-up resisters connected to these pins separately, it will work for RS-232 function with active low. Otherwise, it will work for RS-485 function with active high and the output can be enabled by register (the default is disabled). Please reference to Section3.2.
RTS1 RTS2 RTS3 RTS4	O5/4m	7 66 48 40	Request to send (Active Low)
RXD1 RXD2 RXD3 RXD4	O5/PU/4m	5 65 47 38	Serial received data input from transceiver or IrDA data input from IrDA detector.
485EN1 485EN2 485EN3 485EN4	O5/4m	3 64 46 34	Interface Selection 1: RS-485 selected 0: RS-232 selected
485TE1 485TE2 485TE3 485TE4	O5/4m	4 63 45 33	RS485 Termination Enable for transceiver.
RXEN1 RXEN2 RXEN3 RXEN4	O5/4m	2 62 44 32	Receiver Enable 1: Enable Receiver 0: Disable Receiver Note: Software should enable RS-485 function for the corresponding ports first.
CTS1 CTS2 CTS3 CTS4	I5	1 61 43 31	Clear to send (Active Low)

Note 1: Serial Port 1 and 2 are only valid when **CHIP_MODE** = 010, 100 and 111.
Note 2: Serial Port 3 and 4 are only valid when **CHIP_MODE** = 101 and 111.

1.4.4 Serial Port with GPIO enabled

Table 1-7: Serial Interface for GPIO Enabled Pin Description

Enable Serial Port for GPIO mode			
Pin Name	**Type**	**Pin No**	**Pin Description**
TXD1 TXD2 TXD3 TXD4	O5/4m	9 68 50 42	Transmit data output to transceiver or IrDA data output to IR LED
SP1_GPIO0 SP2_GPIO0 SP3_GPIO0 SP4_GPIO0	B5/CU/4m	8 67 49 41	Serial Port GPIO
SP1_GPIO1 SP2_GPIO1 SP3_GPIO1 SP4_GPIO1	B5/CU/4m	7 66 48 40	Serial Port GPIO
RXD1 RXD2 RXD3 RXD4	O5/PU/4m	5 65 47 38	Serial receives data input from transceiver or IrDA data input from IrDA detector.
SP1_GPIO5 SP2_GPIO5 SP3_GPIO5 SP4_GPIO5	B5/CU/4m	3 64 46 34	Serial Port GPIO
SP1_GPIO3 SP2_GPIO3 SP3_GPIO3 SP4_GPIO3	B5/CU/4m	4 63 45 33	Serial Port GPIO
SP1_GPIO4 SP2_GPIO4 SP3_GPIO4 SP4_GPIO4	B5/CU/4m	2 62 44 32	Serial Port GPIO
SP1_GPIO2 SP2_GPIO2 SP3_GPIO2 SP4_GPIO2	B5/CU/4m	1 61 43 31	Serial Port GPIO

Note: Above Serial Port GPIO function are valid when Software enabled the GPIO function by register setting in each functions.

1.4.5 Serial Port with Function Disabled

Table 1-8: Serial Interface with Port2 and Port4 Disabled Pin Description

Serial Interface with Port2 and Port4 Disabled			
Pin Name	**Type**	**Pin No**	**Pin Description**
TXD2 TXD4	O5/4m	68 42	No any function for this pin due to disable.
SP1_GPIO0 SP3_GPIO0	B5/CU/4m	67 41	Serial Port GPIO(Note 2)
SP1_GPIO1 SP3_GPIO1	B5/CU/4m	66 40	Serial Port GPIO
RXD2 RXD4	O5/PU/4m	65 38	No any function for this pin due to disable.
SP1_GPIO5 SP3_GPIO5	B5/CU/4m	64 34	Serial Port GPIO
SP1_GPIO3 SP3_GPIO3	B5/CU/4m	63 33	Serial Port GPIO
SP1_GPIO4 SP3_GPIO4	B5/CU/4m	62 32	Serial Port GPIO
SP1_GPIO2 SP3_GPIO2	B5/CU/4m	61 31	Serial Port GPIO

Note 1: If Port 2 or Port 4 are disabled by setting **HWCFGEE** when **CHIP_MODE** setting for those serial port interface, all pins for Port 2 or Port 4 (excluded TXD and RXD) will be re-directed to the GPIO function of Port 1 and Port 3. Thus the pins of Port 1 and Port 3 cannot be set for GPIO function by software register setting.

Note 2: Pin 67 and 41 will be re-directed to DTR1/DXEN1 and DTR3/DXEN3 also. However software can enable it to GPIO function as SP1_GPIO0 and SP3_GPIO0.

1.4.6 Parallel Port

Table 1-9: Parallel Port Pin Description

Parallel Port Interface			
Pin Name	**Type**	**Pin No**	**Pin Description**
STROBEn	SPP: O5/T/4m Others: O5/4m	42	Set active low by the host to transfer data into the input latch of the peripheral. Data are valid while STROBEn is low. The pin is open-drain when operation in SPP mode, otherwise, is direct drive logic 0 or logic 1.
AUTOLFn	SPP: O5/T/4m Others: O5/4m	41	The interpretation of this signal varies from peripheral to peripheral. Set low by host to put some printers into auto-line feed mode The pin is open-drain when operation in SPP mode, otherwise, is direct drive logic 0 or logic 1.
INITn	SPP: O5/T/4m Others: O5/4m	40	Pulsed low by the host in conjunction with IEEE 1284 Active low to reset the interface and force a return to Compatibility Mode idle phase The pin is open-drain when operation in SPP mode, otherwise, is direct drive logic 0 or logic 1.
SELECTINn	SPP: O5/T/4m Others: O5/4m	38	Set low by host to select peripheral The pin is open-drain when operation in SPP mode, otherwise, is direct drive logic 0 or logic 1.
PP_DIR	O5/4m	52	Parallel Port Data Transfer Direction Indications
ACKn	I5	34	Pulsed low by the peripheral to acknowledge transfer of a data byte from the host
BUSY	I5	33	Driven high by the peripheral to indicate that it is not ready to receive data
PAPEREND	I5	32	Driven high by the peripheral to indicate that is has encountered an error in its paper path. The meaning of this signal varies from peripheral to peripheral. Peripherals shall set FAULTn low whenever PAPEREND is set high
SELECT	I5	31	Set high to indicate that the peripheral is online
FAULTn	I5	51	Set low by the peripheral to indicate that an error has occurred. The meaning of this signal varies from peripheral to peripheral
DATA[7:0]	B5/4m	43, 44, 45, 46, 47, 48, 49, 50	Driven by the host in Compatibility Mode and the negotiation phase, not used in Nibble Mode, and bidirectional in all other modes

Note: Above signals are only valid when **CHIP_MODE** = 010 and 001.

1.4.7 SPI Interface

Table 1-10: SPI Pin Description

SPI Interface			
Pin Name	**Type**	**Pin No**	**Pin Description**
SS[2:0]	O5/4m	41, 40, 34	SPI Slave Select for SPI master. SS[2:0] is a tri-stateable output, which requires an external pull-up resistor.
SCLK	O5/4m	31	SPI CLocK for SPI master. SCLK is a tri-stateable output. At Mode 0 or 2, SCLK requires external pull-down resistor; while at Mode 1 or 3, SCLK requires external pull-up resistor.
MOSI	O5/4m	32	SPI Master Output Slave Input line for SPI master. When High Speed SPI controller is operating in master module, MOSI is used to transmit serial data and is a tri-stateable output.
MISO	I5	33	SPI Master Input Slave Output line for SPI master. When High Speed SPI controller is operating in master module, MISO is used to receive serial data.
SWAKEn	I5/PU	38	SPI External Wakeup SWAKEn is external wakeup for SPI interface.
GPIO16	B5/8m	42	General Purpose I/O signal

Note: Above signals are only valid when **CHIP_MODE** = 100 and 110.

1.4.8 Local Bus Interface

Table 1-11: Local Bus Pin Description

Local Bus Interface			
Pin Name	**Type**	**Pin No**	**Pin Description**
A0/ CHIP_MODE[2]	O5/4m	58	Local Bus Address Bus, A[2:0] These pins are input direction during chip reset use to bootstrap the mode setting to decide the operation mode. Please reference to Section 3.1. In Local Bus mode, These pins should always use external pull-down resistors to ground.
A1/ CHIP_MODE[1]	O5/4m	56	
A2/ CHIP_MODE[0]	O5/4m	54	
A3	O5/4m	53	Local Bus Address Bus, A[3] This pin should be connected to the 3.3V AUX in PCIe slot via an external pull-up resistor. It is used to detect the 3.3V AUX is existed or not.
A[9:4]	O5/4m	60, 59, 47, 48, 49, 50	Local Bus Address Bus, A[9:4] The A[9:0] are outputs and provide up to 10 Local Bus address lines in non-multiplexed address and data bus format
AD[15:0]	B5/4m	61, 62, 63, 64, 65, 66, 67, 68, 1, 2, 4, 3, 5, 7, 8, 9	Data and Address bus Multiplexed mode: address on bus when ALE issued, other time data on bus Non-multiplexed mode: data always on bus
RSTO	B5/4m	52	Local Bus Reset Output The output polarity can be decided by adding external pull up/down resistor. If connected this pin to VCCIO via external pull-up resistor, means RSTO is active high. If pull-down to ground, means active low.
CLKO	B5/8m	51	Local Bus Clock Output
CS1n CS0n	O5/4m	41 42	Local Bus Chip Select 1 Local Bus Chip Select 0
DREQ[1:0]	I5	44, 46	DMA Request
DACK[1:0]	O5/4m	43, 45	DMA Acknowledge
INT[1:0]	I5	31, 32	Interrupt
ALE	O5/4m	40	Address Latch Enable When in non-multiplexed mode, ALE can choice remap to A[10] (detail description same as above A[9:0]) or address latch enable for ISA bus type When in multiplexed mode, ALE for address latch enable
RDn	O5/4m	38	Local Bus Read Cycle
WRn	O5/4m	34	Local Bus Write Cycle
RDY	I5	33	Local Bus Device Ready

Note: Above signals are only valid when **CHIP_MODE** = 000.

2 Function Description

2.1 Clocks/Resets and Power

The AX99100 requires an external clock from PCIe connector (CLKP and CLKN) as the main clock source. PCIe PHY feeds this 100 MHz differential clock to internal PLL to generate the 125MHz clock for PCIe PHY and Controller or other peripherals used. The AX99100 also supports a clock input from external oscillator for those special baud rate generated for UART, SPI and Local Bus used if needs. Thus there are three different clock sources (100Mhz, 125Mhz and EXT_CLK) in this chip can be selected for some interfaces to generate the desired baud rate to meet the application requirement.

There are two reset sources in the AX99100. During the VCCK power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks when the VCCK power pin rise to certain threshold voltage level. Another reset is RSTn pin, which is from PCIe slot to perform the PCIe Fundamental Reset. If AX99100 is not in L2 power sate, this reset pin will logical and with POR reset to reset all the function blocks also. AX99100 is designed to meet the PCIe standard for Power Management State.

The AX99100 contains an internal 3.3V to 1.2V low-dropout-voltage regulator. The internal regulator provides up to 150mA of driving current for the 1.2V core and analog power of this chip to satisfy the worst-case power consumption scenario.

In order to support PCIe power management, all VCCIO power and the regulator power supply should connect to PCIe Auxiliary Power (3.3Vaux) to maintain the deep sleep and wakeup event.

2.2 PCIe Operation

PCIe is divided into three major blocks as Physical layer, Data link layer and Transaction layer. Physical link layer and Transaction layer together comprises PCIe core. Their functionality is explained below.

PCIe PHY
The Physical Layer isolates the Transaction and Data Link Layers from the signaling technology used for Link data interchange. The Physical Layer is divided into the logical and electrical functional sub-blocks.

The logical sub-block has two main sections: A transmit section that prepares outgoing information passed from the Data Link Layer for transmission by the electrical sub-block, and a receiver section that identifies and prepares received information before passing it to the Data Link Layer. The logical sub-block and electrical sub-block coordinate the state of each transceiver through a status and control register interface or functional equivalent. The logical sub-block directs control and management functions of the Physical Layer.

The electrical sub-block contains a Transmitter and a Receiver. The Transmitter is supplied by the logical sub-block with Symbols which it serializes and transmits onto a Lane. The Receiver is supplied with serialized Symbols from the Lane. It transforms the electrical signals into a bit stream which is de-serialized and supplied to the logical sub-block along with a Link clock recovered from the incoming serial stream.

The Physical Layer is responsible for the following
- Power management
- Width and lane negotiation
- Reset/hot-plug control
- 8-bit/10-bit encoding/decoding
- Scrambling/de-scrambling
- Embedded clock tuning and alignment
- Transmission and reception circuit
- Elastic buffer
- Data Link Layer

The Data Link Layer

The Data Link Layer acts as an intermediate stage between the Transaction Layer and the Physical Layer. The Data Link Layer is responsible for reliably conveying Transaction Layer Packets (TLPs) supplied by the Transaction Layer across a PCI Express Link to the other component's Transaction Layer

The Data Link Layer is responsible for the following

- Link management including TLP acknowledgment
- Retry mechanism in case of a non-acknowledged packet
- Flow control across the Link (transmission and reception)
- Power management
- CRC generation and CRC checking
- Error reporting

Transaction Layer/User Interface Layer

Transaction layer and User interface layer together perform all transaction layer functionalities. User interface layer defines a plug-and-play type interface mechanism to accept TLPs from user space for transmission, and to pass received TLPs on reception.

The Transaction Layer is primarily responsible for the following

- Assembly and disassembly of Transaction Layer packets (TLPs)
- Storage of configuration information
- Converts received Completion packets into data payloads,
- Updates status information
- Responsible for flow control services
- Ordering rules
- Power management services
- PCIe Bridge
- Master Slave Bridge is divided into PCIe packet formatter, PCIe target interface block, Mater arbiter, Slave de-mux and VCI interface block.

All detail description for PCIe operation, please reference to the standard of "PCI Express Base Specification".

2.3 I²C Controller

The I²C Controller of AX99100 contains of an I²C master to support communication to external I²C devices and an I²C Hardware Configuration EEPROM Loader to support loading chip configuration data from external I²C EEPROM during chip reset.

2.4 Serial Port (SP)

The AX99100 supports up to 4 Serial Ports, namely, Serial Port 1/2/3/4. Each serial port is compatible with standard 16C450, 16C550 and Extend 16C550, 16C650, 16C750 and 16C950 device architectures and the default operating mode is set to 16C450. Each serial port provides serial communication capabilities to communicate with Modem or other external device (e.g. computer) using RS-232, RS-422 or RS-485 protocols and support slow IrDA mode (up to 115200bps). It supports customized transfer baud rate (up to 25Mbps) by programming internal divider register or external clock, provides 256-byte Transmitter and Receiver FIFO for data buffering, supports DMA mode burst transfer for data receive and transmit process, and supports Auto-hardware flow control (Auto-RTS and Auto-CTS) and Auto-software flow control (Auto-send and Auto-detect XON and XOFF characters) to reduce CPU/software loading.

Each serial port supports 5, 6, 7, 8 bit Serial format. In addition, it also supports 9 bit serial format to accomplish multi-drop function. Each serial port supports Even, Odd, None, Space and Mark parity. Furthermore, it also supports remote wakeup, power management and transceiver shutdown features.

2.5 Parallel Port (PP)

The Parallel Port of AX99100 is a bidirectional extension of the existing PC parallel interface. The interface supports a number of distinct communication modes, and the interpretation of interface signals depends on the current mode. The different modes are Compatibility, Nibble, Byte and ECP modes. Not all devices support all communication modes. A mechanism is provided for the host and peripheral to negotiate the mode to be used for data transfers and to renegotiate as needed. The host may return the link to the Compatibility Mode whenever the interface is in a valid state, which is uniquely specified for each mode.

Compatibility Mode: This is an asynchronous data transfer mode, byte-wide forward (host-to-peripheral) channel with data and status lines. This Mode provides host-to-peripheral communication in a manner compatible with the traditional unidirectional interface.

Nibble Mode: This is an asynchronous data transfer mode, reverse (peripheral-to-host) channel, under control of the host.

Byte Mode: This is an asynchronous, byte-wide reverse (peripheral-to-host) channel using the eight data lines of the interface for data and the control/status lines for handshaking.

Extended Capabilities Port (ECP) Mode: This is an asynchronous byte-wide mode, bidirectional channel.

2.6 SPI Master Controller (SPI)

The AX99100 contain the High Speed Serial Peripheral Interface (SPI) Master Controller provides a full-duplex, synchronous serial communication interface (4 wires) to flexibly work with numerous SPI peripheral devices. The High Speed SPI Controller consists of a High Speed SPI master controller with 3 slave select pins, SS[2:0], to connect up to 7 SPI devices.

This High Speed SPI master controller supports 4 types of interface timing mode, namely, Mode 0, Mode 1, Mode 2, and Mode 3 to allow working with most SPI devices available. It supports MSB/LSB first data transfer. The SCLK SPI clock is programmable by software and can run up to 42MHz. The AX99100 also provides many programmable registers can be used to adjust the bus timing to fit the variety Slave timing requirements. Please reference the section 4.5.4.

The AX99100 SPI master supports four kinds of access types below.
Non-Burst-Type Transfer: Supports up to 8 bytes registers can be read and written by Software with none DMA access.

Burst-Type Transfer: Supports TX/RX DMA transfer. Upon configured by software and one DMA length up to 64K bytes, SPI RX DMA supports moving data from SPI bus through SPI RX FIFO into PCIe BUS; SPI TX DMA supports moving data from PCIe BUS through SPI TX FIFO to SPI bus.

Burst-Type with OP-code Transfer: supports up to 8 bytes pre-programmable OP code automatic insertion in each Burst-Type Transfer with successive chip select assertion, to reduce CPU/software loading.

Fragmentation: supports to fragment large data block into several smaller transfers on SPI bus with programmable length for each small transfer fragment, to reduce CPU/software loading.

2.7 Local Bus Controller (LB)

The AX99100's Local Bus mode provides a PCIe bus target (slave) for adapter boards, in others words, AX99100 can connect a wide variety local bus design to PCIe bus.

The local bus mode provides four PCIe BARs for access, BAR0 and BAR1 direct mapping to local bus's chip select (CS0n and CS1n), configurable with Memory or I/O access with Hardware Configuration EEPROM setting. Software can use PCIe memory or I/O command through BAR0/1 to access device with local bus directly or active bus master function (DMA) to transfer large data between PCIe and device. The bus master's access can be programmed for port mapping (fixed address) or memory mapping (auto-increment address) also. Another two BARs are BAR4 (I/O access) and BAR5 (memory access) serve software and driver handle whole PCIe and local bus function. These two BARs are mapped to same registers to provide local bus access timing adjustment, control pins setting (polarity, remapping etc.), interrupt control and status response, DMA engine (bus master controller) handling, and I^2C controller assessment.

The local bus can be configured to asynchronous or synchronous mode, 8 or 16 bits data bus width, data bus alignment with MSB or LSB when bus width 8 bits and endian type with big or little mode. The address/data of local bus can be set to Multiplexed or Separated bus type, address/data setup timing, address/data hold timing, address latch enable timing, read cycle timing and write cycle timing, control pin polarity, and output enable. Above all parameters can be loaded from EEPROM, and most timing parameters and bus configuration could be adjusted by BAR4/5 related registers too. The BAR0/1 space size could up to 64K Bytes when local bus use address/data multiplex bus type. If use the separated bus type, the largest size of BAR0/1 are only to 2K Bytes (remapping ALE to A[10]) or 1K Bytes with ISA bus type (ALE presented access).

The Local Bus of AX99100 also supports clock output (CLKO), which can be configured to generate up to 62.5MHz with internal 125 MHz clock source or 60MHz with external clock source from EXT_CLK, and reset output (RSTO), which can be controlled by Software Driver to reset the related off-chip components.

The Local Bus supports address shift feature with local bus shift base register, used for those device with small BAR space match to local bus with non-zero starting address (like ISA bus device), the chip select also supports starting address shifting and range resizing feature too.

To enhance the performance, local bus supports "Slave Request based DMA" mode. After software configured external device and DMA engine was ready, bus master transfer data between PCIe bus and local bus's device followed device request to reduce the efforts for the Software checking device status timing.

The Local Bus of AX99100 supports the remote wakeup in L2 power state for PCIe. Application can use INT0/1 and DREQ0/1 pins to generate the wakeup event to PCIe bus to exit L2 power state.

2.8 GPIO Function

There are up to 24 General Purpose Input/output pins (GPIO[23:0]) in AX99100, reference section 1.4.1, Table 1-4, in none Local Bus mode. The driving strength of GPIO[7:0] are 8mA and GPIO[23:8] are 4mA only. Each GPIO pin is independent and can be configured for input or output, open drain or direct drive, internal pull-up enabled and event mode detection for IRQ generation. Due to GPIO[5:2] have been used for CHIP_MODE and 3.3Vaux detection, these pins can be used as the directed drive output pin without internal pull-up feature.

2.9 Power Management

The AX99100 supports the following power management and budgeting features.

- Compliant with PCI Power Management Interface Specification 1.2
- Supports Native Active State Power Management L0s state
- Supports Power Management Event (PME message)
- Supports CLK_REQ mechanism for Express card interface
- Supports wakeup from D3 hot and D3 cold states

AX99100 supports all the device power management states defined in **PCI Bus Power Management Interface Specification 1.2**. Power Management capabilities are mentioned in Power Management Capability (PMC) register of configuration space which provides information on the capabilities of the function related to power management. Bit[15] of PMC, i.e. wake from D3 cold is supported only if auxiliary power is present, this bit is updated through bootstrap option on pin “GPIO2” or “A3” (weak pull-up with supply 3.3V AUX is connected to pin “GPIO2” or “A3”) and logic AND with the contents in Bit[2] of EEPROM offset 0Fh(Func0), 23h(Func1), 37h(Func2) and 4Bh(Func3) corresponds to Bit[15] of PMC, please reference section 3.3.1, Power Management Capabilities_Fx, in detail.

AX99100 Supports wakeup from any power management capable device connected to AX99100 from both D3 hot and D3 cold states.

D3 hot: Any device connected to AX99100 can wakeup the system from D3-hot state (Standby) through WAKEn (referred as WAKE# in **PCIe base specification 1.1**) or through PME message. Default wakeup is through WAKEn. EEPROM should be configured in order to wake the PC through PME message from D3 hot state.

D3 cold: Any devices connected to AX99100 can wakeup the system from D3-cold state (Hibernate) through WAKEn only (referred as WAKE# in **PCIe base Specification 1.1**).

Note: There is NO power plane separation between 3.3V AUX and VCCIO in AX99100. In D3 Cold, the chip VCCIO and VCC33A_REG should be powered from 3.3V AUX to support remote wake up.

3 Chip Configuration

3.1 Boot Strapping Pins for Chip Mode

The AX99100 is able to configure to 8 different chip modes by pull up or pull down the Pin 54, 56 and 58. These pins will be pulled up internally during reset. Therefore, user just needs to use external resistor to pull down these pins for the chip mode setting to '0'. But it is still accepted if user would like to use the external resistor to pull up these pins for the mode setting to '1'.

Pins	Signal Name	Description
54	CHIP_MODE[0]	Chip Mode Select bit 0 0: Added external pull-down resistor to this pin. 1: Otherwise.
56	CHIP_MODE[1]	Chip Mode Select bit 1 0: Added external pull-down resistor to this pin. 1: Otherwise.
58	CHIP_MODE[2]	Chip Mode Select bit 2 0: Added external pull-down resistor to this pin. 1: Otherwise.

Table 3-1: Chip Mode Selection Pins

There are 8 chip modes (**4MP**, **2S1SPI**, **2S2MP, 2MP1SPI, 4S, 2MP1P, 2S1P and LB)** can be selected by different pull-down for **CHIP_MODE**. It is the detail descriptions for the each chip mode abbreviations below.

4MP	Means to support four Serial Ports with Multi-Protocol transceivers in PCIe function 0~3.
2S1SPI	Means to support two general Serial Ports in function 0~1 and one SPI master in PCIe function 3.
2S2MP	Means to support two general Serial Ports in function 0~1 and two Serial Ports with Multi-Protocol transceivers in PCIe function 2~3.
2MP1SPI	Means to support two Serial Ports with Multi-Protocol transceivers in function 0~1and one SPI master in PCIe function 3.
4S	Means to support four general Serial Ports in PCIe function 0~3.
2MP1P	Means to support two Serial Ports with Multi-Protocol transceivers in function 0~1and one Parallel Port in PCIe function 2.
2S1P	Means to support two general Serial Ports in function 0~1 and one Parallel Port in PCIe function 2.
LB	Means to support one Local Bus interface in PCIe function 0.

Following table specified abbreviation of all chip modes with **CHP_MODE**[2:0] decode and port mapping. "GPIO" is for GPIO[15:8], it occupies the 8 pins in Port 3 and controlled by BAR5 in each function same as GPIO[7:0] pins. "Parallel Port" occupies the pins of Port 3 and 4 and controlled by function 2 in PCIe. "SPI" occupies the pins of Port 4 and controlled by function 3 in PCIe. "LB" is for Local Bus interface, it occupies all pins from Port 1 to Port 4 but only controlled by function 0 in PCIe. In "Serial Port" and "Multi-protocol", Port 1 will be controlled by function 0, Port 2 controlled by function 1, Port 3 controlled by function 2 and Port 4 controlled by function 3 in PCIe.

Table 3-2: Chip Mode Selection Table

CHIP_ Mode[2:0]	4MP	2S1SPI	2S2MP	2MP1SPI	4S	2MP1P	2S1P	LB
	111	110	101	100	011	010	001	000
Port 1	Multi-Protocol	Serial Port	Serial Port	Multi-Protocol	Serial Port	Multi-Protocol	Serial Port	Local Bus
Port 2	Multi-Protocol	Serial Port	Serial Port	Multi-Protocol	Serial Port	Multi-Protocol	Serial Port	
Port 3	Multi-Protocol	GPIO	Multi-Protocol	GPIO	Serial Port	Parallel Port	Parallel Port	
Port 4	Multi-Protocol	SPI	Multi-Protocol	SPI	Serial Port			

Note: The AX99100 Multi-protocol Mode is designed to support the Multi-protocol transceiver. Please contact ASIX product support for the detail.

3.2 DTR Boot Strapping Pins for Serial Port

Each Serial Port or Serial Port with multi-protocol transceivers mode can support for RS-232 or RS-485 function, the DTR/DXEN pin will has different behavior for the both mode. In Hardware design, each DTR/DXEN pin has internal pull-down during reset. User may use the external pull-up resister to decide which mode is selected for operation.

Pins	Signal Name	Description
8	DTR_MODE[0]	DTR Mode Select bit 0 for Serial Port 1 1: Added external pull-up resistor to this pin. It works for RS-232 mode with active low. 0: Otherwise, means to use internal pull-down to this pin. It works for RS-485 mode with active high.
67	DTR_MODE[1]	DTR Mode Select bit 1 for Serial Port 2 1: Added external pull-up resistor to this pin. It works for RS-232 mode with active low. 0: Otherwise, means to use internal pull-down to this pin. It works for RS-485 mode with active high.
49	DTR_MODE[2]	DTR Mode Select bit 2 for Serial Port 3 1: Added external pull-up resistor to this pin. It works for RS-232 mode with active low. 0: Otherwise, means to use internal pull-down to this pin. It works for RS-485 mode with active high.
41	DTR_MODE[3]	DTR Mode Select bit 3 for Serial Port 4 1: Added external pull-up resistor to this pin. It works for RS-232 mode with active low. 0: Otherwise, means to use internal pull-down to this pin. It works for RS-485 mode with active high.

Table 3-3: DTR Mode selection Pins

3.3 Hardware Configuration EEPROM

AX99100 can use the I^2C Hardware Configuration EEPROM (**HWCFGEE**) to overwrite some hardware default values during boot up if the Configuration EEPROM existed and the checksum is correct. If EEPROM not existed or checksum uncorrected, Hardware will skip to load the content or give up the loaded values from EEPROM then still use the hardware default values in each chip mode for the chip operation. It uses a serial EEPROM with I^2C interface with at least 256x8 (2048 bits), for example Atmel AT24C02. The 7-bit device address of the I^2C Hardware Configuration EEPROM on application circuit must be set to 1010000b. Note that the Hardware will only use the "8-bit Device Memory Address Format" to load **HWCFGEE** when boot up.

Following sections show the I^2C Hardware Configuration EEPROM memory maps with the different layouts between none Local Bus and Local Bus in EEPROM.

Following are the abbreviations for each interface function for further descriptions.

SP	For those PCIe functions which be configured to support general Serial Ports or Serial Ports with Multi-Protocol transceivers in Port 1, 2, 3 or 4.
SPI	For the PCIe function 3 which be configured to support SPI master in Port 4.
PP	For the PCIe function 2 which be configured to support Parallel Port in Port 3 and 4.
LB	For the PCIe function 0 which be configured to support Local Bus interface.

Note1: Some "Reserved" fields in **HWCFGEE** may preserve for design optimization. User should use ASIX provided EEPROM utility to modify or create the new EEPROM contents to avoid the incorrected value to cause system unstable.

Note2: Boot strapping pins and **HWCFGEE** will be reloaded in following conditions.

- Power OFF (includes 3.3VAUX) then Power ON.
- Perform PCIe reset in none L2 state.

3.3.1 Configuration EEPROM Memory Map for None Local Bus Interface

Table 3-4: Configuration EEPROM Memory Map for none Local Bus mode

EEPROM Offset	Parameter	Note
0x00	Divide Clock Selection	SPI interface used
0x01	Clock Divider	
0x03~0x02	Vendor ID_F0	Function0
0x05~0x04	Device ID_F0	
0x06	Revision ID	
0x07	Programming IF_F0	
0x08	Sub-Class Code_F0	
0x09	Base Class Code_F0	
0x0B~0x0A	Subsystem Vendor ID_F0	
0x0D~0x0C	Subsystem Device ID_F0	
0x0F~0x0E	Power Management Capabilities_F0	
0x16~0x10	Reserved	
0x18~0x17	Vendor ID_F1	Function1
0x1A~0x19	Device ID_F1	
0x1B	Programming IF_F1	
0x1C	Sub-Class Code_F1	
0x1D	Base Class Code_F1	
0x1F~0x1E	Subsystem Vendor ID_F1	
0x21~0x20	Subsystem Device ID_F1	
0x23~0x22	Power Management Capabilities _F1	
0x2A~0x24	Reserved	
0x2C~0x2B	Vendor ID_F2	Function2
0x2E~0x2D	Device ID_F2	
0x2F	Programming IF_F2	
0x30	Sub-Class Code_F2	
0x31	Base Class Code_F2	
0x33~0x32	Subsystem Vendor ID_F2	
0x35~0x34	Subsystem Device ID_F2	
0x37~0x36	Power Management Capabilities_F2	
0x3E~0x38	Reserved	
0x40~0x3F	Vendor ID_F3	Function3
0x42~0x41	Device ID_F3	
0x43	Programmable IF_F3	
0x44	Sub-Class Code_F3	
0x45	Base Class Code_F3	
0x47~0x46	Subsystem Vendor ID_F3	
0x49~0x48	Subsystem Device ID_F3	
0x4B~0x4A	Power Management Capabilities_F3	
0x52~0x4C	Reserved	
0x54~0x53	INT Mask	For each function
0x55	Port Disable Register	
0x56	Global Setting	
0x5A~0x57	Reserved	
0x5B	Check-Sum	
0x7F ~ 0x5C	Reserved	

Note: Function 2 should be disabled in SPI mode and Function 3 should be disabled in PP mode.

Divide Clock Selection (0x00)

Bit	Description
1:0	Clock source select for LB or SPI used. 00: 125MHz from internal PLL. 01: 100MHz from PCIe reference clock. 1x: EXT_CLK. Hardware Default Value: 01: In LB and SPI mode. 00: Others.
2	Divide Enable. 0: Disabled clock divider to LB and SPI module. 1: Enabled clock divider to generate desired clock frequency for LB or SPI module. Hardware Default Value: 1: In LB and SPI mode. 0: Others.
7:3	Reserved

Note: " Hardware Default Value" means HWCFGEE load failed for without Hardware Configuration EEPROM or checksum failed.

Divide Register (0x01)

Bit	Description
7:0	Clock Divider N Register. The number of N in this field is used to generate the desired clock frequency and the frequency will follow following equation: Desired clock frequency = (125MHz or 100MHz or EXT_CLK) / N Note: ◎ N equal to 0x00 or 0x01 is divided by 1, N = '2' is divided by 2, and so on. ◎ This value N should >= 2 when the clock source from 125MHz and 100MHz for SPI. Hardware Default Value: 0x02: In LB and SPI mode. 0x00: Others.

Vendor ID_Fx (0x03~0x02, 0x18~0x17, 0x2C~0x2B, 0x40~0x3F)

Bit	Description
15:0	Vendor ID_Fx. This field will be loaded into PCIe Configuration Space offset 0x00 (Vendor ID). Hardware Default Value: 0x125B. Note 1: Vendor ID_F3 = 0xFFFF In PP mode, Vendor ID_F2 = 0xFFFF In SPI mode. Note 2: Only "Vendor ID_F0" existed in LB mode.

Note: " x" is from 0~3 means PCIe function 0~3.

Device ID_Fx (0x05~0x04, 0x1A~0x19, 0x2E~0x2D, 0x42~0x41)

Bit	Description
15:0	Device ID_Fx. This field will be loaded into PCIe Configuration Space offset 0x02 (Device ID). Hardware Default Value: 0x9100 Note 1: Device ID_F3 = 0xFFFF In PP mode, Device ID_F2 = 0xFFFF In SPI mode. Note 2: Only "Device ID_F0"=(0x9110) existed in LB mode.

Revision ID (0x06)

Bit	Description
7:0	Revision ID. This field will be loaded into PCIe Configuration Space offset 0x08 (Revision ID). Hardware Default Value: 0x00

Programming IF_Fx (0x07, 0x1B, 0x2F, 0x43)

Bit	Description
7:0	Programming Interface_Fx. This field will be loaded into PCIe Configuration Space offset 0x09 (Programming Interface). Hardware Default Value: 0x02: For all SP mode. 0x03: For "Programming Interface_F3" in PP mode. 0x00: Others (includes "Programming Interface_F0" in PP or LB mode and "Programming Interface_F2" in SPI mode). Note: Only "Programming Interface_F0" existed in LB mode.

Sub-Class Code_Fx (0x08, 0x1C, 0x30, 0x44)

Bit	Description
7:0	Sub-Class Code_Fx. This field will be loaded into PCIe Configuration Space offset 0x0A (Sub-Class). Hardware Default Value: 0x80: For "Sub-Class Code_F0" in LB mode. 0x01: For "Sub-Class Code_F2" in PP mode. 0x00: Others (includes "Sub-Class Code_F3" in SPI mode and all SP mode). Note: Only "Sub-Class Code_F0" existed in LB mode.

Base Class Code_Fx (0x09, 0x1D, 0x31, 0x45)

Bit	Description
7:0	Base Class Code_Fx. This field will be loaded into PCIe Configuration Space offset 0x0B (Base Class). Hardware Default Value: 0x07: For all SP mode and "Base Class Code_F2" in PP mode. 0x06: For "Base Class Code_F0" in LB mode 0xFF: For "Base Class Code_F3" in SPI mode 0x00: Others Note: Only "Base Class Code_F0" existed in LB mode.

Subsystem Vendor ID_Fx (0x0B~0x0A, 0x1F~0x1E, 0x33~0x32, 0x47~0x46)

Bit	Description
15:0	Subsystem Vendor ID_Fx. This field will be loaded into PCIe Configuration Space offset 0x2C (Subsystem Vendor ID). Hardware Default Value: 0xA000 Note: Only "Subsystem Vendor ID_F0" existed in LB mode and if the function has been disabled this file should be set to 0x0000.

Subsystem Device ID_Fx (0x0D~0x0C, 0x21~0x20, 0x35~0x34, 0x49~0x48)

Bit	Description
15:0	Subsystem Device ID_Fx. This field will be loaded into PCIe Configuration Space offset 0x2E (Subsystem Device ID). Note: ◎For SP related PCIe function, bit15~12 should be set to 0x1. ◎For PP related PCIe function, bit15~12 of "Subsystem Device ID_F2" should be set to 0x2. ◎For SPI related PCIe function, bit15~12 of "Subsystem Device ID_F3" should be set to 0x6. Hardware Default Value: 0x1000: For all SP function. 0x2000: For "Subsystem Device ID_F2" in PP mode. 0x6000: For "Subsystem Device ID_F3" in SPI mode. 0x7000: For "Subsystem Device ID_F0" in LB mode. Note: Only "Subsystem Device ID_F0" existed in LB mode and if the function has been disabled this file should be set to 0x0000.

Power Management Capabilities_Fx (0x0F~0x0E, 0x23~0x22, 0x37~0x36, 0x4B~0x4A)

Bit	Description
0	No Soft Reset. This field will be loaded into PCIe Configuration Space offset 0x7C (Power Management Status/Control Register), bit 3. Hardware Default Value:0x1.
3:1	Maximum Current Required. This field will be loaded into PCIe Configuration Space offset 0x78 (Power Management Capabilities Register), bit 24:22. Hardware Default Value:0x7 (375 mA).
4	D1 Support. This field will be loaded into PCIe Configuration Space offset 0x78 (Power Management Capabilities Register), bit 25. Hardware Default Value:0x1.
5	D2 Support. This field will be loaded into PCIe Configuration Space offset 0x78 (Power Management Capabilities Register), bit 26. Hardware Default Value:0x1.
10:6	PME Support. This field will be loaded into PCIe Configuration Space offset 0x78 (Power Management Capabilities Register), bit 31:27. {D3 cold, D3 hot PME, D2 PME, D1 PME, D0 PME}. Note: Bit10, D3 cold, will be "and" logic operation with the 3.3V AUX detect (GPIO2/A3 pull-up Aux3.3V). Hardware Default Value:0x1F.

Note 1: Only " Power Management Capabilities_F0" existed in LB mode.
Note 2: This field should be set to 0x0000 if this function is disabled.

INT Mask (0x54~0x53)

Bit	Description
3:0	Setting INT A bit mapping (0x1) for Function 0. Hardware Default value: 0x1.
7:4	Setting INT B bit mapping (0x2) for Function 1. Hardware Default value: 0x0: for LB mode. 0x2: Others.
11:8	Setting INT C bit mapping (0x4) for Function 2. Hardware Default value: 0x0: For LB and SPI mode. 0x4: Others.
15:12	Setting INT D bit mapping (0x8) for Function 3. Hardware Default value: 0x0: For LB and PP mode. 0x8: Others.

Port Disable Register (0x55)

Bit	Description
0	XCVR Polarity Selection. 1: XCVR is active Low when AX99100 enter L2(D3) power saving mode 0: XCVR is active High when AX99100 enter L2(D3) power saving mode Note: This bit is valid when set Bit1 to '1'. Hardware Default value: 0x0
1	XCVR Function Enable Enable the output of GPIO6 as "XCVR" function to shutdown external Serial Port transceiver in L2 power state. 1: Enable XCVR function output to GPIO6 0: Disable XCVR output to GPIO6, the GPIO6 is a generic GPIO function Hardware Default value: 0: In LB mode 1: Others
2	Serial Port 1 System Clock Disable 1: Disabled Serial Port 1 system clock 0: Enabled Serial Port 1 system clock Hardware Default value: 1: In LB mode 0: Others
3	Serial Port 2 System Clock Disable 1: Disabled Serial Port 2 system clock 0: Enabled Serial Port 2 system clock Hardware Default value: 1: In LB mode 0: Others
4	Serial Port 3 System Clock Disable 1: Disabled Serial Port 3 system clock 0: Enabled Serial Port 3 system clock

	Hardware Default value: 1: In LB, PP or SPI mode 0: Others
5	Serial Port 4 System Clock Disable 1: Disabled Serial Port 4 system clock 0: Enable Serial Port 4 system clock Hardware Default value: 1: in LB, PP or SPI mode 0: Others
6	SPI System Clock Disable 1: Disabled SPI system clock 0: Enabled SPI system clock Hardware Default value: 0: In SPI mode. 1: Others
7	Reserved

Global Setting (0x56)

Bit	Description
3:0	PCIe Function Enable Indicates the function existed or not in PCIe system. Bit0 is for Function 1, Bit1 is for Function 2 and Bit2 is for function 3. Note Bit3 should be set to '0' and the Function 0 is always enabled in AX99100. 1: Enabled the corresponding PCIe Function. 0: Disabled the corresponding PCIe Function. Hardware Default value: 0x0: For LB mode (CHIP_MODE= 000) 0x3: For PP related mode (CHIP_MODE=001 and 010) 0x5: For SPI related mode (CHIP_MODE=100 and 110) 0x7: Others
4	ECRC forwarding to and from the Application Layer implemented. This field should always set to 0b
7:5	Reserved

Check-Sum (0x5B)

Bit	Description
7:0	Check-Sum Value Hardware Check-Sum verification is the sum of the all bytes from offset 0x00 to 0x5B with an 8bit adder and the carry need to be added back to bit0. The final value should equal to the Hardware pre-define, 0x79. So the Check-Sum value should be used to adjust the final value to 0x79 to pass the Check-Sum verification. If the check-sum verification failed, Hardware will not load the EEPROM contents and use the Hardware default value to replace it. Please reference section 3.3.3 in detail. For example, if the summation is 0x7A from offset 0x00 to 0x5A. Due to 0x7A is large than 0x79, the Check-Sum Value should be 0xFE (0x79-0x7A-0x01). If the summation is 0x79, Check-Sum Value will be 0x00 (0x79-0x79).

Reserved (0x5C-0x7F)

EEPROM address 0x5C~0x7F are Reserved.

3.3.2 Configuration EEPROM Memory Map for Local Bus Interface

Table 3-5: Configuration EEPROM Memory Map for Local Bus

EEPROM Offset	Parameter
0x00	Divide Clock Selection
0x01	Clock Divider
0x03~0x02	Vendor ID_F0
0x05~0x04	Device ID_F0
0x06	Revision ID
0x07	Programming IF_F0
0x08	Sub-Class Code_F0
0x09	Base Class Code_F0
0x0B~0x0A	Subsystem Vendor ID_F0
0x0D~0x0C	Subsystem Device ID_F0
0x0F~0x0E	Power Management Capabilities_F0
0x17~0x10	Reserved
0x19~0x18	Local Bus Interrupt Enable/Miscellaneous Setting
0x1B~0x1A	PCIe BAR0 Range
0x1D~0x1C	PCIe BAR1 Range
0x1F~0x1E	Reserved
0x21~0x20	Local Address Space 0 Setting
0x25~0x22	Local Address Space 0 Timing Setting
0x29~0x26	Local Address Space 0 Address Setting
0x2B~0x2A	Local Address Space 1 Setting
0x2F~0x2C	Local Address Space 1 Timing Setting
0x33~0x30	Local Address Space 1 Address Setting
0x54~0x34	INT Mask
0x55	Port Disable Register
0x56	Global Setting
0x5A~0x57	Reserved
0x5B	Check-Sum
0x7F ~ 0x5C	Reserved

Offset 0x00~0x16:

Please reference section 3.3.1.

Local Bus Interrupt Enable/Miscellaneous Setting (0x19~0x18)

Bit	Description
0	INT0 Wakeup Enable 1: Enable INT0 wakeup 0: Disable INT0 wakeup Hardware Default Value: 0x0
1	INT1 Wakeup Enable 1: Enable INT1 wakeup 0: Disable INT1 wakeup Hardware Default Value: 0x0
2	RDY Timeout Enable 1: Enables RDY timeout. 0: Disable RDY timeout. Hardware Default Value: 0x0
3	RDY Timeout Select 1: 128 clocks 0: 32 clocks Hardware Default Value: 0x0
4	Ready Polarity 1: Active high 0: Active low Hardware Default Value: 0x1
5	ALE Polarity 1: Active High 0: Active Low Hardware Default Value: 0x1
6	Synchronous Bus 1: Synchronous Bus 0: Asynchronous Bus Hardware Default Value: 0x0
7	Multiplexed Bus 1: Address and Data multiplexed 0: Address and Data bus separated Hardware Default Value: 0x0
8	CLKO Driven Strength 1: 8mA 0: 4mA Hardware Default Value: 0x1
9	CLKO Output Enable 1: Enable clock output 0: Disable clock output Hardware Default Value: 0x1

10	ALE Remap to A[10] 1: Re-assigned ALE pin to A[10], only valid when set bit7 to '0' 0: ALE pin is for ALE function Hardware Default Value: 0x0
11	Reserved
12	CLKO Output Invert 1: Bus cycle active with rising edge 0: Bus cycle active with falling edge Hardware Default Value: 0x0
13	Reserved
14	DREQ0 Wakeup Enable 1: Enable DREQ0 wakeup 0: Disable DREQ0 wakeup Hardware Default Value: 0x0
15	DREQ1 Wakeup Enable 1: Enable DREQ1 wakeup 0: Disable DREQ1 wakeup Hardware Default Value: 0x0

PCIe BAR0 Range (0x1B~0x1A)

Bit	Description
0	IO SPACE 1: Indicates Local Address Space 0 maps into I/O space. 0: Indicates Local Address Space 0 maps into Memory space. Hardware Default Value: 0x0
2:1	Space Decode When mapped into Memory space, the only valid value is 00. (32-bit access space with non-prefetchable) When mapped into I/O space, bit 1 should be '0' and bit 2 will be loaded to BADDR0[2] to indicate the decoding range. Hardware Default Value: 0x0
3	Prefetchable When mapped into Memory space, '1' indicates reads are prefetchable. When mapped into I/O space, this bit will be loaded to BADDR0[3] to indicate the decoding range. Hardware Default Value: 0x0
15:4	BADDR0[15:4] Specifies which Address bits to be used for decoding the PCIe access to Local Address Space 0. Each bit corresponds to Address bit. '1' is for PCI address decoding and '0' means the occupied range for the BAR0 access. The address bit 31 to 16 of BAR0 is always '1'. Hardware Default Value: 0x000 (64KByte)

PCIe BAR1 Range (0x1D~0x1C)

Bit	Description
0	IO SPACE 1: Indicates Local Address Space 0 maps into I/O space. 0: Indicates Local Address Space 0 maps into Memory space. Hardware Default Value: 0x0
2:1	Space Decode When mapped into Memory space, the only valid value is 00. (32-bit access space with non-prefetchable) When mapped into I/O space, bit 1 should be '0' and bit 2 will be loaded to BADDR1[2] to indicate the decoding range. Hardware Default Value: 0x0
3	Prefetchable When mapped into Memory space, '1' indicates reads are prefetchable. When mapped into I/O space, this bit will be loaded to BADDR1[3] to indicate the decoding range. Hardware Default Value: 0x0
15:4	BADDR1[15:4] Specifies which Address bits to be used for decoding the PCIe access to Local Address Space 1. Each bit corresponds to Address bit. '1' is for PCI address decoding and '0' means the occupied range for the BAR1 access. The address bit 31 to 16 of BAR1 is always '1'. Hardware Default Value: 0x000 (64KByte)

Local Address Space 0 Setting (0x21~0x20)

Bit	Description
0	INT0 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x0
1	INT0 Trigger Style 1: Level Trigger 0: Edge Trigger Hardware Default Value: 0x0
2	DREQ0 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x0
3	DACK0 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x1
4	Local Address Space 0 External Ready Control 1: External RDY control usage for Local Address Space 0 bus access 0: Internal counter used for Local Address Space 0 bus access Hardware Default Value: 0x0

5	Bus Endian and Alignment for Local Address Space 0 When data bus width is 16-bit, 1: Big endian 0: Little endian When data bus width is 8-bit, 1: Data place to/from DA[15:8] 0: Data place to/from DA[7:0] Hardware Default Value: 0x0
6	Data Bus Width for Local Address Space 0 1: Bus width 16-bit width 0: Bus width 8-bit width Hardware Default Value: 0x1
7	ALE Insertion Enable for Local Address Space 0 1: Enable ALE insertion 0: Disable ALE insertion Note: This bit should be set to '1' when bit7 of "Local Bus Interrupt Enable/Miscellaneous Setting", offset 0x19~0x18, is '1'. Hardware Default Value: 0x0
8	Chip Select (CS0n) Enable for Local address Space 0 1: Enable Local Address Space 0 Chip Select 0: Disable Local Address Space 0 Chip Select Hardware Default Value: 0x1
9	Local address Space 0 Enable 1: Enable the address mapping from PCIe BAR0 access to Local Address Space 0. 0: Disable the address mapping. Hardware Default Value: 0x1
11:10	Reserved Hardware Default Value: 0x3
12	Burst Read Enable for Local Address Space 0 1: Enable burst read access 0: Disable burst read access Hardware Default Value: 0x1
14:13	Reserved Hardware Default Value: 0x0
15	BAR0 Enable 1: Enable BAR0 access 0: Disable BAR0 access even offset 0x1B~0x1A, Local Bus PCIe BAR0 Range, are valid. Hardware Default Value: 0x1

Local Address Space 0 Timing Setting (0x25~0x22)

Bit	Description
3:0	ALE Pulse Width (ALE_PW) ALE pulse width cycle = (ALE_PW +1) * clock period Hardware Default Value: 0x0
5:4	Data and Address Setup Time (DA_SET) Address stable or ALE de-assert before RD_N or WR_N assert Address setup time = DA_SET * clock period Hardware Default Value: 0x0
7:6	Data and Address Hold Time (DA_HD) Address and data de-assert after RD_N or WR_N de-assert Address hold time = DA_HD * clock period Hardware Default Value: 0x0
11:8	Read Access Time (RD_ACC) For single access or burst read first cycle Read access time = (RD_ACC + 1) * clock period Hardware Default Value: 0x1
15:12	Burst Read Access Time (BRD_ACC) For burst read second and late cycle Burst read access time = (BRD_ACC + 1) * clock period Note: BRD_ACC should large than 0x0. Hardware Default Value: 0x1
19:16	Write Access Time (WR_ACC) Write access time = (WR_ACC + 1) * clock period Hardware Default Value: 0x0
23:20	Access GAP Time (AGAP) Access back to back time = (AGAP + 1) * clock period Hardware Default Value: 0x0
27:24	CS0n Space Range Local Address Space 0 Range for CS0n CS0n Space Range = $2^{(LCS0RAN + 1)}$ Hardware Default Value: 0xF
31:28	Reserved

Local Address Space 0 Address Setting (0x29~0x26)

Bit	Description
15:0	Local Address Space 0 address shift Base Hardware Default Value: 0x0000
31:16	CS0n space Starting Address Starting Address Shift of CS0n for Local Address Space 0 Hardware Default Value: 0x0000

Local Address Space 1 Setting (0x2B~0x2A)

Bit	Description
0	INT1 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x0
1	INT1 Trigger Style 1: Level Trigger 0: Edge Trigger Hardware Default Value: 0x0
2	DREQ1 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x0
3	DACK1 Polarity 1: Active High 0: Active Low Hardware Default Value: 0x1
4	Local address Space 1 External Ready control 1: External RDY control usage for Local Address Space 1 bus access 0: Internal counter used for Local Address Space 1 bus access Hardware Default Value: 0x0
5	Bus Endian and Alignment for Local Address Space 1 When data bus width is 16-bit, 1: Big endian 0: Little endian When data bus width is 8-bit, 1: Data place to/from DA[15:8] 0: Data place to/from DA[7:0] Hardware Default Value: 0x0
6	Data Bus Width for Local Address Space 1 1: Bus width 16-bit width 0: Bus width 8-bit width Hardware Default Value: 0x1
7	ALE Insertion Enable for Local Address Space 1 1: Enable ALE insertion 0: Disable ALE insertion Note: This bit should be set to ‘1’ when bit7 of “Local Bus Interrupt Enable/Miscellaneous Setting”, offset 0x19~0x18, is ‘1’. Hardware Default Value: 0x0
8	Chip Select (CS1n) Enable for Local address Space 1 1: Enable Local Address Space 1 Chip Select 0: Disable Local Address Space 1 Chip Select Hardware Default Value: 0x1

9	Local address Space 1 Enable 1: Enable the address mapping from PCIe BAR1 access to Local Address Space 1. 0: Disable the address mapping. Hardware Default Value: 0x1
11:10	Reserved Hardware Default Value: 0x3
12	Burst Read Enable for Local Address Space 1 1: Enable burst read access 0: Disable burst read access Hardware Default Value: 0x1
14:13	Reserved Hardware Default Value: 0x0
15	BAR1 Enable 1: Enable BAR1 access 0: Disable BAR1 access even offset 0x1D~0x1C, Local Bus PCIe BAR1 Range, are valid. Hardware Default Value: 0x1

Local Address Space 1 Timing Setting (0x2F~0x2C)

Bit	Description
3:0	ALE Pulse Width (ALE_PW) ALE pulse width cycle = (ALE_PW +1) * clock period Hardware Default Value: 0x0
5:4	Data and Address Setup Time (DA_SET) Address stable or ALE de-assert before RD_N or WR_N assert Address setup time = DA_SET * clock period Hardware Default Value: 0x0
7:6	Data and Address Hold Time (DA_HD) Address and data de-assert after RD_N or WR_N de-assert Address hold time = DA_HD * clock period Hardware Default Value: 0x0
11:8	Read Access Time (RD_ACC) For single access or burst read first cycle Read access time = (RD_ACC + 1) * clock period Hardware Default Value: 0x1
15:12	Burst Read Access Time (BRD_ACC) For burst read second and late cycle Burst read access time = (BRD_ACC + 1) * clock period Note: BRD_ACC should large than 0x0. Hardware Default Value: 0x1
19:16	Write Access Time (WR_ACC) Write access time = (WR_ACC + 1) * clock period Hardware Default Value: 0x0
23:20	Access GAP Time (AGAP) Access back to back time = (AGAP + 1) * clock period Hardware Default Value: 0x0

27:24	CS1n space Range Local Address Space 1 Range for CS1n CS1n Space Range = $2^{(LCS1RAN + 1)}$ Hardware Default Value: 0xF
31:28	Reserved

Local Address Space 1 Address Setting (0x33~0x30)

Bit	Description
15:0	Local Address Space 1 address shift Base Hardware Default Value: 0x0000
31:16	CS1n space Starting Address Starting Address Shift of CS1n for Local Address Space 0 Hardware Default Value: 0x0000

Offset 0x53~0x7F:

Please reference section 3.3.1.

3.3.3 Hardware Default Values Summary

This section summarizes all hardware default values in section 3.3.1 and 3.3.2.

Table 3-6: Hardware Default Values in each CHIP_MODE Setting

	CHIP_MODE			
EEPROM offset	**LB(000)**	**2S1P(001), 2MP1P(010)**	**4S(011), 4MP(111), 2S2MP(101)**	**2S1SPI(110), 2MP1SPI(100)**
0x00	05	00	00	05
0x01	02	00	00	02
0x02	5B	5B	5B	5B
0x03	12	12	12	12
0x04	10	00	00	00
0x05	91	91	91	91
0x06	00	00	00	00
0x07	00	02	02	02
0x08	80	00	00	00
0x09	06	07	07	07
0x0A	00	00	00	00
0x0B	A0	A0	A0	A0
0x0C	00	00	00	00
0x0D	70	10	10	10
0x0E	FF	FF	FF	FF
0x0F	07	07	07	07
0x10	01	01	01	01
0x11	00	00	00	00
0x12	02	02	02	02
0x13	83	83	83	83
0x14	FD	FD	FD	FD
0x15	41	31	31	31
0x16	01	01	01	01
0x17	00	5B	5B	5B
0x18	30	12	12	12
0x19	03	00	00	00
0x1A	00	91	91	91
0x1B	00	02	02	02
0x1C	00	00	00	00
0x1D	00	07	07	07
0x1E	00	00	00	00
0x1F	00	A0	A0	A0
0x20	48	00	00	00
0x21	9F	10	10	10
0x22	00	FF	FF	FF
0x23	11	07	07	07
0x24	00	11	11	11
0x25	0F	00	00	00
0x26	00	02	02	02
0x27	00	83	83	83
0x28	00	FD	FD	FD
0x29	00	31	31	31

	CHIP_MODE			
EEPROM offset	LB(000)	2S1P(001), 2MP1P(010)	4S(011), 4MP(111), 2S2MP(101)	2S1SPI(110), 2MP1SPI(100)
0x2A	48	02	02	02
0x2B	9F	5B	5B	FF
0x2C	00	12	12	FF
0x2D	11	00	00	FF
0x2E	00	91	91	FF
0x2F	0F	03	02	00
0x30	00	01	00	00
0x31	00	07	07	00
0x32	00	00	00	00
0x33	00	A0	A0	00
0x34	00	00	00	00
0x35	00	20	10	00
0x36	00	FF	FF	00
0x37	00	07	07	00
0x38	00	11	11	00
0x39	00	00	00	00
0x3A	00	02	02	00
0x3B	00	83	83	00
0x3C	00	FD	FD	00
0x3D	00	31	31	00
0x3E	00	03	03	00
0x3F	00	FF	5B	5B
0x40	00	FF	12	12
0x41	00	FF	00	00
0x42	00	FF	91	91
0x43	00	00	02	00
0x44	00	00	00	00
0x45	00	00	07	FF
0x46	00	00	00	00
0x47	00	00	A0	A0
0x48	00	00	00	00
0x49	00	00	10	60
0x4A	00	00	FF	FF
0x4B	00	00	07	07
0x4C	00	00	11	11
0x4D	00	00	00	00
0x4E	00	00	02	02
0x4F	00	00	83	83
0x50	00	00	FD	FD
0x51	00	00	31	31
0x52	00	00	04	04
0x53	01	21	21	21
0x54	00	04	84	80
0x55	7C	72	42	32
0x56	00	03	07	05
0x57	00	E4	E4	E4
0x58	00	00	00	00

	CHIP_MODE			
EEPROM offset	**LB(000)**	**2S1P(001), 2MP1P(010)**	**4S(011), 4MP(111), 2S2MP(101)**	**2S1SPI(110), 2MP1SPI(100)**
0x59	00	00	00	00
0x5A	00	00	00	00
0x5B	-	-	-	-

3.3.4 Disable Unused PCIe Function in HWCFGEE

The AX99100 supports to disable the unused PCIe function via **HWCFGEE**. For example, if user would like to use one Serial Port and hope AX99100 just occupy only one PCIe function (**1S**) in system. User can set **CHIP_MODE** = 011b to select **4S** mode and use the proper setting in **HWCFGEE** to disable PCIe function 1~3. Following descriptions will introduce how to fill the **HWCFGEE** content to disable PCIe function.

※ Set the field of "Vendor ID" and "Device ID" to 0xFFFF in the corresponding PCIe function which would like to be disabled.
※ Set others fields to 0x00 in the corresponding PCIe function which would like to be disabled.
※ Set '1' to disable the corresponding function in offset 0x55, bit 2~6.
※ Set '0x0' to bit15:4 for those unused Functions in offset 0x54~0x33.
※ Set '0' to bit3:0 to disable those unused Functions in offset 0x56.

Notice:

◎ The PCIe function 0 can't be disabled.
◎ If PCIe function 1 or 3 disabled, the Serial Port GPIO of function 0 or 2 will be redirected to the IO of Serial Port 2 and 4 in Serial Port related **CHIP_MODE** setting. Please reference section 1.4.5.
◎ If PCIe function 3 disabled, the IO of Port 4 will be redirected to GPIO in SPI related CHIP_**MODE** setting.

Following table show an example for configuring AX99100 to 1S mode in CHIP_**MODE** = 011 (**4S**). The PCIe function 1~3 will be disabled via **HWCFGEE**.

Table 3-7: The HWCHGEE content for 1S setting

EEPROM offset	CHIP_MODE = 011 (4S)	PCIe Function No.
0x00	00	
0x01	00	
0x02	5B	Function 0
0x03	12	
0x04	00	
0x05	91	
0x06	00	
0x07	02	
0x08	00	
0x09	07	
0x0A	00	
0x0B	A0	
0x0C	00	
0x0D	10	
0x0E	FF	
0x0F	07	
0x10	01	
0x11	00	
0x12	02	
0x13	83	
0x14	FD	
0x15	31	
0x16	01	
0x17	FF	Function 1
0x18	FF	
0x19	FF	

EEPROM offset	CHIP_MODE = 011 (4S)	PCIe Function No.
0x1A	FF	
0x1B	00	
0x1C	00	
0x1D	00	
0x1E	00	
0x1F	00	
0x20	00	
0x21	00	
0x22	00	
0x23	00	
0x24	00	
0x25	00	
0x26	00	
0x27	00	
0x28	00	
0x29	00	
0x2A	00	
0x2B	FF	Function 2
0x2C	FF	
0x2D	FF	
0x2E	FF	
0x2F	00	
0x30	00	
0x31	00	
0x32	00	
0x33	00	
0x34	00	
0x35	00	
0x36	00	
0x37	00	
0x38	00	
0x39	00	
0x3A	00	
0x3B	00	
0x3C	00	
0x3D	00	
0x3E	00	
0x3F	FF	Function 3
0x40	FF	
0x41	FF	
0x42	FF	
0x43	00	
0x44	00	
0x45	00	
0x46	00	
0x47	00	

EEPROM offset	CHIP_MODE = 011 (4S)	PCIe Function No.
0x48	00	
0x49	00	
0x4A	00	
0x4B	00	
0x4C	00	
0x4D	00	
0x4E	00	
0x4F	00	
0x50	00	
0x51	00	
0x52	00	
0x53	01	
0x54	00	
0x55	7A	
0x56	00	
0x57	E4	
0x58	00	
0x59	00	
0x5A	00	
0x5B	A2	

3.4 PCIe Configuration Space Map

Following tables show the BAR usages in different interfaces. The detail function description, please reference in **PCIe base specification Revision 1.1**. About the interrupt mapping in chip default, the function 0~3 will be mapped to INTA~D.

PCI Configuration Space Map for SP (Function 0~3)

Offset	Register Name			
	31 24	23 16	15 8	7 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C				
0x10	Base Address Registers 0			
0x14	Base Address Registers 1			
0x18				
0x1C				
0x20				
0x24	Base Address Registers 5			
0x28				
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30				
0x34				
0x38				
0x3C			Interrupt Pin	Interrupt Line

PCI Configuration Space Map for PP (Function 2)

Offset	Register Name			
	31 24	23 16	15 8	7 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C				
0x10	Base Address Registers 0			
0x14	Base Address Registers 1			
0x18	Base Address Registers 2			
0x1C				
0x20				
0x24	Base Address Registers 5			
0x28				
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30				
0x34				
0x38				
0x3C			Interrupt Pin (0x03)	Interrupt Line

PCI Configuration Space Map for SPI (Function 3)

Offset	Register Name															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	Device ID																Vendor ID															
0x04	Status																Command															
0x08	Class Code																								Revision ID							
0x0C																																
0x10	Base Address Registers 0																															
0x14	Base Address Registers 1																															
0x18																																
0x1C																																
0x20																																
0x24	Base Address Registers 5																															
0x28																																
0x2C	Subsystem ID																Subsystem Vendor ID															
0x30																																
0x34																																
0x38																																
0x3C																	Interrupt Pin (0x04)								Interrupt Line							

PCI Configuration Space Map for LB (Function 0)

Offset	Register Name															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	Device ID																Vendor ID															
0x04	Status																Command															
0x08	Class Code																								Revision ID							
0x0C																																
0x10	Base Address Registers 0																															
0x14	Base Address Registers 1																															
0x18																																
0x1C																																
0x20	Base Address Registers 4																															
0x24	Base Address Registers 5																															
0x28																																
0x2C	Subsystem ID																Subsystem Vendor ID															
0x30																																
0x34																																
0x38																																
0x3C																	Interrupt Pin (0x01)								Interrupt Line (0x00)							

4 Electrical Specifications

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCCK	Digital core power supply.	- 0.5 to 1.6	V
VCCIO, VCC33A_REG	Power supply of 3.3V I/O and Regulator.	- 0.5 to 4.6	V
VCC12A_TX, VCC12A_AUX, VCC12A_D	Analog power supply for PCIe PHY.	- 0.5 to 1.6	V
V_{IN}	Input voltage of 3.3V I/O with 5V tolerant.	- 0.5 to 5.8	V
T_{STG}	Storage temperature.	- 65 to 150	℃
I_{IN}	DC input current.	50	mA
I_{OUT}	Output short circuit current.	50	mA

Note:
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

4.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
VCCIO	Power supply of 3.3V I/O.	2.97	3.3	3.63	V
VCCK	Digital core power supply.	1.08	1.2	1.32	V
VCC33A_REG	Analog power supply for Regulator.	2.0	3.3	3.6	V
VCC12A_TX, VCC12A_AUX, VCC12A_D	Analog power supply for PCIe PHY.	1.14	1.2	1.26	V
Tj	AX99100 QF operating junction temperature. AX99100 QI operating junction temperature.	0 -40	25	125 125	℃
Ta	AX99100 QF operating ambient temperature. AX99100 QI operating ambient temperature.	0 -40	-	70 85	℃

4.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V with 5V tolerant I/O pins. Vin = 5 or 0V.	-	< ±1	-	μA
C_{IN}	Input capacitance.	3.3V with 5V tolerant I/O pins.	-	2.3	-	pF

4.1.4 DC Characteristics of 3.3V with 5V Tolerant I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCCIO	Power supply of 3.3V I/O.	3.3V I/O	2.97	3.3	3.63	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage.	Iol = 2 ~ 4mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = -2 ~ -4mA	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	VCCIO – 0.9	-	-	V
Rpu	Input pull-up resistance.		40	75	190	KΩ
Rpd	Input pull-down resistance.		40	75	190	KΩ
Iin	Input leakage current.	Vin = 5 or 0V	-	±1	-	μA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	μA
	Input leakage current with pull-down resistance.	Vin = VCCIO	-	45	-	μA

Note: This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VCCIO DC level even without DC loading current.

4.1.5 DC Characteristics of Voltage Regulator

Symbol	Description	Condition	Min	Typ	Max	Unit
VCC33A_REG	Power supply of on-chip voltage regulator.		2.0	3.3	3.6	V
VO12	Output voltage of on-chip voltage regulator.	VCC33A_REG = 3.3V	1.14	1.2	1.26	V
Tj	Operating junction temperature.		-40	25	125	℃
I_{load}	Driving current.	VCC33A_REG = 3.3V	-	-	150	mA
$\frac{\triangle VO12}{(\triangle VCC33A\_REG \times VO12)}$	Line regulation.	I_{load} = 10mA	-	0.5	1.0	%/V
$\frac{\triangle VO12}{(\triangle I_{load} \times VO12)}$	Load regulation.	VCC33A_REG = 3.3V, 1mA ≦ I_{load} ≦ 150mA	-	0.05	0.1	%/mA
$\frac{\triangle VO12}{\triangle Tj}$	Temperature coefficient.	VCC33A_REG = 3.3V, -40℃ ≦ Tj ≦ 125℃	-	0.1	0.3	mV/℃
I_Q	Quiescent current consumption	VCC33A_REG = 3.3V, I_{load} = 0 mA	-	110	310	μA
Cout	Output external capacitor.		3.3	-	-	μF
ESR	Allowable effective series resistance of external capacitor.		0.5	-	-	Ω

4.2 PCIe Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
UI	Unit Interval	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations	399.88	400	400.12	ps
Input Levels						
$V_{RX-DIFF-PP}$	Differential RX peak-peak voltage	$2*\|V_{RX(DIP)}-V_{RX(DIN)}\|$, measured at the connection of the near-end receiver	175	-	1200	mV
V_{IDLE}	Electrical idle detect threshold	Peak voltage	65	-	175	mV
$V_{RX-CM-AC}$	RX AC common-mode voltage	Peak voltage	-	-	150	mV
T_{RX-EYE}	Minimum Receiver Eye Width		0.4	-	-	UI
$RL_{RX-DIFF}$	Differential Return Loss	Measured over 50 MHz to 1.25 GHz.	10	-	-	dB
RL_{RX-cm}	Common Mode Return Loss	Measured over 50 MHz to 1.25 GHz.	6	-	-	dB
Output Levels						
$V_{TX-DIFF-PP}$	Differential TX peak-peak voltage swing	$2*\|V_{TX(DOP)}-V_{TX(DON)}\|$, measured at the connection of the near-end transmitter	800	-	1200	mV
T_{TX-EYE}	Transmitter eye, including all jitter sources	SSC or Refclk jitter is not included	0.75	-	-	UI
$V_{TX-IDLE-AC}$	Electrical idle differential peak output voltage		-	-	20	mV
V_{T-D-R}	Amount of voltage change allowed during the receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	600	mV
$V_{TX-CM-AC}$	TX AC common-mode voltage	Measured as the AC RMS value	-	-	20	mV
$V_{TX-DEM-ratio}$	TX de-emphasis level	Non-transient bits are driven out with degrading amplitude	-3.0	-	-4.0	dB
F_{BEACON}	A signal of wakeup mechanism	Signal frequency	2.0	-	15	MHz
Resistance						
R_{RX}	Built-in receiver input impedance		40	50	60	Ω
R_{TX}	Built-in driver output impedance		40	50	60	Ω
Capacitance						
C_{TX}	AC coupling capacitor		75	-	200	nF

4.3 Power Consumption

Interface	Configuration	Loading	Condition	VCCIO	VCCK	VCC12A_TX	VCC12A_D	VCC12A_AUX	Unit
4S	L0	Idle		2.5	36.7	12	19.2	17.1	mA
		Full load	4 Serial Ports with 25Mhz Baud Rate	5.5	53.3	12	19.2	17.1	mA
	L1			0	30.8	2.8	16.2	12.5	mA
	L2			1.2	0.1	3.6	0.7	8.3	mA
	ASPM L0s	Idle		3.1	35.6	13.2	17.7	14.8	mA
		Full load	4 Serial Ports with 25Mhz Baud Rate	4.6	51.8	13.2	17.7	16.4	mA
LB	L0	Idle		5.9	35.9	12.6	18.8	14.6	mA
		Full load	Synchronous 16-bit Multiplexed Bus with 62.5MHz Local Bus clock	24.7	38.1	12.6	18.8	14.6	mA
	L1			5.5	34.4	10.7	17.0	12.2	mA
	L2			1.0	0.0	3.79	0.5	8.6	mA
	ASPM L0s	Idle		4.9	30.0	13.4	16.9	15.7	mA
		Full load		24.0	36.7	13.4	16.9	15.7	mA

Note: The measurement is for the operation at Typical Condition and used ASIX 4S and Local Bus test board.

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	11.9	-	℃/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	28.3	-	℃/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	0.30	-	℃/W

4.4 Power–up/down and Power Management Sequence

The AX99100 related power up/down and power management sequences are designed to meet the **PCI Express Card Electromechanical Specification Revision 2.0**. Please reference the section 2.2.1 for power up sequence, section 2.2.2 for power management sequence and section 2.2.3 for power down sequence for the detail in this standard.

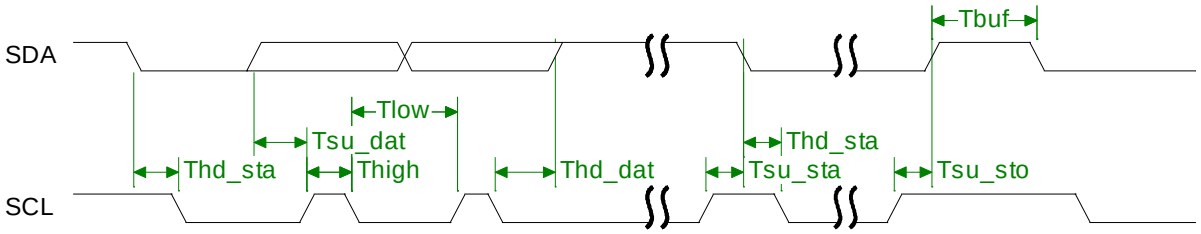
Note: There is NO power plane separation between 3.3V AUX and VCCIO in AX99100. In D3 Cold, the chip VCCIO and VCC33A_REG should be powered from 3.3V AUX to support remote wake up.

4.5 AC Timing Characteristics

4.5.1 PCIe Reference Clock Timing

The reference clock (CLKP and CLKN) of AX99100 is designed for the **PCI Express Card Electromechanical Specification Revision 2.0**. Please reference the section 2.1.3 in this standard for the detail.

4.5.2 I²C Timing



Symbol	Parameter	Min	Typ	Max	Units
Fclk[2]	SCL clock frequency SCL will use 100KHz during the configuration EEPORM loading and can be changed to support 400KHz operating.	-	-	100, 400	KHz
Thigh	High period of the SCL clock	-	SCL_HP+5	-	Tsys_clk[1]
Tlow	Low period of the SCL clock	-	SCL_LP+2	-	Tsys_clk
Thd_sta	Hold time of (repeated) START condition. After this period, the first clock pulse is generated	-	SHSC+1	-	Tsys_clk
Tsu_sta	Setup time for a repeated START condition	-	SHSC+1	-	Tsys_clk
Tsu_dat	Data Setup time	-	(SCL_LP/2)+1	-	Tsys_clk
Thd_dat	Data hold time	-	(SCL_LP/2)+1	-	Tsys_clk
Tsu_sto	Setup time for STOP condition	-	SCL_HP+5	-	Tsys_clk
Tbuf	Bus free time between a STOP and START condition	-	(SCL_HP/2)+BFT+2	-	Tsys_clk

Note 1: Tsys_clk = 16ns for 62.5 MHz operating system clock.
Note 2: Fclk = 1/Tclk, where Tclk = ((SCL_HP + SCL_LP) * Tsys_clk). The SCL_HP and SCL_LP are I²C SCL Period Register.

Table 4-1: I²C Master Controller Timing Table

4.5.3 Serial Port Timing

The Serial Port data transmit and receive is via TXD[4:1] and RXD[4:1] pins. The complete data transmit/receive includes 1 start bit, 5~8 data bit, 1 parity bit (if supported parity check) and 1~2 stop bit.

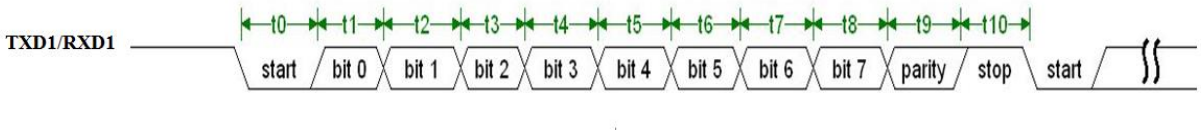
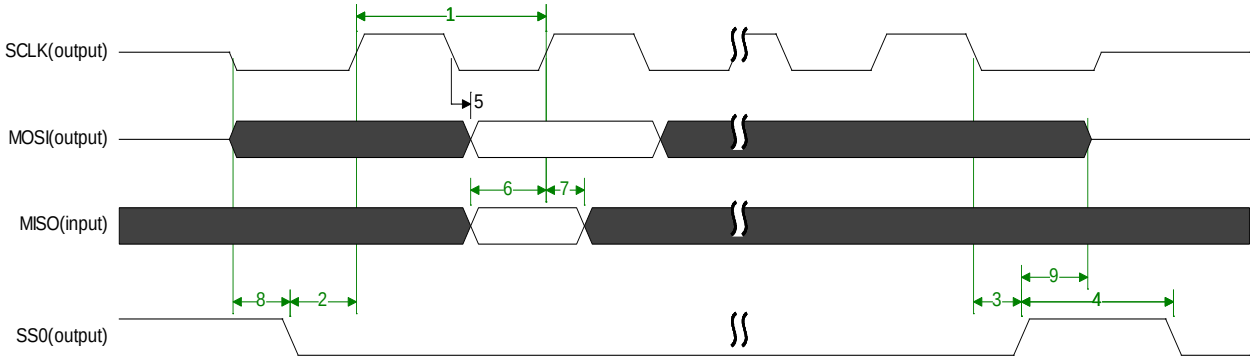


Figure 4-1: TXD1 and RXD1 Timing Diagram

Symbol	Parameter	Min	Typ	Max	Units
t0~t9	t0 is start bit time; t1 ~ t8 is data bit time; t9 is parity bit time;	-	1/Baud Rate		S
t10	stop bit time : 1 bit 1.5 bit 2 bit	-	 1/Baud Rate 1.5*(1/Baud Rate) 2*(1/Baud Rate)	-	S

Note: RXD[4:1] baud rate tolerance ±3%.

4.5.4 SPI Timing



Symbol	Description	Min	Typ	Max	Units
1	SCLK clock frequency	-	$\frac{\text{Fsys\_clk}}{\text{SPIBRR}}$	-	MHz
2	Setup time of SS[2:0] to the first SCLK edge	-	Mode0, 1: (1.0 + DBS) * Tsclk. Mode2, 3: (0.5 + DBS) * Tsclk.	-	ns
3	Hold time of SS[2:0] after the last SCLK edge	-	Mode0, 1: (0.5 + DBS) * Tsclk. Mode2, 3: (1.0 + DBS) * Tsclk.	-	ns
4	Minimum idle time between transfers (minimum SS[2:0] high time)	-	(2 + DT) * Tsclk.	-	ns
5	MOSI data valid time, after SCLK edge	-	-	2	ns
6	MISO data setup time before SCLK edge	7	-	-	ns
7	MISO data hold time after SCLK edge	0	-	-	ns
8, 9	Bus drive time before SS[2:0] assertion and after SS[2:0] de-assertion	-	Tsclk	-	

Note: Fsys_clk is from 125MHz, 100MHz or EXT_CLK and the SCLK frequency is same as "Desired clock frequency". Please reference section 3.3.1, Divide Register. The SPIBRR is SPI Baud Rate Register and same as N.

Figure 4-2: High Speed SPI Master Controller Timing Diagram and Table

4.5.5 Local Bus Timing

4.5.5.1 Synchronous Bus Mode

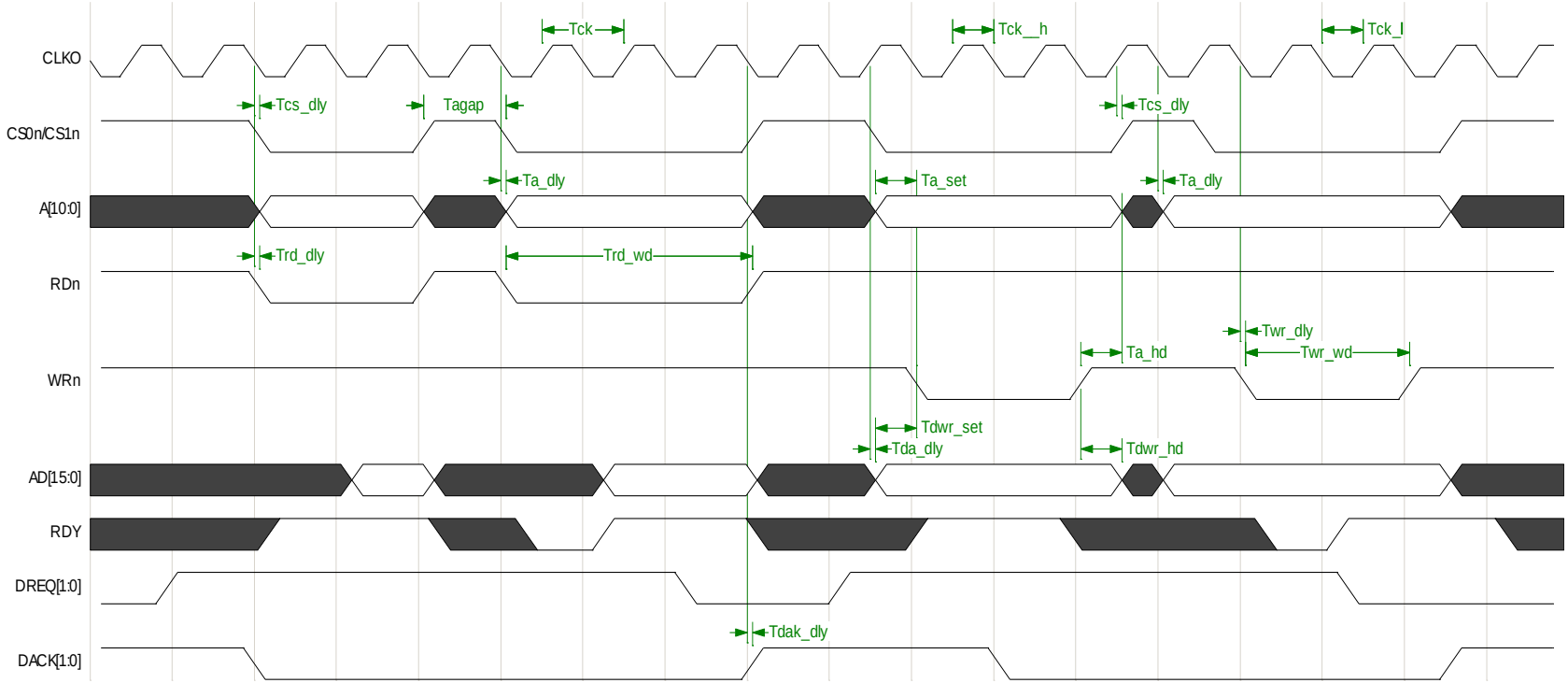


Figure 4-3: Non-multiplexed Bus Type with External RDY Timing Diagram

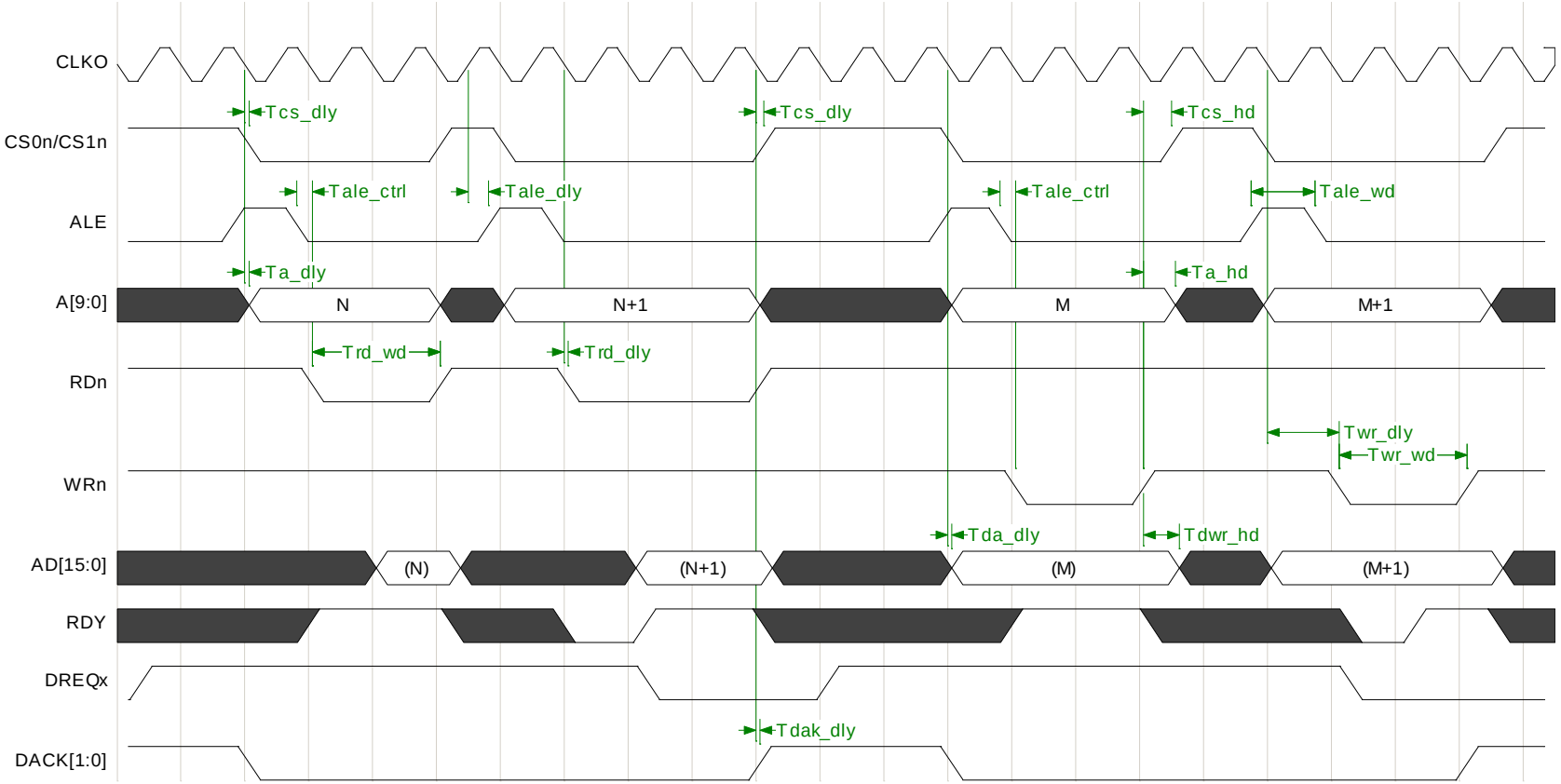


Figure 4-4: ISA-Like Bus Type with External RDY Timing Diagram

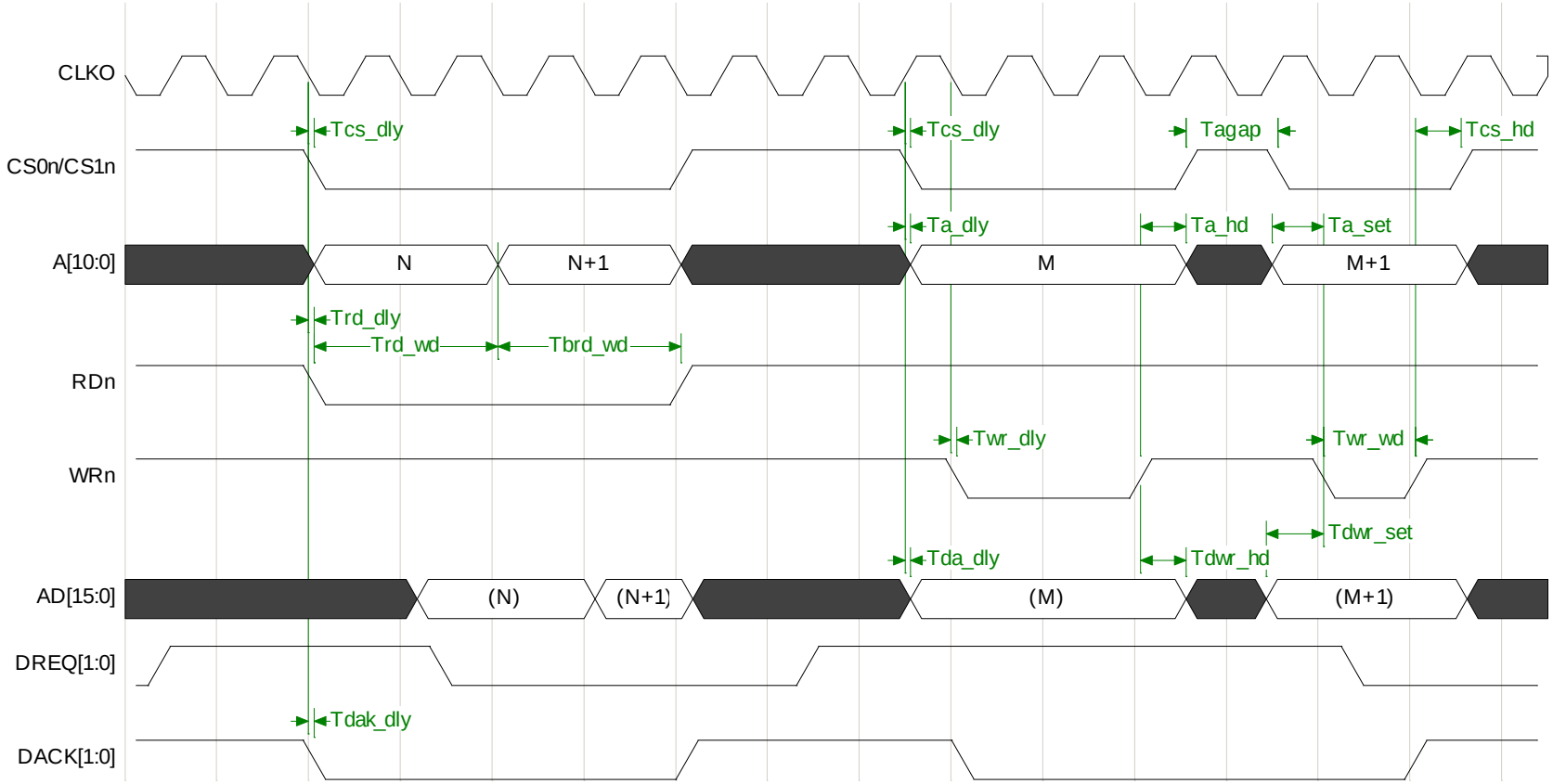


Figure 4-5: Non-multiplexed Bus type with internal cycle count Timing Diagram

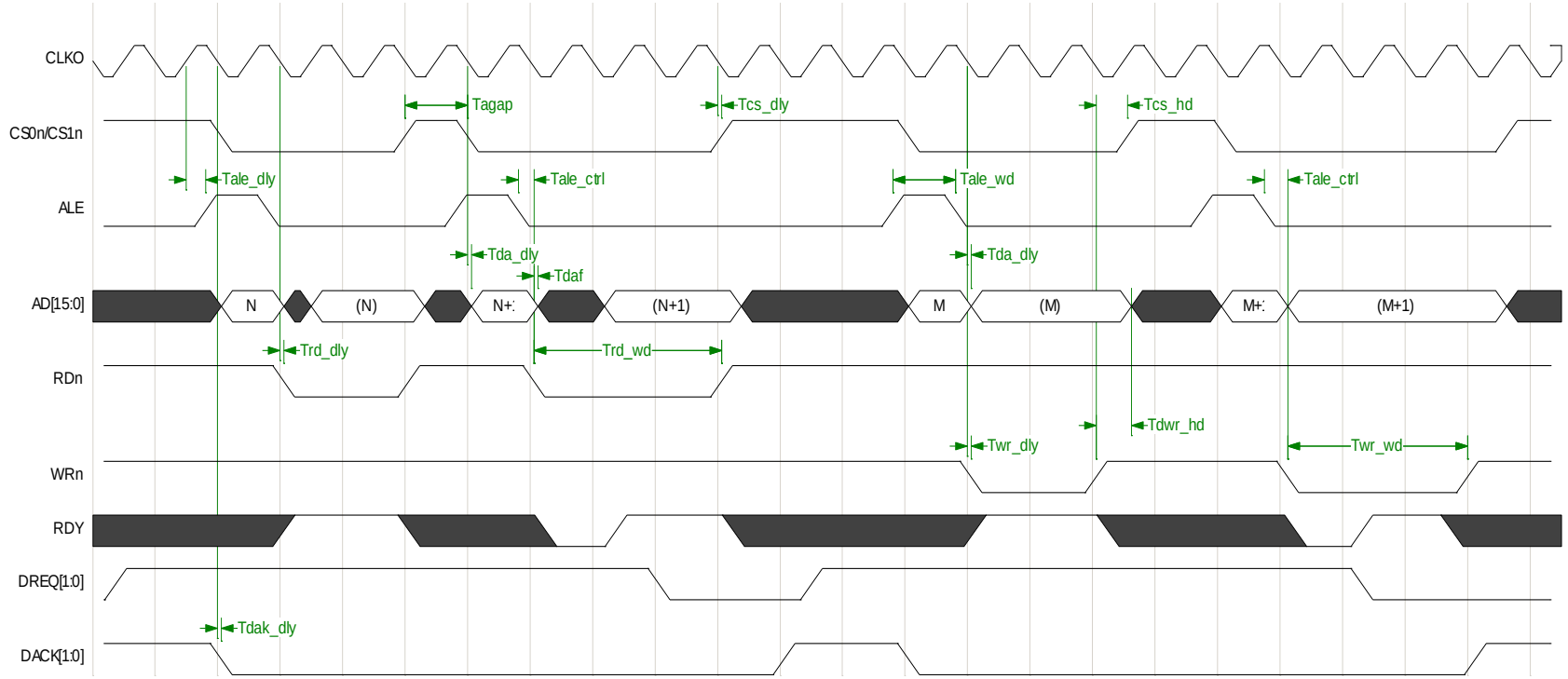


Figure 4-6: Multiplexed Bus type with external RDY Timing Diagram

4.5.5.2 Asynchronous Bus Mode

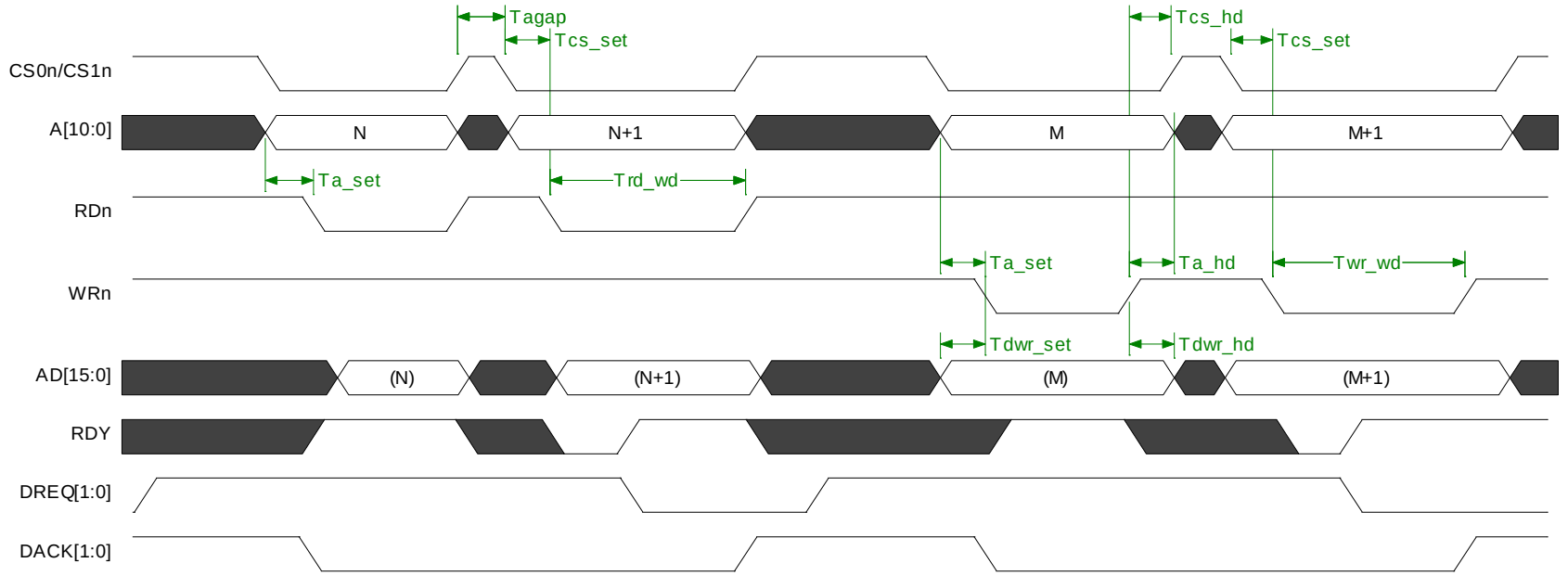


Figure 4-7: Non-multiplexed Bus Type with External RDY Timing Diagram

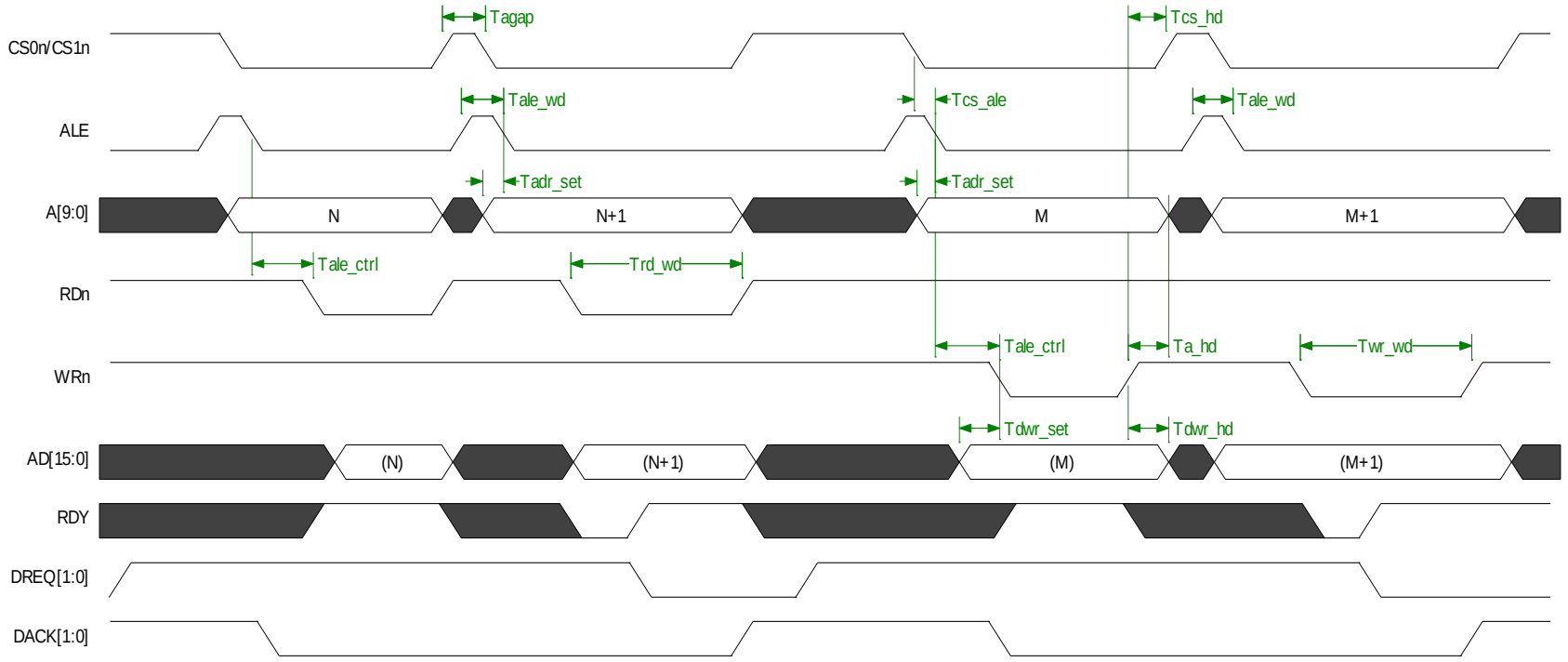


Figure 4-8: ISA-Like Bus Type with External RDY Timing Diagram

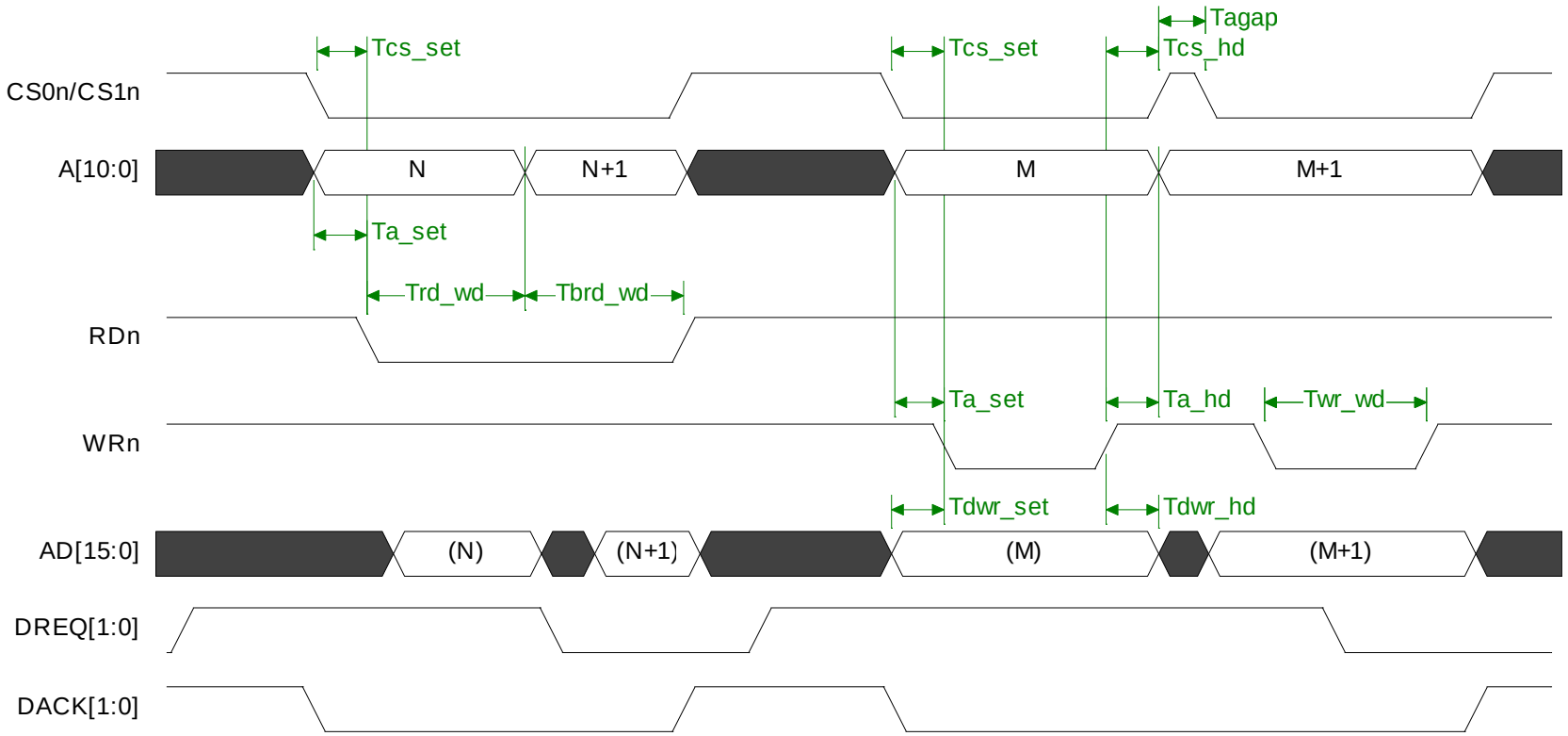


Figure 4-9: Non-multiplexed Bus type with internal cycle count Timing Diagram

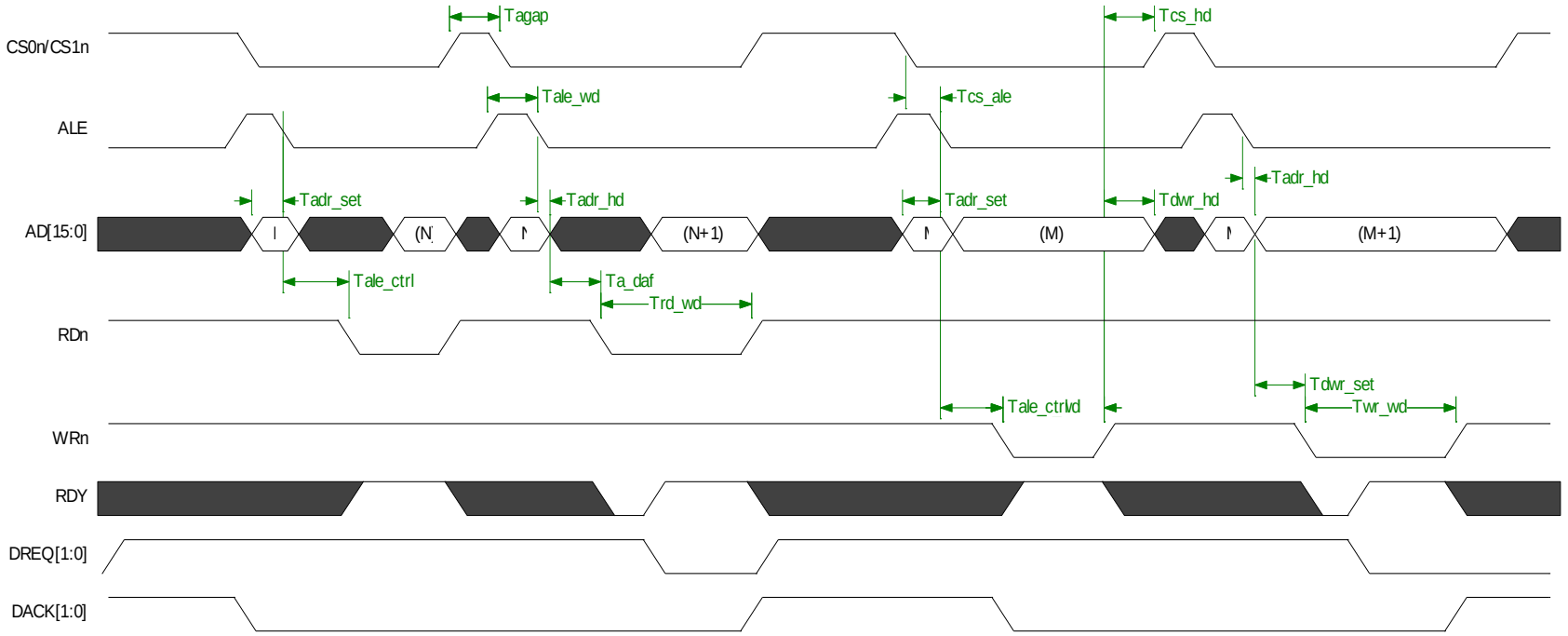
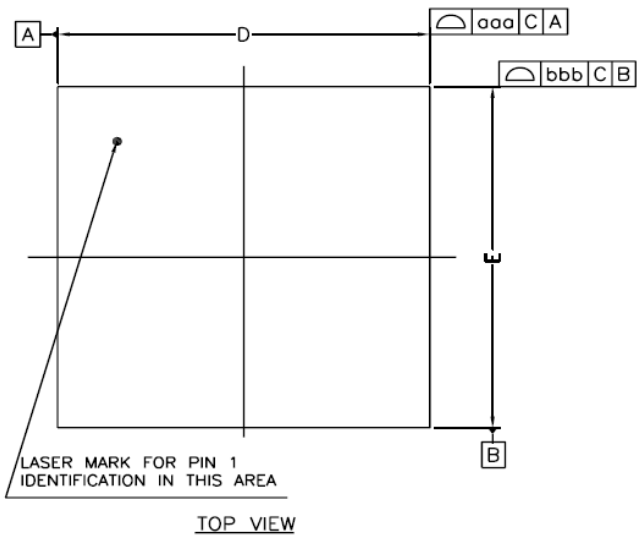


Figure 4-10: Multiplexed Bus type with external RDY Timing Diagram

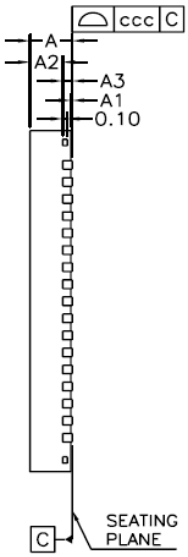
Symbol	Description	Min	Typ	Max	Units
Clock					
Tck	Clock Period	16	-	-	ns
Tck_h	Clock Low Time	-	Tck/2-1	-	ns
Tck_l	Clock High Time	-	Tck/2-1	-	ns
Tck_ris	Clock Rising Time	-	1	-	ns
Tck_fall	Clock Falling Time	-	1	-	ns
Bus Timing					
Tcs_dly	Chip Select Delay	0.2		1	ns
Tcs_set	Chip Select Setup Time Chip Select active to Read/Write active	-0.2	-	Tck/2+0.2	ns
Tcs_hd	Chip Select Hold Time Write inactive to Chip Select inactive	Tck/2-1.3	-	Tck*DA_HD	ns
Tale_ctrl	ALE to control active ALE inactive to read or write active	Tck/4-0.2	-	Tck*DA_SET-0.1	ns
Tale_dly	ALE Delay	Tck/4+0.3	-	Tck/4+1	ns
Tale_wd	ALE Width	-	Tck*(ALE_PW+1)	-	ns
Trd_dly	Read Delay	0.1	-	1	ns
Trd_wd	Read Width	-	Tck*(RD_ACC+1) , or RDY active, or RDY timeout	-	ns
Tbrd_wd	Burst Read Width	-	Tck*(BRD_ACC+1)	-	ns
Twr_dly	Write Delay	0.3	-	1	ns
Twr_wd	Write Width	-	Tck*(WR_ACC+1), RDY active or RDY timeout	-	ns
Tagap	Access Gap	Tck*(AGAP+1)	-	-	ns
Ta_dly	Address Delay	-	-	0.5	ns
Tcs_ale	ALE with Chip Select Chip Select active to ALE inactive	-	Tck/4 + 0.1	-	ns
Ta_set	Address Setup Address valid to Read/Write active	0.4	Tck*DA_SET	-	ns
Ta_hd	Address hold Write inactive to Address invalid	Tck/2	-	Tck*DA_HD	ns
Tadr_set	Address Setup Address valid to ALE inactive	Tck*(ALE_PW+3/4)	-	Tck*(ALE_PW+3/4)+1.1	ns
Tadr_hd	Address Hold ALE inactive to Address invalid	Tck/4 - 1.2	-	Tck/4	ns
Tda_dly	Data bus Delay	-0.5	-	0.5	ns
Tdaf	Data Float Read active to Data bus float	-1.1	-	0.2	ns
Tdwr_set	Data Write Setup Data valid to Write active	0.4	-	Tck*DA_SET	ns
Tdwr_hd	Data Write Hold Write inactive to Data invalid (bus floating)	Tck/2	-	Tck*DA_HD	ns
Trdy_set	RDY Setup	0	-	-	ns
Tdak_dly	DACK[1:0] Delay	0	-	0.6	ns
Tint_wd	INT[1:0] Width	Tck*2	-	-	ns

Table 4-2: Local Bus Timing Table

5 Package Information

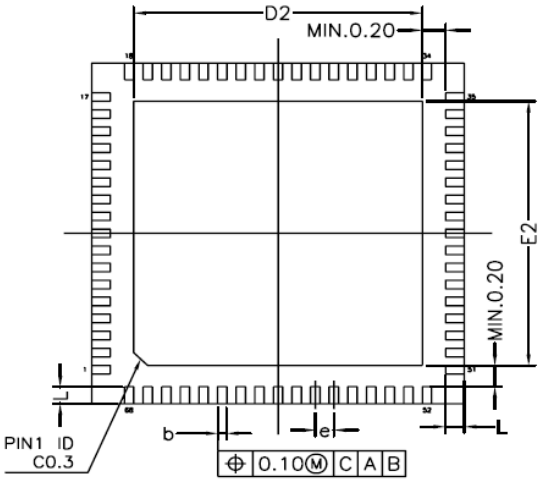


TOP VIEW



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.67	---	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.05	0.311	0.315	0.317
D2	4.20	4.30	4.40	0.165	0.169	0.173
E	7.90	8.00	8.05	0.311	0.315	0.317
E2	4.20	4.30	4.40	0.165	0.169	0.173
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		



BOTTOM VIEW

SIDE VIEW

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

6 Ordering Information

Part Number	Description
AX99100 QF	68-pin QFN lead Free package, commercial temperature range: 0 to 70℃.
AX99100 QI	68-pin QFN lead Free package, Industrial temperature range: -40 to 85℃.

7 Revision History

Revision	Date	Comments
V0.20	2016/04/18	Preliminary release.
V0.21	2016/04/22	1. Added some descriptions for offset 0x55 bit2~6 in Section 3.3.1. 2. Changed offset 0x20 and 0x2A, Active 0/1 to Low/High in Section 3.3.2. 3. Added offset 0x5A~0x56 as Reserved fields in Section 3.3.2. 4. Added some descriptions for Local Address Space 0/1 Timing Setting, Local Address Space 0/1 Address Setting in Section 3.3.2.
V0.22	2016/04/29	1. Changed offset 0x14 from 0xFF to 0xFD, offset 0x58 from 1 to 00 and offset 0x5B from 0x9F to 0xA2 in Table 3-7. 2. Added offset 0x53 ~ 0x54 and 0x56 in Table 3-4, Table 3-5 and section 3.3.1. 3. Added more descriptions in section 3.3 and 3.3.4.
V0.23	2016/05/06	1. Changed the offset 0x56 naming from “PCIe Function Enable” to “Global Setting” in Table 3-4 and Table 3-5.
V0.24	2016/06/06	1. Changed the offset 0x58 from 0x01 to 0x00 for LB mode in Table 3-6. 2. Changed bit11:10 to “Reserved” for offset 0x21~0x20 and 0x2B~0x2A in section 3.3.2.

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