T-75-37-05

Microchip

AY31015D

UAR/T: UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

FEATURES

- DTL and TTL compatible - no interfacing circuits required - drives one TTL load
- Fully Double Buffered - eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation - can handle multiple bauds (receiving - transmitting) simultaneously
- Start Bit Verification - decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs - bus structure capability
- Low Power - minimum power requirements
- Input Protected - eliminates handling problems
- Single Supply Operation: +4.75V to +5.25V
- 1 1/2 stop bit mode
- External reset of all registers except control bits register
- N-channel Ion Implant Process
- 0 to 25K baud
- Pull-up resistors to Vcc on all inputs

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, 1, 1-1/2, or 2 stop bit capability, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

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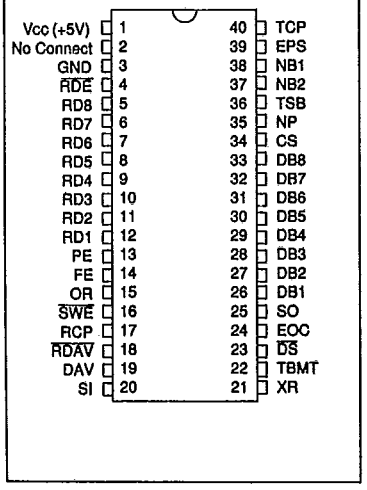
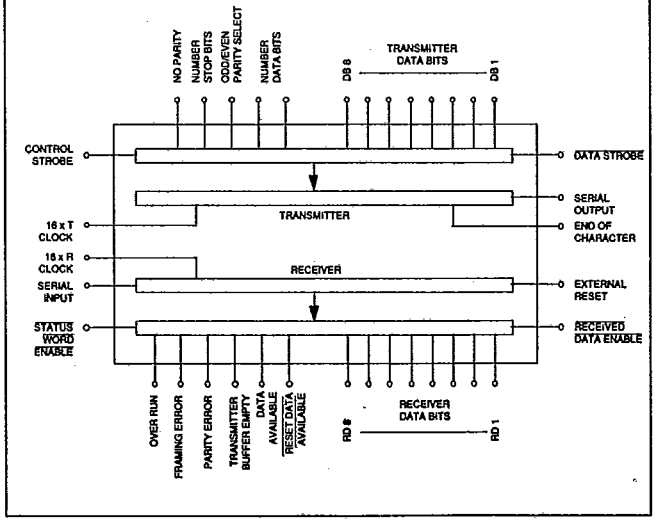
PIN CONFIGURATION

40 LEAD DUAL INLINE

Top View



AY31015D BLOCK DIAGRAM



PIN FUNCTIONS

Pin Number	Signal Name	Input/ Output	Function
1	VCC	I	VCC Power Supply: +5V Supply
2	N.C.	-	(Not Connected)
3	Ground	-	Ground
4	$\overline{RDE}$		$\overline{Received\ Data\ Enable}$: A logic "0" on this input places the received data onto the output lines (RD8..RD1).
5-12	RD8..RD1	I	Received Data Bits: These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{RDE}$ is "0" and a high impedence state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	PE	O	Parity Error: This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state when $\overline{SWE}$ (pin 16) is "1".
14	FE	O	Framing Error: This line goes to a logic "1" if the received character has no valid stop bit. Tri-state when $\overline{SWE}$ (pin 16) is "1".
15	OR	O	Over-Run: This line goes to a logic "1"if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state when $\overline{SWE}$ (pin 16) is "1".
16	$\overline{SWE}$	I	$\overline{Status\ Word\ Enable}$: A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. A logic "1" puts the status word bit outputs into a high impedance state.
17	RCP	I	Receiver Clock: This input line requires a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAV}$	I	$\overline{Reset\ Data\ Available}$: A logic "0" will reset the DAV line. The DAV F/F is the only thing that is reset.
19	DAV	O	Data Available: This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state when $\overline{SWE}$ (pin 16) is "1". Fig. 8.
20	SI	I	Serial Input: This line accepts the serial bit input stream. A marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 7, 8.
21	XR	I	External Reset: Resets all registers. Sets S0, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.

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PIN FUNCTIONS (CONT.)

Pin Number	Signal Name	Input/ Output	Function
22	TBMT	O	Transmitter Buffer Empty: The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 14, 16. Tristate when $\overline{SWE}$ (pin 16) is "1".
23	$\overline{DS}$	I	$\overline{Data\ Strobe}$: A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	EOC	O	End of Character: This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 13, 15.
25	SO	O	Serial Output: This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.
26..33	DB1..DB8	I	Data Bit Inputs: There are up to 8 data bit input lines available.
34	CS	I	Control Strobe: A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	NP	I	No Parity: A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	TSB	I	Number of Stop Bits: This lead will select the number of stop bits, 1 or 2 to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1 1/2 stop bits.
37-38	NB2, NB1	I	Number of Bits/Character: These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	EPS	I	Odd/Even Parity Select: The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even partiy.
40	TCP	I	Transmitter Clock: This input line requires a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc(with Respect to GND) ..... -0.3 to +16V
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) .....+330°C

Standard Conditions

(unless otherwise noted)
Vcc .....+4.75V to +5.25V
Operating Temperature (TA) .....0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Min	Typ	Max	Units	Conditions
Input Logic Levels (AY31015D)					
Logic 0	0	-	0.8	Volts	
Logic 1	2.0	-	V_{CC}+0.3	Volts	Has internal pull-up resistors to V_{CC}
Input Capacitance					
All inputs	-	-	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Tri-State Outputs	1.0	-	-	M ohms	
Data Output Levels					
Logic 0	-	-	0.8	Volts	I_{OL} = 1.6mA (sink)
Logic 1	2.4	-	-	Volts	I_{OL} = 40 µA (source) - at V_{CC} = +5V
Output Capacitance	-	10	15	pF	
Power Supply Current					
I_{CC} at V_{CC} = +5V	-	10	15	mA	

AC CHARACTERISTICS

Characteristics	Min	Typ	Max	Units	Conditions	Remarks
Clock Frequency	DC	-	400	kHz	at V_{CC} = +4.75V	All AC testing
Baud	0	-	25	kbaud	at V_{CC} = +4.75V	waveforms at:
Pulse Width						V_{IH} = 2.4V
Clock Pulse	1.0	-	-	µs	See Fig. 5	V_{IL} = 0.8V
Control Strobe	200	-	-	ns	See Fig. 11	V_{OH} = 2.0V
Data Strobe	200	-	-	ns	See Fig. 10	V_{OL} = 0.8V
External Reset	500	-	-	ns	See Fig. 9	
Status Word Enable	500	-	-	ns	See Fig. 17	
Reset Data Available	200	-	-	ns	See Fig. 18	
Received Data Enable	500	-	-	ns	See Fig. 17	
Set Up & Hold Time						
Input Data Bits	20	-	-	ns	See Fig. 10	
Input Control Bits	20	-	-	ns	See Fig. 11	
Output Propagation Delay						
TPD0	-	-	500	ns	See Figs. 17 and 20	
TPD1	-	-	500	ns	See Figs. 17 and 20	

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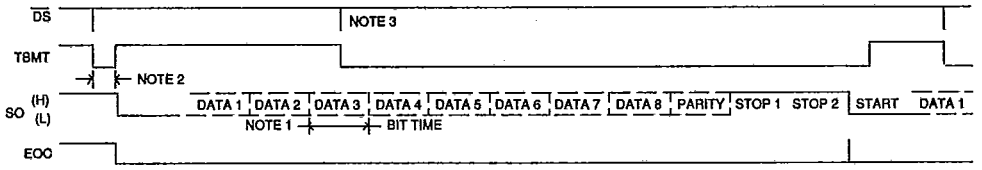
TIMING DIAGRAMS

FIG. 1 UAR/T - TRANSMITTER TIMING



NOTES: SEE FIGURES 2, 3, 4 FOR DETAILS
TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM.
SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE SO 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

DETAIL:

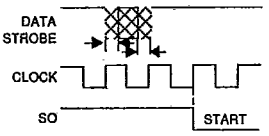


FIG. 2 TRANSMITTER AT START BIT NOT A TEST POINT

TRANSMITTER INACTIVE
TRANSMIT BUFFER LOADED WHEN EOC HIGH

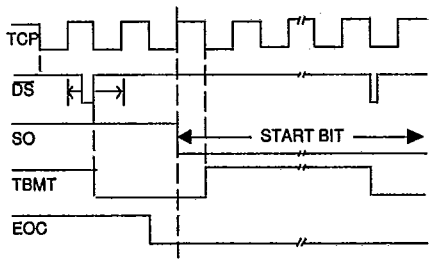


FIG. 3 TRANSMITTER AT START BIT

TRANSMITTER ACTIVE
TRANSMIT BUFFER LOADED WHEN EOC LOW

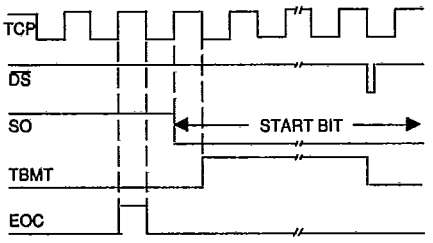
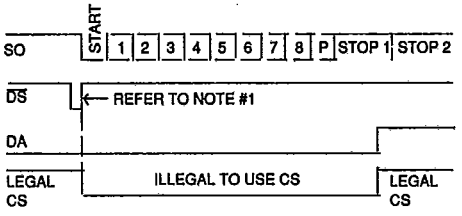


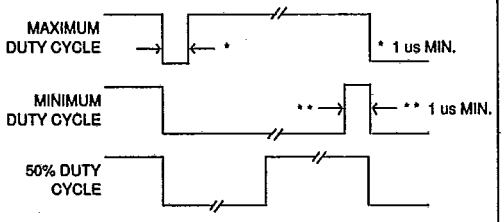
FIG. 4 ALLOWABLE POINTS TO USE



NOTE 1:
DS AND CS MAY OCCUR SIMULTANEOUSLY WHEN TRANSMITTER INACTIVE.

NOTE:
IF CONTROL STROBE IS HARDWIRED TO "1", THEN THE CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME.

FIG. 5 ALLOWABLE TCP, RCP



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

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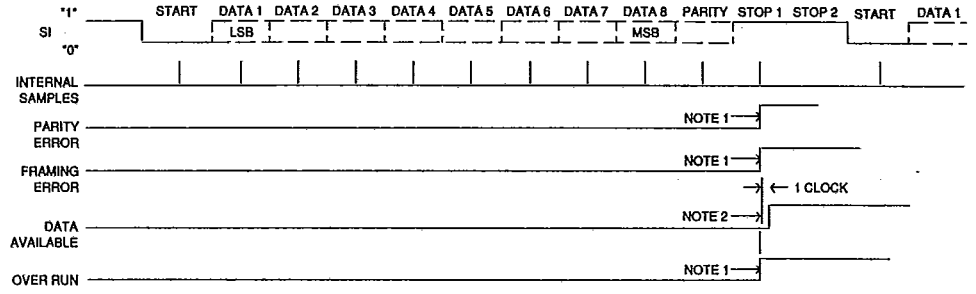
TIMING DIAGRAMS (CONT.)

FIG. 6 UAR/T - RECEIVER TIMING



NOTES:
1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA AND PE, FE, OR HAVE BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTERS UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 BIT CODE WITH PARITY AND TWO STOP BITS. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE, THE DATA IN THE HOLDING REGISTER IS RIGHT JUSTIFIED, THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

FIG. 7 TRUE RECEIVER CENTER SAMPLING

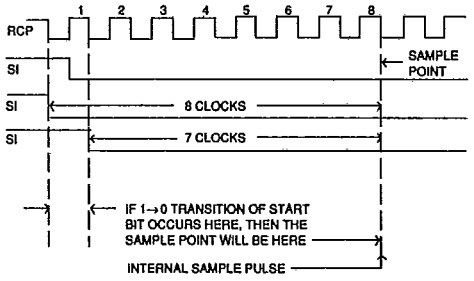


FIG. 8 RECEIVER DURING 1ST STOP BIT

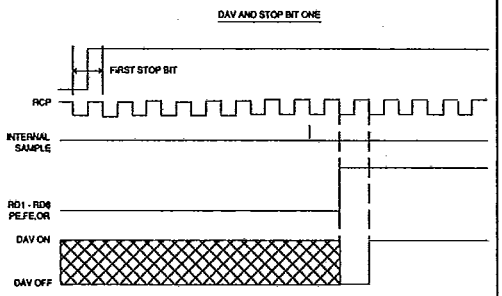
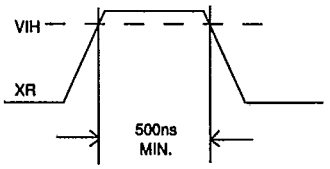


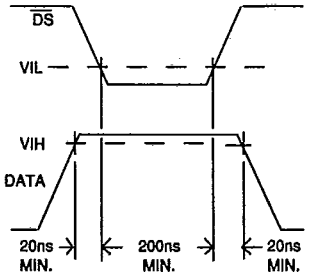
FIG. 9 XR PULSE



WHEN NOT IN USE, XR MUST BE HELD AT GND.

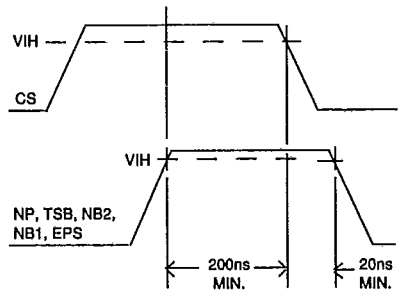
XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT EOC ARE RESET TO LOGIC "1". ALL OTHER OUTPUTS RESET TO LOGIC "0".

FIG. 10 $\overline{DS}$



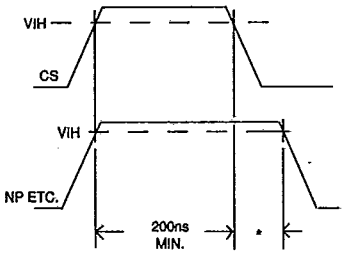
TIMING DIAGRAMS (CONT.)

FIG. 11A CS



CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

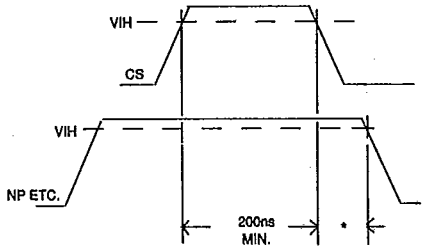
FIG. 11B



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM.

*20ns MIN.

FIG. 12



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

*20ns MIN.

FIG. 13 EOC TURN - ON

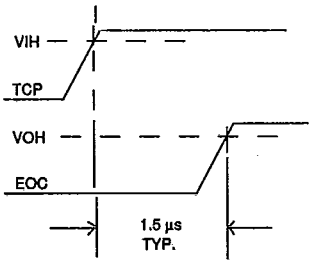


FIG. 14 TBMT TURN - OFF

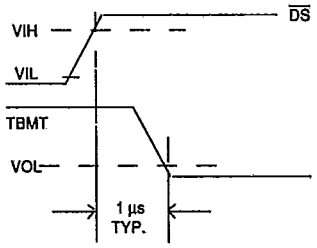
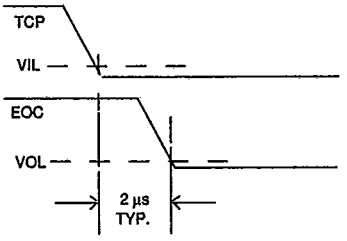


FIG. 15 EOC TURN - OFF



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TIMING DIAGRAMS

FIG. 16 TBMT TURN - ON

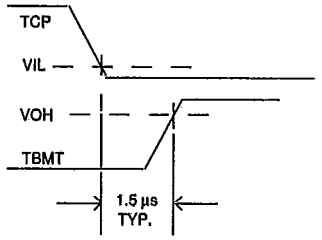


FIG. 17 $\overline{RDE}$, $\overline{SWE}$

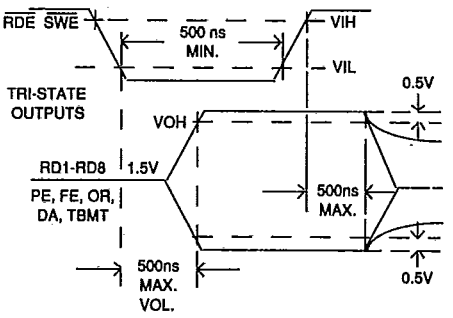


FIG. 18 RDAV

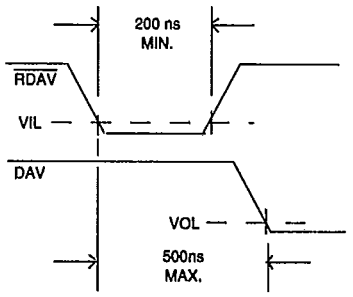


FIG. 19 SHORT CIRCUIT OUTPUT CURRENT

(only 1 output may be shorted at a

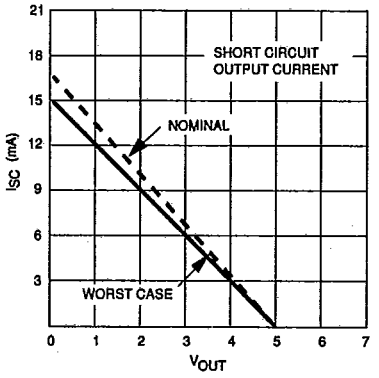


FIG. 20 RD1 - RD8, PE, FE, OR, TBMT, DAV

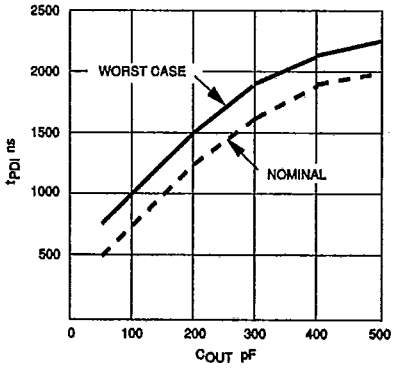


FIG. 21 +5 VOLT SUPPLY CURRENT

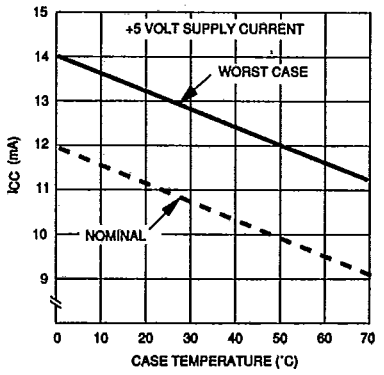
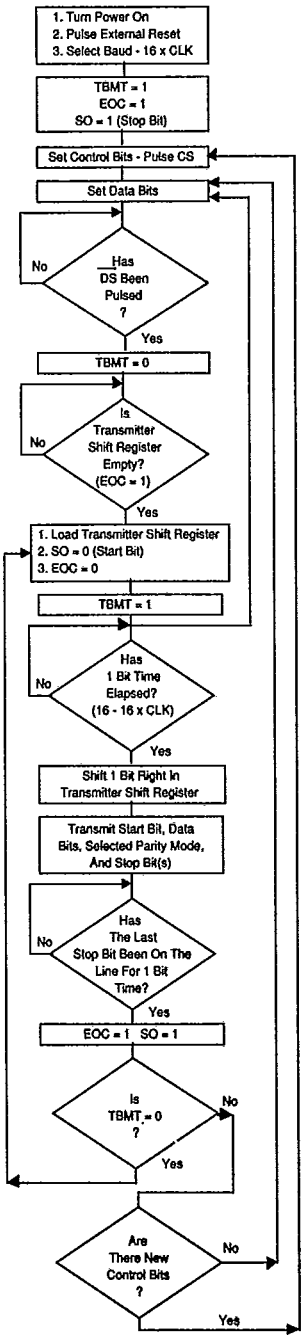


FIG. 22 TRANSMITTER OPERATION



TRANSMITTER

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initialization is complete, user may set control bits and data bits. Control bits selection should occur before data bit selection, however, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0" and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss of transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

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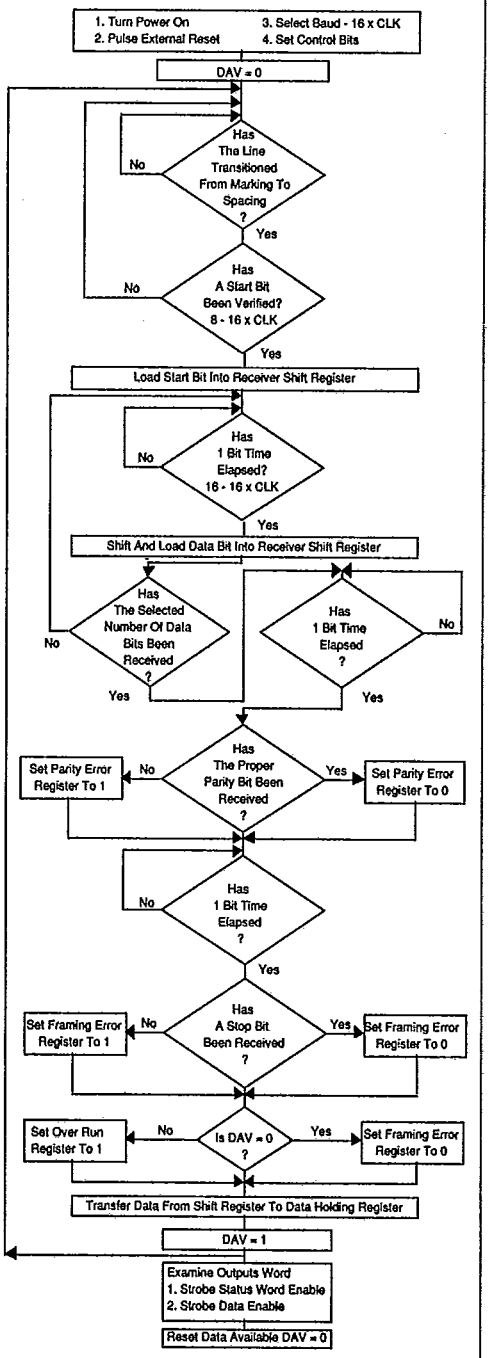
FIG. 23 RECEIVER OPERATION



RECEIVER

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "0".

After initialization is complete, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0"state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s) reception proceeds in an orderly manner.

While receiving parity and stop bit(s), the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected, the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been read out. If the DAV signal is at a logic "1", the receiver will assume data has not been read out and the over run flip-flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0", the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

FIG. 24 TRANSMITTER BLOCK DIAGRAM

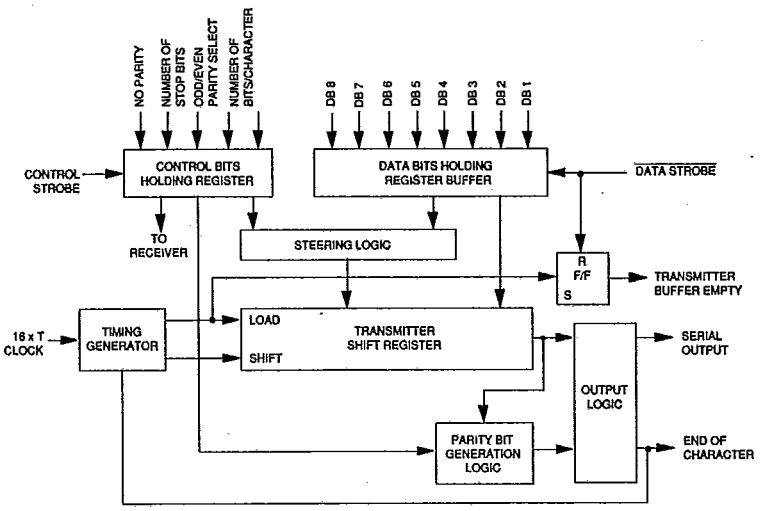
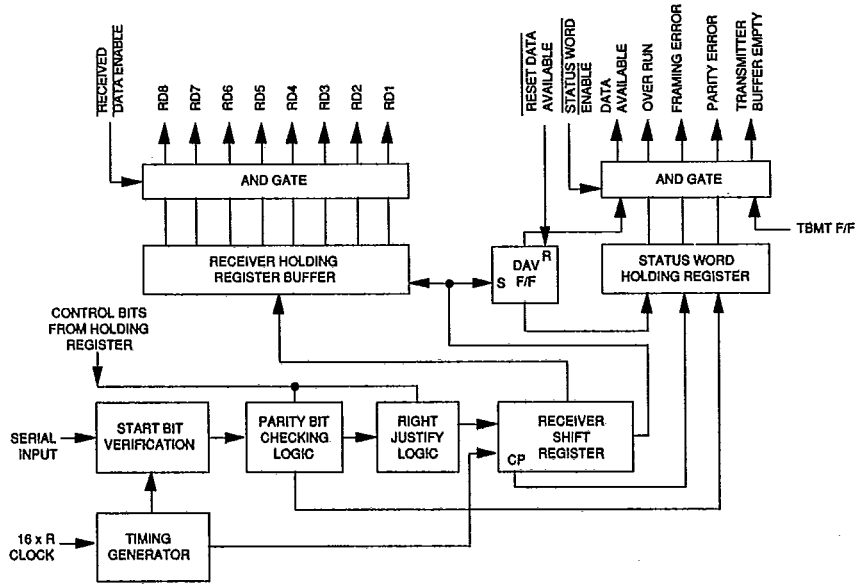


FIG. 25 RECEIVER BLOCK DIAGRAM



5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

AY31015D - / P

Package:		D	Ceramic DIP
		J	CERDIP
		P	Plastic DIP
		L	PLCC
Temperature Range:		Blank	0° C to 70° C only
Device:	AY31015D		UAR/T