ARIZONA MICROTEK, INC.

AZ100ELT23

Dual Differential PECL to CMOS/TTL Translator

FEATURES

- Green / RoHS Compliant / Lead (Pb) Free package available
- 3.5ns Typical Propagation Delay
- <500ps Typical Output to Output Skew
- Differential PECL Inputs
- CMOS/TTL Outputs
- Flow Through Pinouts
- Direct Replacement for ON Semiconductor MC100ELT23
- Operating Range of 3.0V to 5.5V (For operation down to 2.5V consult AZM)
- Use AZ100ELT23 for 10K Applications

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
SOIC 8	AZ100ELT23D	AZM100 ELT23	1,2
SOIC 8 RoHS Compliant / Lead (Pb) Free	AZ100ELT23D+	AZM100+ ELT23	1,2
SOIC 8 Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT23DG	AZM100G ELT23	1,2,3
TSSOP 8	AZ100ELT23T	AZH T23	1,2

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" or "YY" for year followed by "WW" for week on underside of part.
3 The Green package mold compound is halogen free. The leads are plated with 100% matte tin (Sn), eliminating lead (Pb). The Green package is also RoHS compliant / Lead (Pb) Free.

DESCRIPTION

The AZ100ELT23 is a dual differential PECL to CMOS/TTL translator. Because PECL (Positive ECL) levels are used, only V_{CC} and ground are required. The small outline 8-lead packaging and the low skew, dual gate design of the ELT23 makes it ideal for applications that require the translation of a clock and a data signal.

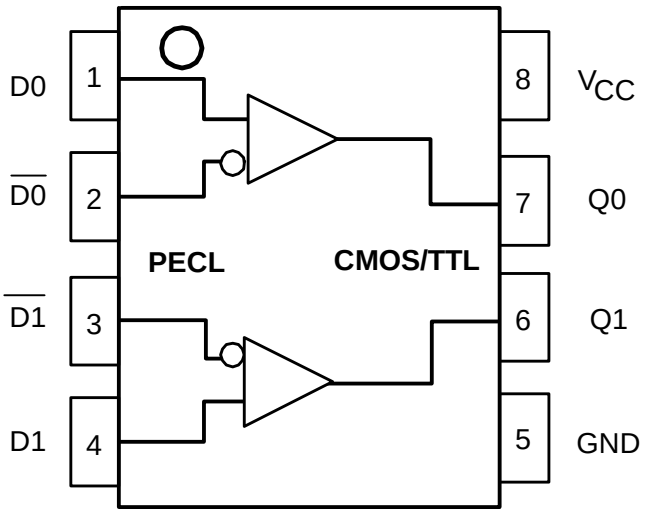
The ELT23 is available in only the ECL 100K standard. Since there are no PECL outputs or an external V_{BB} reference, the ELT23 does not require both ECL standard versions. The PECL inputs are differential; there is no specified difference between the differential input 10K and 100K standards. Therefore the AZ100ELT23 can accept any standard differential PECL input referenced from a V_{CC} of 3.0V to 5.5V.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	CMOS/TTL Outputs
DO, $\overline{D0}$ – D1, $\overline{D1}$	Differential PECL inputs
V_{CC}	Positive Supply
GND	Ground

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



1630 S. STAPLEY DR., SUITE 125 • MESA, ARIZONA 85204 • USA • (480) 962-5881 • FAX (480) 890-2541
www.azmicrotek.com

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Character	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	7.0	V
T_A	Operating Temperature Range (In Free-Air)	-40 to+ 85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

CMOS/TTL DC CHARACTERISTICS (V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC} - 0.5			V	I_{OH} = -24 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 24 mA
I_{CC}	Power Supply Current		9.0	15	mA	0°C to 85°C
I_{CC}	Power Supply Current		9.0	17.6	mA	-40°C to 85°C
I_{OS}	Output Short Circuit Current		100		mA	

100K LVPECL DC Characteristics (V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	1490		1825	mV
V_{PP}	Minimum Input Swing[1]	200			200			200			200			mV
V_{CMR}	Common Mode Range	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{IH}	Input HIGH Current			150			150			150			150	µA

1. 200mV input guarantees full logic swing at the output.

100K PECL DC Characteristics (V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{PP}	Minimum Input Swing[1]	200			200			200			200			mV
V_{CMR}	Common Mode Range	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{IH}	Input HIGH Current			150			150			150			150	µA

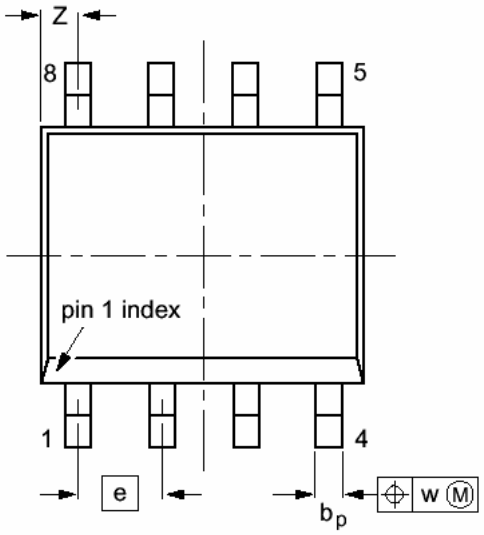
1. 200mV input guarantees full logic swing at the output.

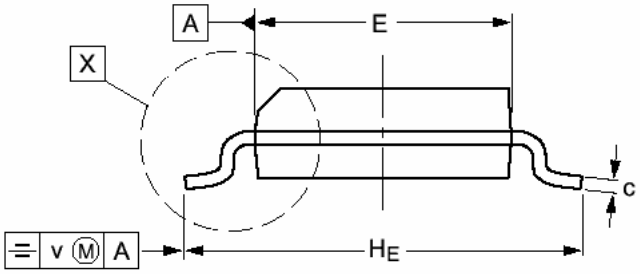
AC Characteristics (V_{CC} = +3.0V to +5.5V)

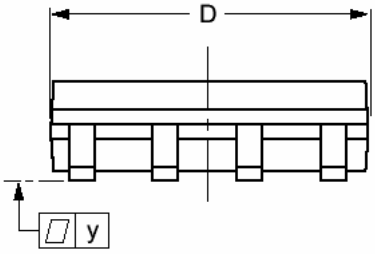
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay to Output[1]													
	V_{CC} = 4.5V to 5.5V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	ns
	V_{CC} = 3.0V to 3.6V	3.5		7.0	3.5		7.0	3.5		7.0	3.5		7.0	

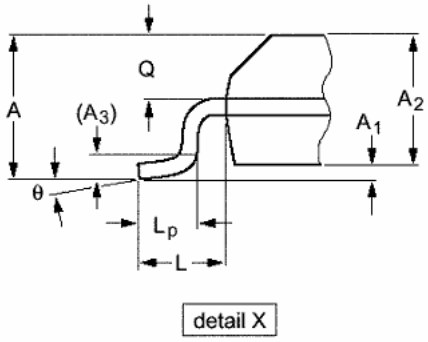
1. C_L=20pF

PACKAGE DIAGRAM
SOIC 8





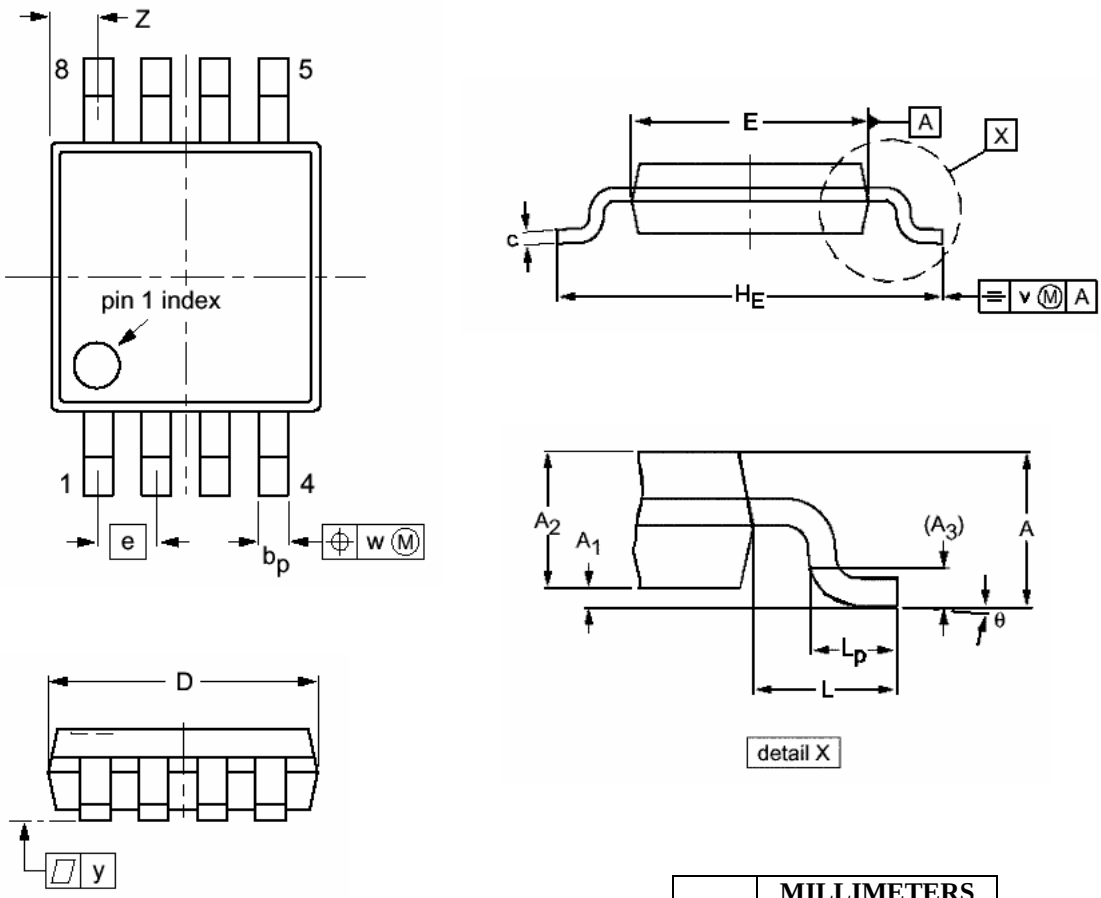




NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
A_2	1.28	1.57	0.050	0.062
A_3	0.25		0.01	
b_p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.0	0.19	0.20
E	3.80	4.0	0.15	0.16
e	1.27		0.050	
H_E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L_p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0^O	8^O	0^O	8^O

PACKAGE DIAGRAM
TSSOP 8



NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
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DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A_1	0.05	0.15
A_2	0.75	0.95
A_3	0.25	
b_p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H_E	4.75	5.05
L	0.95	
L_p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0^O	6^O