



# AZ100LVEL16VT ARIZONA MICROTEK, INC.

## ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

### FEATURES

- High Bandwidth for  $\geq 1\text{GHz}$
- **Similar Operation as AZ100LVEL16VR except in Disabled Condition:  $Q_{HG}$  is High**
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a 3x3 mm or 2x2 mm MLP Package
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website

### PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2x0.75)	AZ100LVEL16VTNA	P9 <Date Code>	1,2,3
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNA+	P9+ <Date Code>	1,2
MLP 8 (2x2x0.75)	AZ100LVEL16VTNB	P8 <Date Code>	1,2,4
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNB+	P8+ <Date Code>	1,2
MLP 8 (2x2x0.75)	AZ100LVEL16VTNC	P2 <Date Code>	1,2,5
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNC+	P2+ <Date Code>	1,2
MLP 8 (2x2x0.75)	AZ100LVEL16VTND	P3 <Date Code>	1,2
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTND+	P3+ <Date Code>	1,2
MLP 16 (3x3)	AZ100LVEL16VTL	AZM 16T <Date Code>	1,2
MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTL+	AZM+ 16T <Date Code>	1,2
DIE	AZ100LVEL16VTXP	N/A	6

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.
- 3 Parts marked TNA for date codes prior to 4WW (prior to 2004).
- 4 Parts marked TNB for date codes prior to 4WW (prior to 2004).
- 5 Parts marked TNC for date codes prior to 4WW (prior to 2004).
- 6 Waffle Pack

### DESCRIPTION

The AZ100LVEL16VT is a specialized oscillator gain stage with high gain output buffer including an enable. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have a voltage gain several times greater than the  $Q/\bar{Q}$  outputs.

#### **MLP 16, 3x3 mm Package (VTL) or DIE (VTX)**

The AZ100LVEL16VTL and AZ100LVEL16VTX provide a selectable enable input (EN) that allows continuous oscillator operation. See truth table for the Enable function. If Enable pull-up is desired in the CMOS/TTL mode, an external  $\leq 20\text{ k}\Omega$  resistor connecting EN to  $V_{CC}$  will override the on-chip pull-down resistor. When disabled, the  $Q_{HG}$  output is forced high and the  $\bar{Q}_{HG}$  output is forced low. The AZ100LVEL16VTL/VTX also provides a  $V_{BB}$  and 470  $\Omega$  internal bias resistors from D to  $V_{BB}$  and  $\bar{D}$  to  $V_{BB}$ . The  $V_{BB}$  pin can support 1.5 mA sink/source current. Bypassing  $V_{BB}$  to ground with a 0.01  $\mu\text{F}$  capacitor is recommended.

The outputs Q and  $\bar{Q}$  each have a selectable on-chip pull-down current source. See truth table below for current source functions. External resistors may also be used to increase pull-down current to a maximum total of 25 mA.

# AZ100LVEL16VT

Outputs  $Q_{HG}$  and  $\bar{Q}_{HG}$  each have an optional on-chip pull-down current source of 10 mA. When pad/pin  $V_{EEP}$  is left open (NC), the output current sources are disabled and the  $Q_{HG}/\bar{Q}_{HG}$  operate as standard PECL/ECL. When  $V_{EEP}$  is connected to  $V_{EE}$ , the current sources are activated. The  $Q_{HG}/\bar{Q}_{HG}$  pull-down current can be decreased, by using a resistor to connect  $V_{EEP}$  to  $V_{EE}$ . (See graph on page 5.)

## MLP 8, 2x2 mm Package, VTNA, VTNB, VTNC & VTND Versions

All MLP 8, 2x2mm versions of the AZ100LVEL16VT provide an enable input that allows continuous oscillator operation. VTNA and VTNB utilize an enable ( $\bar{EN}$ ) that operates in the PECL/ECL mode. When the  $\bar{EN}$  input is LOW, the  $\bar{Q}$  and  $Q_{HG}/\bar{Q}_{HG}$  outputs follow the data inputs. When  $\bar{EN}$  is HIGH, the  $Q_{HG}$  output is forced high and the  $\bar{Q}_{HG}$  output is forced low. VTNC and VTND utilize an enable (EN) that operates in the CMOS/TTL mode. When the EN input is HIGH, the  $\bar{Q}$  and  $Q_{HG}/\bar{Q}_{HG}$  outputs follow the data inputs. When EN is LOW, the  $Q_{HG}$  output is forced high and the  $\bar{Q}_{HG}$  output is forced low.

For VTNA and VTND, both D and  $\bar{D}$  inputs are brought out and tied to the  $V_{BB}$  pin through 470  $\Omega$  internal bias resistors. In VTNB and VTNC, the  $\bar{D}$  input is internally tied directly to the  $V_{BB}$  pin and the D input is tied to the  $V_{BB}$  pin through a 470  $\Omega$  internal bias resistor. Bypassing  $V_{BB}$  to ground with a 0.01  $\mu$ F capacitor is recommended.

All MLP 8, 2x2mm versions (VTNA, VTNB, VTNC & VTND) have the Q,  $Q_{HG}$ , and  $\bar{Q}_{HG}$  current sources disabled, while the  $\bar{Q}$  output operates with a 4 mA current source to  $V_{EE}$ .

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

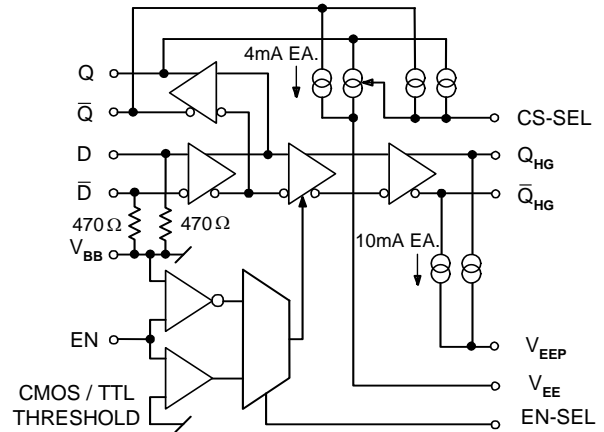
**ENABLE TRUTH TABLE**  
MLP 16 (VTL) or DIE (VTX)

EN-SEL	EN	Q/Q	$Q_{HG}$	$\bar{Q}_{HG}$
NC	PECL Low, $V_{EE}$ or NC	Data	Data	Data
NC	PECL High or $V_{CC}$	Data	High	Low
$V_{EE}^*$	CMOS Low or $V_{EE}$	Data	High	Low
$V_{EE}^*$	CMOS High or $V_{CC}$	Data	Data	Data
$V_{EE}^*$	NC, no external pull-up	Data	High	Low
$V_{EE}^*$	NC, with $\leq 20k\Omega$ to $V_{CC}$	Data	Data	Data

\*Connections to  $V_{CC}$  or  $V_{EE}$  must be less than 1 $\Omega$ .

## PIN DESCRIPTION

PIN	FUNCTION
D/ $\bar{D}$	Data Inputs
Q/ $\bar{Q}$	Data Outputs
$Q_{HG}/\bar{Q}_{HG}$	Data Outputs w/High Gain
$V_{BB}$	Reference Voltage Output
EN-SEL	Selects Enable Logic
EN/ $\bar{EN}$	Enable Input
CS-SEL	Selects Q and $\bar{Q}$ Current Source Magnitude
$V_{EEP}$	Optional $Q_{HG}$ and $\bar{Q}_{HG}$ Current Sources
$V_{EE}$	Negative Supply
$V_{CC}$	Positive Supply



MLP 16 (VTL) or DIE (VTX)

**CURRENT SOURCE TRUTH TABLE**  
MLP 16 (VTL) or DIE (VTX)

CS-SEL	Q	$\bar{Q}$
NC	4mA typ.	4mA typ.
$V_{EE}^*$	8mA typ.	8mA typ.
$V_{CC}^*$	0	4mA typ.

\*Connections to  $V_{CC}$  or  $V_{EE}$  must be less than 1 $\Omega$ .

# AZ100LVEL16VT

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
V <sub>CC</sub>	PECL Power Supply (V <sub>EE</sub> = 0V)	0 to +8.0	Vdc
V <sub>I</sub>	PECL Input Voltage (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>EE</sub>	ECL Power Supply (V <sub>CC</sub> = 0V)	-8.0 to 0	Vdc
V <sub>I</sub>	ECL Input Voltage (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
I <sub>OUT</sub>	Output Current Q <sub>HG</sub> /Q <sub>HG</sub> --- Continuous	50	mA
	--- Surge	100	
Output Current Q/Q	--- Continuous	25	
--- Surge		50	
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

## 100K ECL DC Characteristics (V<sub>EE</sub> = -3.0V to -5.5V, V<sub>CC</sub> = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>2</sup>	-1045	-835	-995	-835	-995	-835	-995	-835	mV
V <sub>OH</sub>	Output HIGH Voltage <sup>4</sup>	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V <sub>OL</sub>	Output LOW Voltage <sup>2,4</sup>	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage									
	D/D, EN/EN (PECL) EN (CMOS/TTL)	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage									
	D/D, EN/EN (PECL) EN (CMOS/TTL)	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	mV
V <sub>BB</sub>	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I <sub>IL</sub>	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		µA
I <sub>IH</sub>	Input HIGH Current EN <sup>3</sup>		150		150		150		150	µA
I <sub>EE</sub>	Power Supply Current <sup>1</sup>		48		48		48		54	mA

1. Specified with V<sub>EEP</sub> and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB, VTNC & VTND.
2. Specified with V<sub>EEP</sub> and CS-SEL connected to V<sub>EE</sub> for VTL and VTX only.
3. Specified with EN-SEL open for VTL and VTX only.
4. Specified with Q<sub>HG</sub>/Q<sub>HG</sub> connected with 50 Ω to V<sub>CC</sub>-2V for VTNA, VTNB, VTNC & VTND.

## 100K LVPECL DC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1,3</sup>	2255	2465	2305	2465	2305	2465	2305	2465	mV
V <sub>OH</sub>	Output HIGH Voltage <sup>1,5</sup>	2215	2420	2275	2420	2275	2420	2275	2420	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1,3,5</sup>	1375	1745	1400	1655	1480	1680	1400	1680	mV
V <sub>IH</sub>	Input HIGH Voltage									
	D/D, EN/EN (PECL) <sup>1</sup> EN (CMOS/TTL)	2135 2000	2420 V <sub>CC</sub>	2135 2000	2420 V <sub>CC</sub>	2135 2000	2420 V <sub>CC</sub>	2135 2000	2420 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage									
	D/D, EN/EN (PECL) <sup>1</sup> EN (CMOS/TTL)	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	mV
V <sub>BB</sub>	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
I <sub>IL</sub>	Input LOW Current EN <sup>4</sup>	0.5		0.5		0.5		0.5		µA
I <sub>IH</sub>	Input HIGH Current EN <sup>4</sup>		150		150		150		150	µA
I <sub>EE</sub>	Power Supply Current <sup>2</sup>		48		48		48		54	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with V<sub>EEP</sub> and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB, VTNC & VTND.
3. Specified with V<sub>EEP</sub> and CS-SEL connected to V<sub>EE</sub> for VTL and VTX only.
4. Specified with EN-SEL open for VTL and VTX only.
5. Specified with Q<sub>HG</sub>/Q<sub>HG</sub> connected with 50 Ω to V<sub>CC</sub>-2V for VTNA, VTNB, VTNC & VTND.

# AZ100LVEL16VT

## 100K PECL DC Characteristics ( $V_{EE} = \text{GND}$ , $V_{CC} = +5.0\text{V}$ )

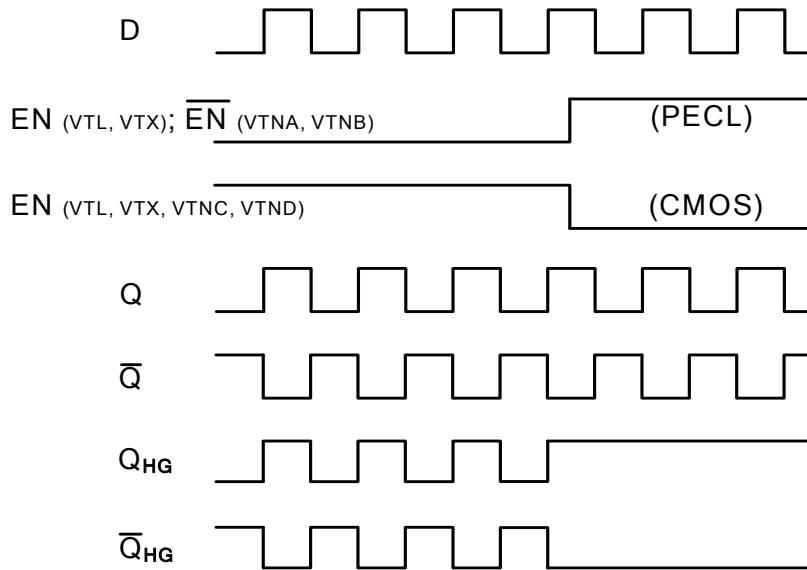
Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,3</sup>	3955	4165	4005	4165	4005	4165	4005	4165	mV
$V_{OH}$	Output HIGH Voltage <sup>1,5</sup>	3915	4120	3975	4120	3975	4120	3975	4120	mV
$V_{OL}$	Output LOW Voltage <sup>1,3,5</sup>	3075	3445	3100	3338	3100	3338	3100	3338	mV
$V_{IH}$	Input HIGH Voltage D/ $\bar{D}$ , EN/ $\bar{EN}$ (PECL) <sup>1</sup> EN (CMOS/TTL)	3835	4120	3835	4120	3835	4120	3835	4120	mV
		2000	$V_{CC}$	2000	$V_{CC}$	2000	$V_{CC}$	2000	$V_{CC}$	
$V_{IL}$	Input LOW Voltage D/ $\bar{D}$ , EN/ $\bar{EN}$ (PECL) <sup>1</sup> EN (CMOS/TTL)	3190	3525	3190	3525	3190	3525	3190	3525	mV
		GND	800	GND	800	GND	800	GND	800	
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IL}$	Input LOW Current EN <sup>4</sup>	0.5		0.5		0.5		0.5		$\mu\text{A}$
$I_{IH}$	Input HIGH Current EN <sup>4</sup>		150		150		150		150	$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Specified with  $V_{EEP}$  and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB, VTNC & VTND.
- Specified with  $V_{EEP}$  and CS-SEL connected to  $V_{EE}$  for VTL and VTX only.
- Specified with EN-SEL open for VTL and VTX only.
- Specified with  $Q_{HG}/\bar{Q}_{HG}$  connected with 50  $\Omega$  to  $V_{CC} - 2\text{V}$  for VTNA, VTNB, VTNC & VTND.

## AC Characteristics ( $V_{EE} = -3.0\text{V}$ to $-5.5\text{V}$ ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$ ; $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH} / t_{PHL}$	Propagation Delay D to Q/ $\bar{Q}$ Outputs <sup>1</sup> (SE) D to $Q_{HG}/\bar{Q}_{HG}$ Outputs <sup>1</sup> (SE)			400			400			400			430	ps
				550			550			550			630	
$t_{SKEW}$	Duty Cycle Skew <sup>2</sup> (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}$	Minimum Input Swing <sup>3</sup> DIFF SE	80			80			80			80			mV
		160			160			160			160			
$t_r / t_f$	Output Rise/Fall Times <sup>1</sup> (20% - 80%)	100		260	100		260	100		260	100		260	ps

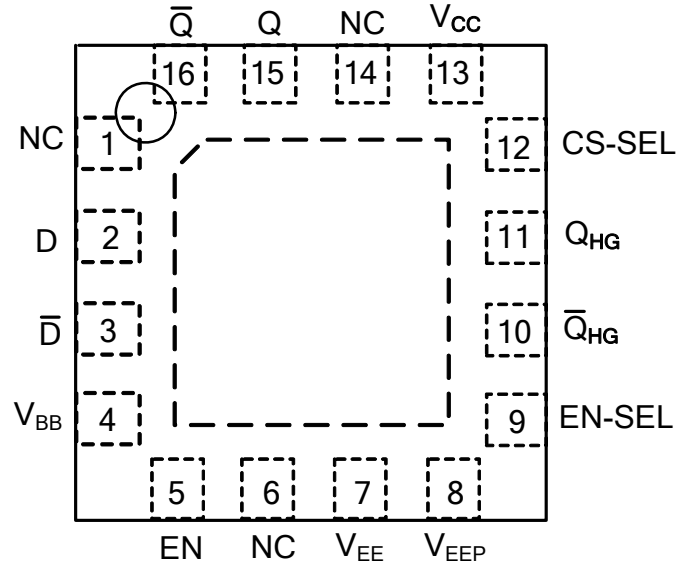
- For VTL and VTX, output specified with  $V_{EEP}$  and CS-SEL connected to  $V_{EE}$  with an AC coupled 50 $\Omega$  load. For VTNA, VTNB, VTNC & VTND, AC coupled 50 $\Omega$  on Q to  $V_{CC} - 2\text{V}$  and DC coupled 50 $\Omega$  to  $V_{CC} - 2\text{V}$  on  $Q_{HG}/\bar{Q}_{HG}$ .
- Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
- $V_{PP}$  is the minimum peak-to-peak input swing for which AC parameters guaranteed. The device has a voltage gain of  $\approx 20$  to Q/ $\bar{Q}$  outputs and a voltage gain of  $\approx 100$  to  $Q_{HG}/\bar{Q}_{HG}$  outputs.



TIMING DIAGRAM

**AZ100LVEL16VTL**

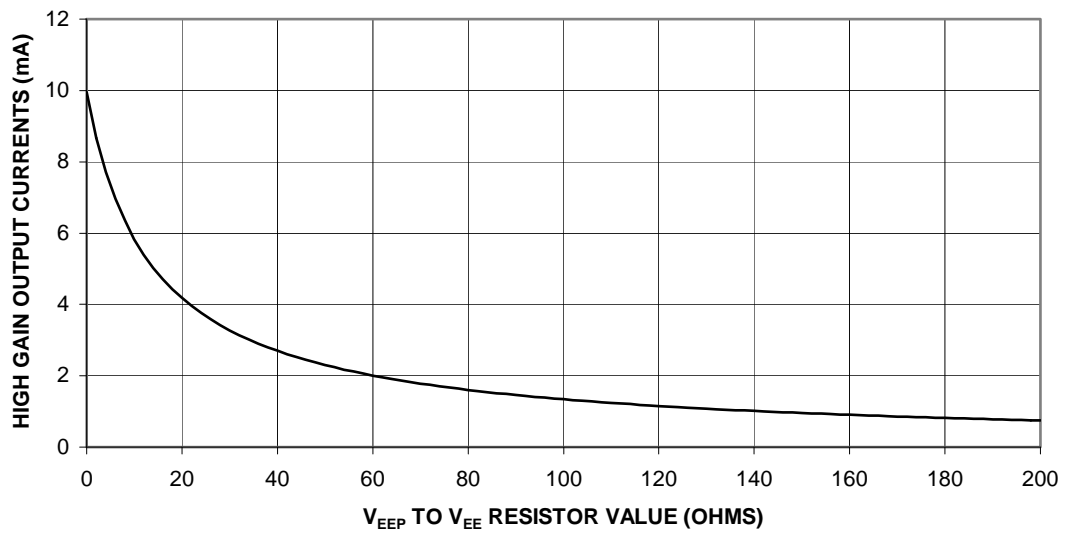
MLP 16  
3x3 mm



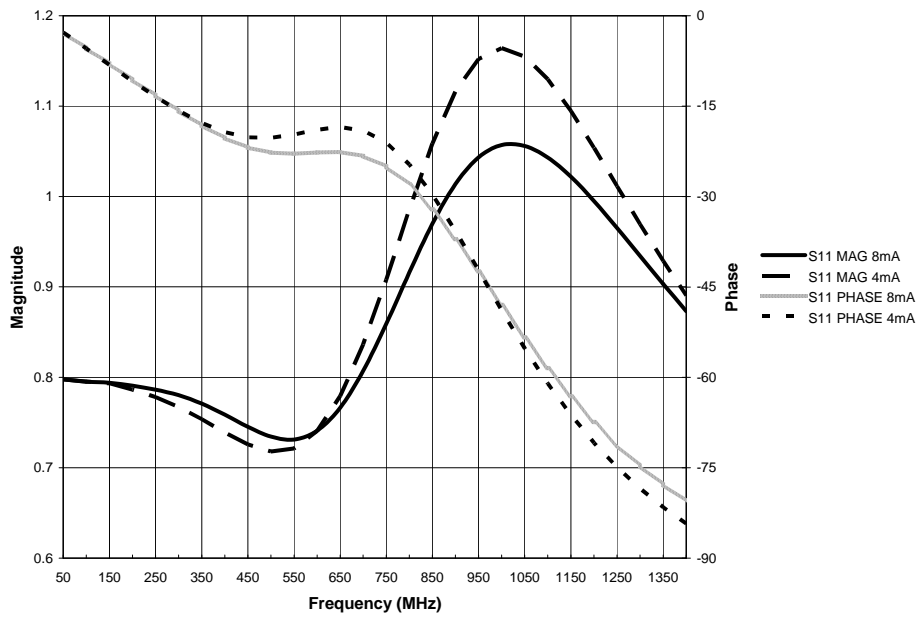
TOP VIEW

Bottom Center Pad may be left open or tied to V<sub>EE</sub>

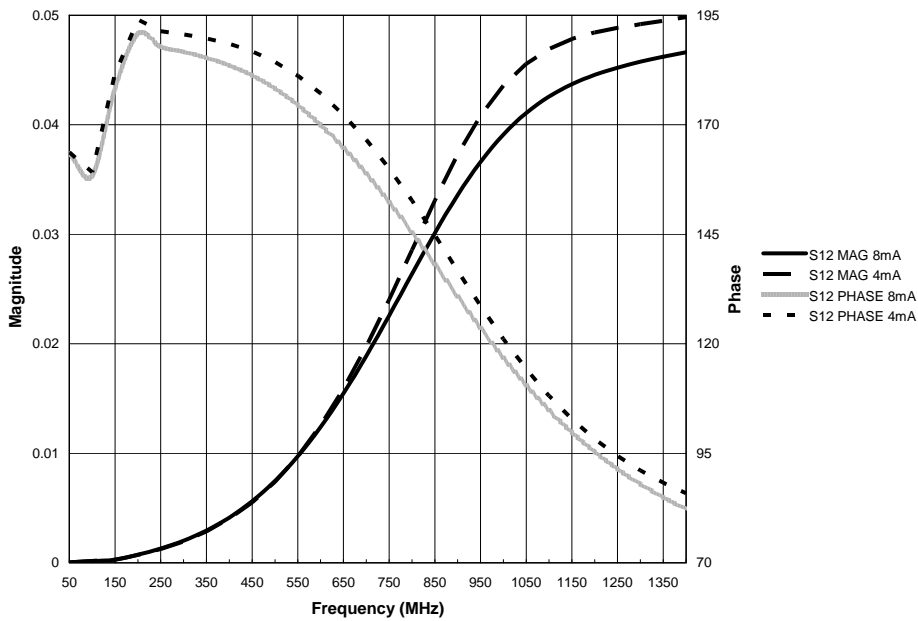
**ADJUSTABLE HIGH GAIN OUTPUT CURRENT**



# AZ100LVEL16VT

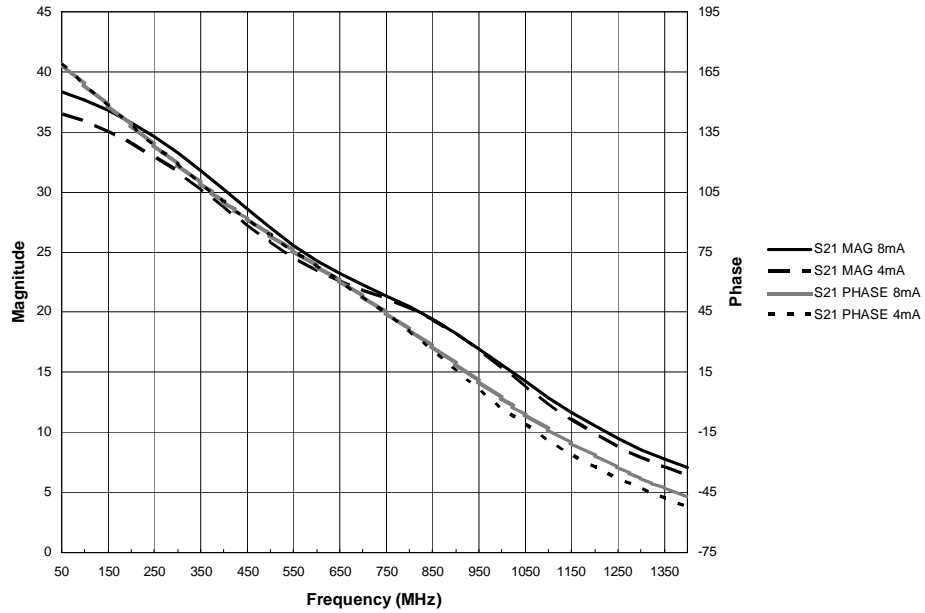


**S11, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

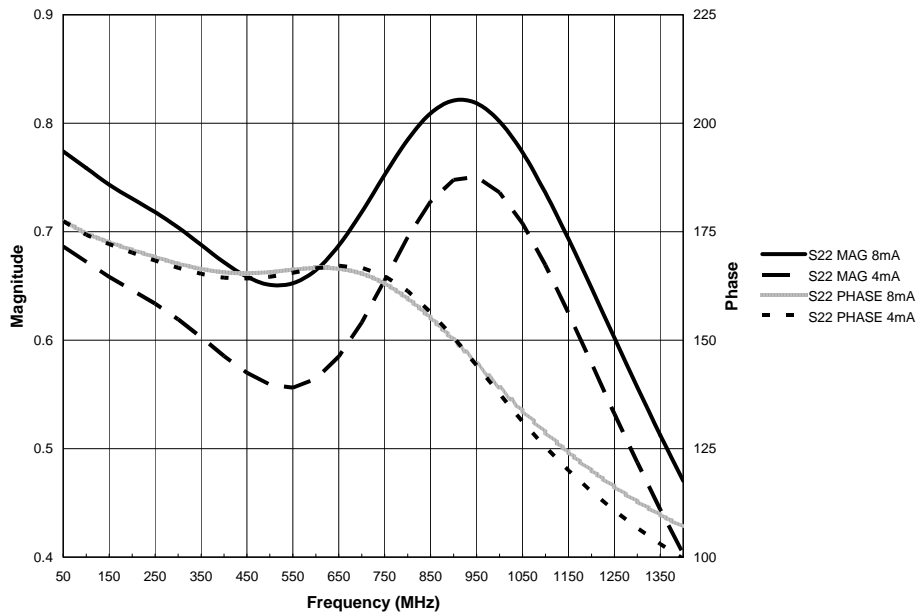


**S12, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

# AZ100LVEL16VT

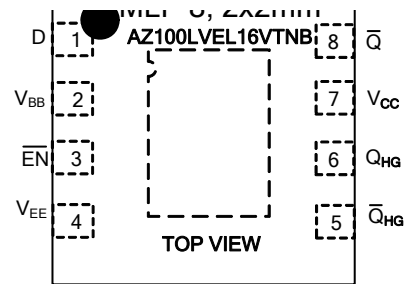
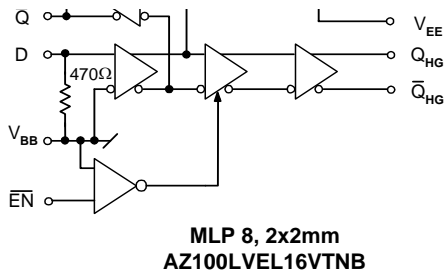
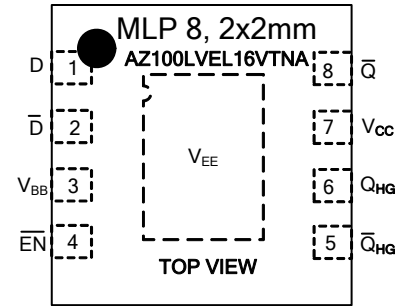
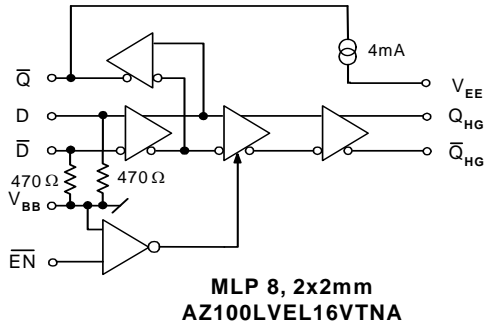


**S21, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)



**S22, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

**LOGIC DIAGRAMS AND PINOUTS FOR 2x2mm PACKAGE**



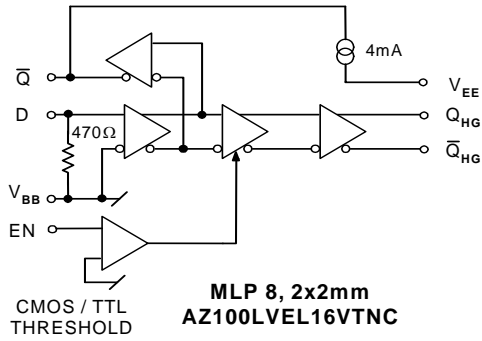
**EN** operation follows PECL functionality.  
See Timing Diagram above.

**Bottom Center Pad** may be left open  
or tied to  $V_{EE}$ . Pin 4 is the  $V_{EE}$  return.

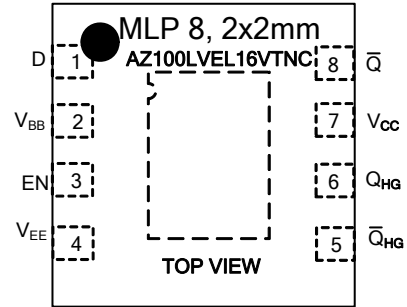


# AZ100LVEL16VT

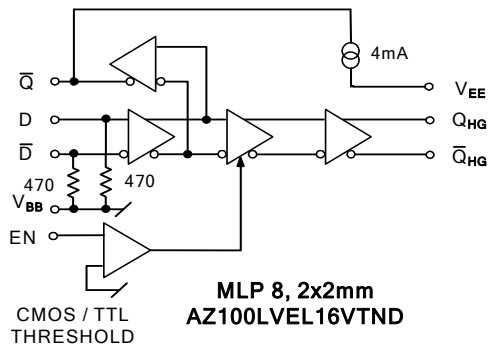
## LOGIC DIAGRAMS AND PINOUTS FOR 2x2mm PACKAGE



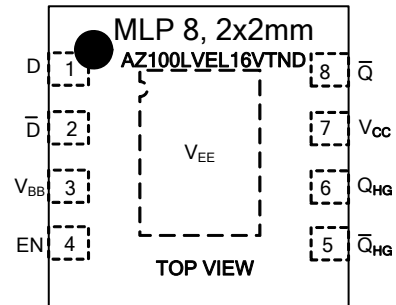
EN operation follows CMOS/TTL functionality. See Timing Diagram above.



Bottom Center Pad may be left open or tied to  $V_{EE}$ . Pin 4 is the  $V_{EE}$  return.



EN operation follows CMOS/TTL functionality. See Timing Diagram above.

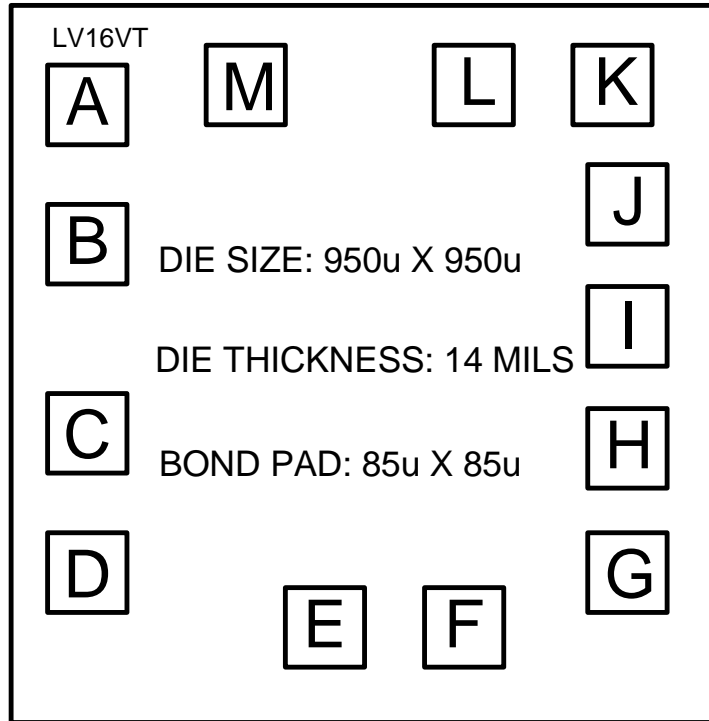


Bottom Center Pad is the  $V_{EE}$  return.

**AZ100LVEL16VT**

**DIE PAD COORDINATES**

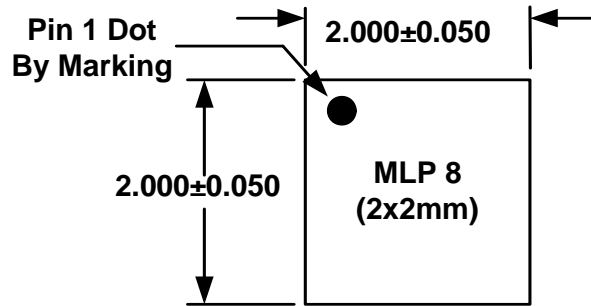
**AZ100LVEL16VT DIE:**



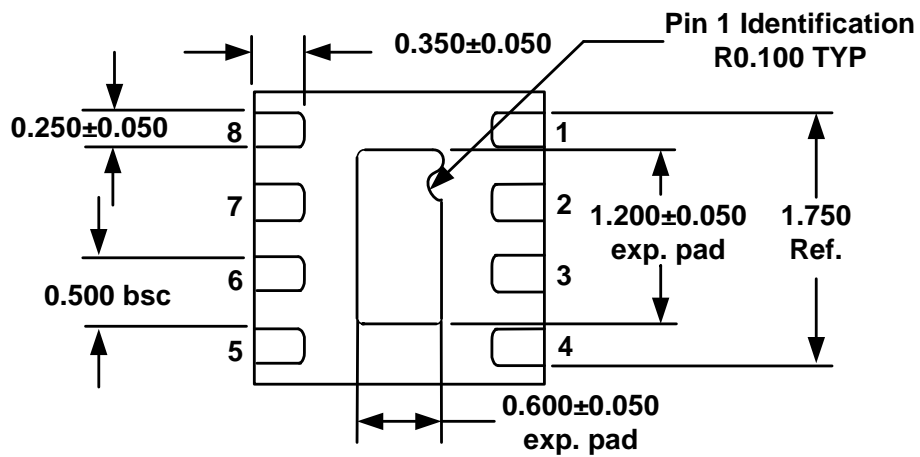
**PAD CENTER COORDINATES**

NAME	PAD DESIGNATION	X(Microns)	Y(Microns)
A	D	-342.5	312.5
B	$\bar{D}$	-342.5	144.5
C	$V_{BB}$	-342.5	-87.0
D	EN	-342.5	-255.0
E	$V_{EE}$	-33.5	-312.5
F	$V_{EEP}$	126.5	-312.5
G	EN-SEL	312.5	-248.5
H	$\bar{Q}_{HG}$	312.5	-98.5
I	$Q_{HG}$	312.5	51.5
J	CS-SEL	312.5	201.5
K	$V_{CC}$	302.5	342.5
L	Q	142.5	342.5
M	$\bar{Q}$	-140.5	342.5

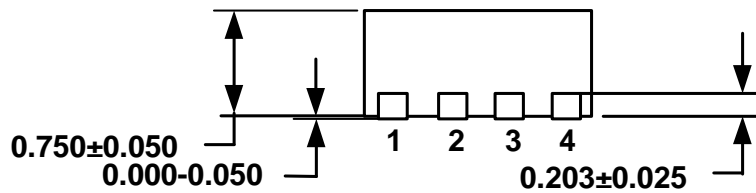
**PACKAGE DIAGRAM**  
**MLP 8 2x2mm**



TOP VIEW



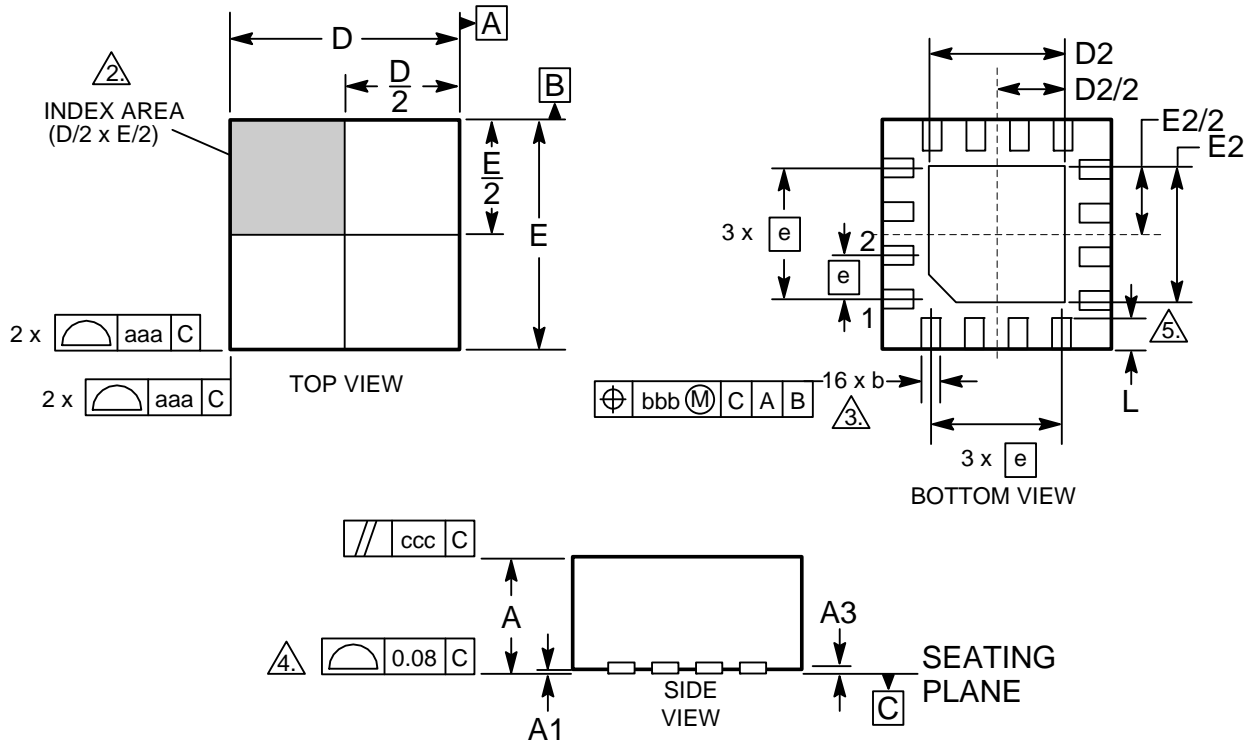
BOTTOM VIEW



SIDE VIEW

**Note: All dimensions are in mm**

**PACKAGE DIAGRAM**  
**MLP 16 3X3mm**



**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
- $(\triangle 2)$ . THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
- $(\triangle 3)$ . DIMENSION  $b$  APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
- $(\triangle 4)$ . COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- $(\triangle 5)$ . INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

## AZ100LEVEL16VT

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