

## Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines
- Provide ESD protection for each line to IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 10\text{kV}$  (contact)
- **For operating voltage of 5V and below**
- **Ultra low capacitance : 0.5pF typical**
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Simplified layout for HDMI connectors
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- **High Definition Multi-Media Interface (HDMI) 1.3 version**
- **DisplayPort interface**
- **SATA and eSATA interface**
- Digital Visual Interface (DVI)
- USB2.0 up to 480Mb/s
- IEEE 1394 up to 3.2 Gb/s
- Ethernet port: 10/100/1000 Mb/s
- Desktop and Notebooks PCs
- Consumer Electronics

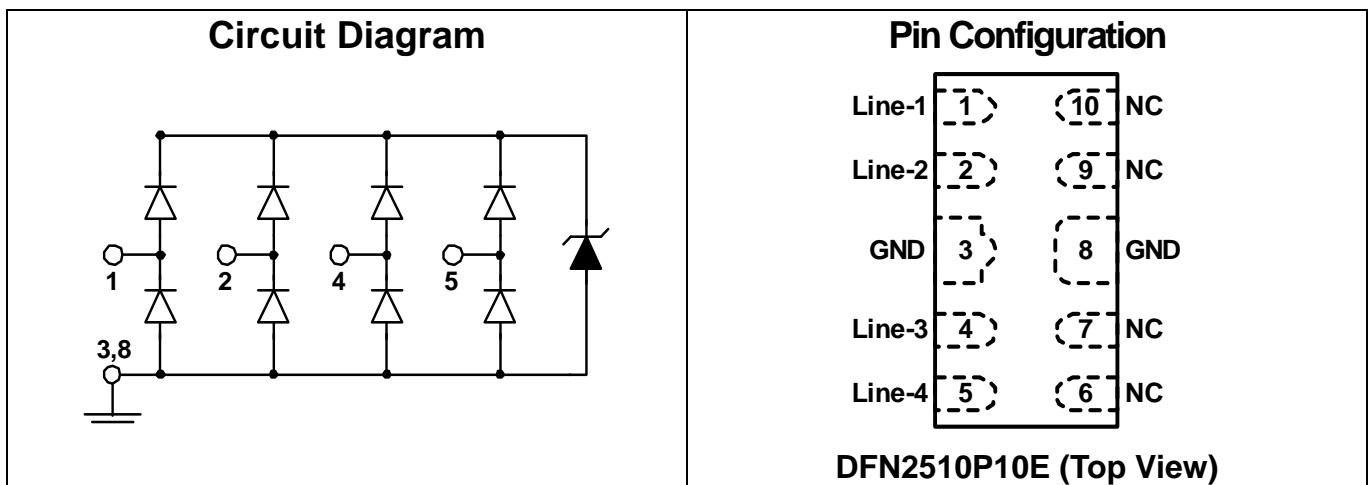
- Set Top Box
- DVDRW Players
- Graphics Cards

## Description

AZ1045-04F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1045-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

AZ1045-04F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1045-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

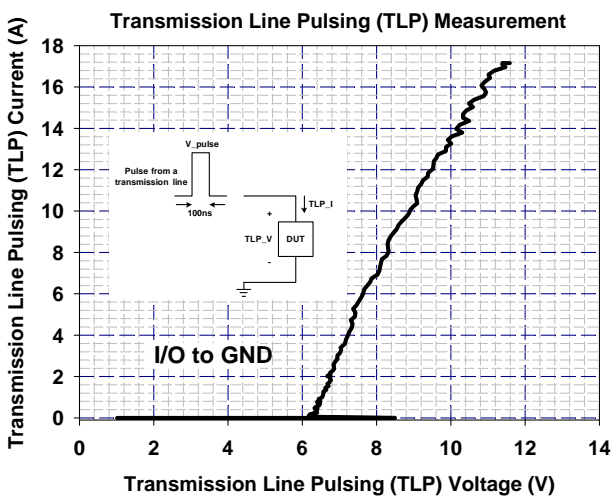
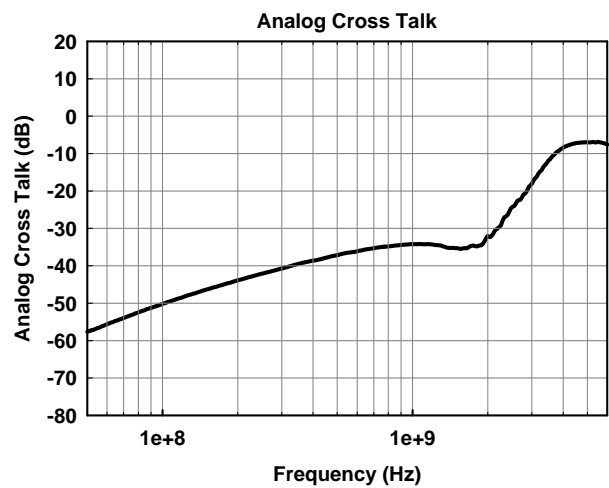
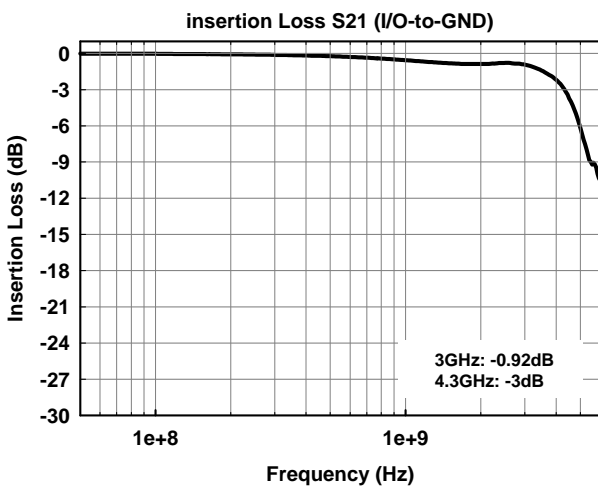
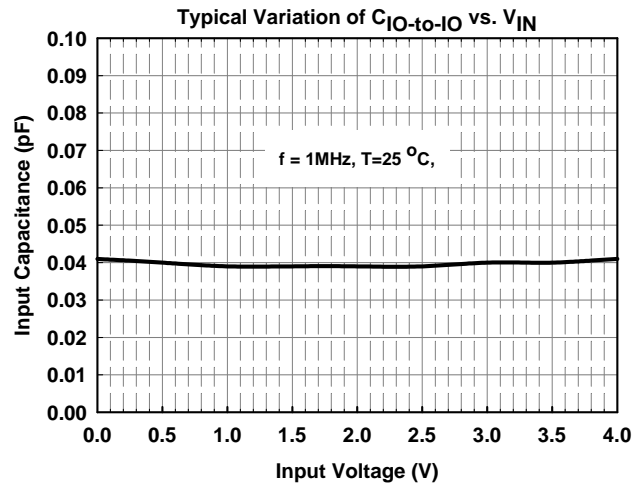
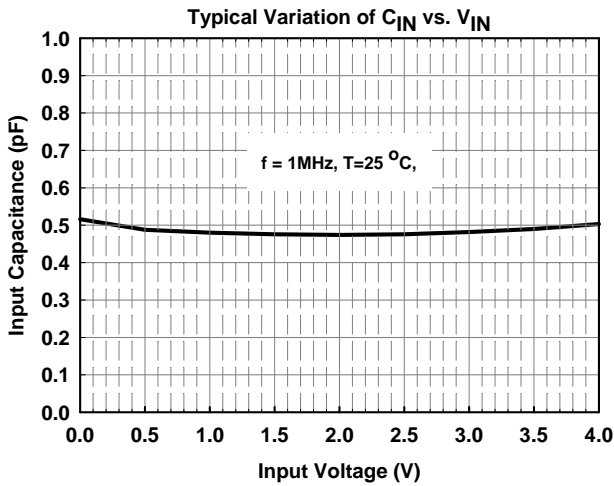


## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Operating Voltage (I/O pin-GND)	$V_{DC}$	6	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	15	kV
ESD per IEC 61000-4-2 (Contact)		10	
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	°C
Operating Temperature	$T_{OP}$	-55 to +85	°C
Storage Temperature	$T_{STO}$	-55 to +150	°C
DC Voltage at any I/O pin	$V_{IO}$	(GND – 0.5) to (VDD + 0.5)	V

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	$V_{RWM}$	Pin-1,-2,-4,-5 to pin-3,-8, T=25 °C			5	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5} = 5V, V_{Pin-3,-8} = 0V, T=25 °C$			1.5	μA
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1mA, T=25 °C, Pin-1,-2,-4,-5$ to pin-3,-8	6			V
Forward Voltage	$V_F$	$I_F = 15mA, T=25 °C, pin-3,-8$ to pin-1,-2,-4,-5		0.9	1.1	V
ESD Clamping Voltage	$V_{clamp}$	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any I/O pin to Ground		12		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+6kV, T=25 °C, Contact mode, any I/O pin to Ground		0.3		Ω
Channel Input Capacitance	$C_{IN}$	$V_{pin-3,-8} = 0V, V_{IN} = 2.5V, f = 1MHz, T=25 °C, any I/O pin to Ground$		0.5	0.65	pF
Channel to Channel Input Capacitance	$C_{CROSS}$	$V_{pin-3,-8} = 0V, V_{IN} = 2.5V, f = 1MHz, T=25 °C, between I/O pins$		0.04	0.08	pF

## Typical Characteristics



## Applications Information

### A. Device Connection

The AZ1045-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1045-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of AZ1045-04F. The ground pins (pin3 and pin8) of AZ1045-04F are the negative reference pins.

These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1045-04F can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

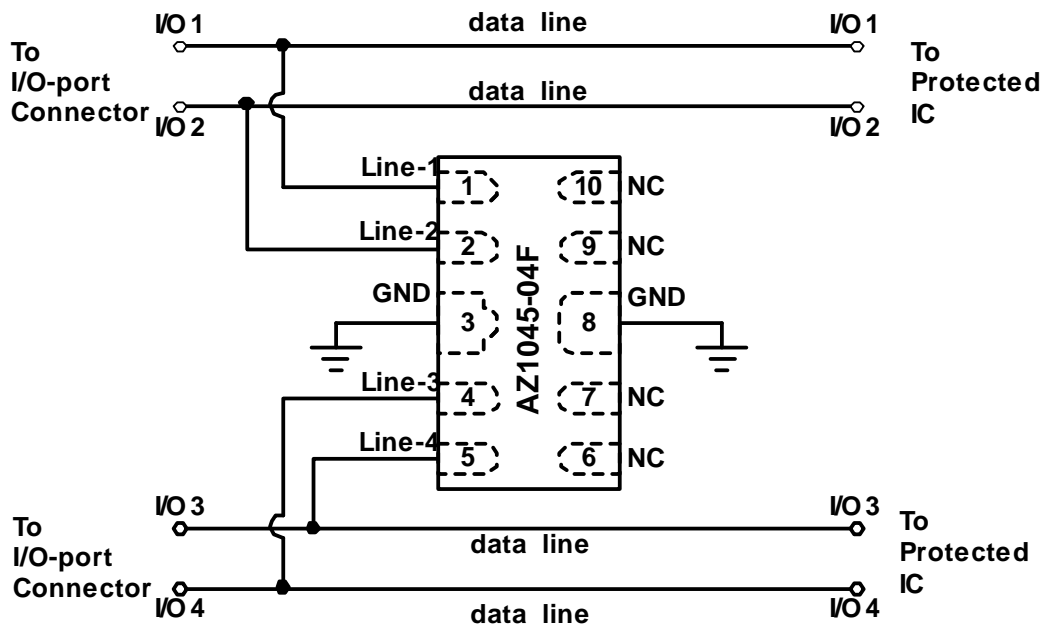


Fig. 1 Data lines connection of AZ1045-04F.

### B. Application

AZ1045-04F is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1045-04F, especially, the HDMI port.

#### HDMI Protection for High and Low speed signals

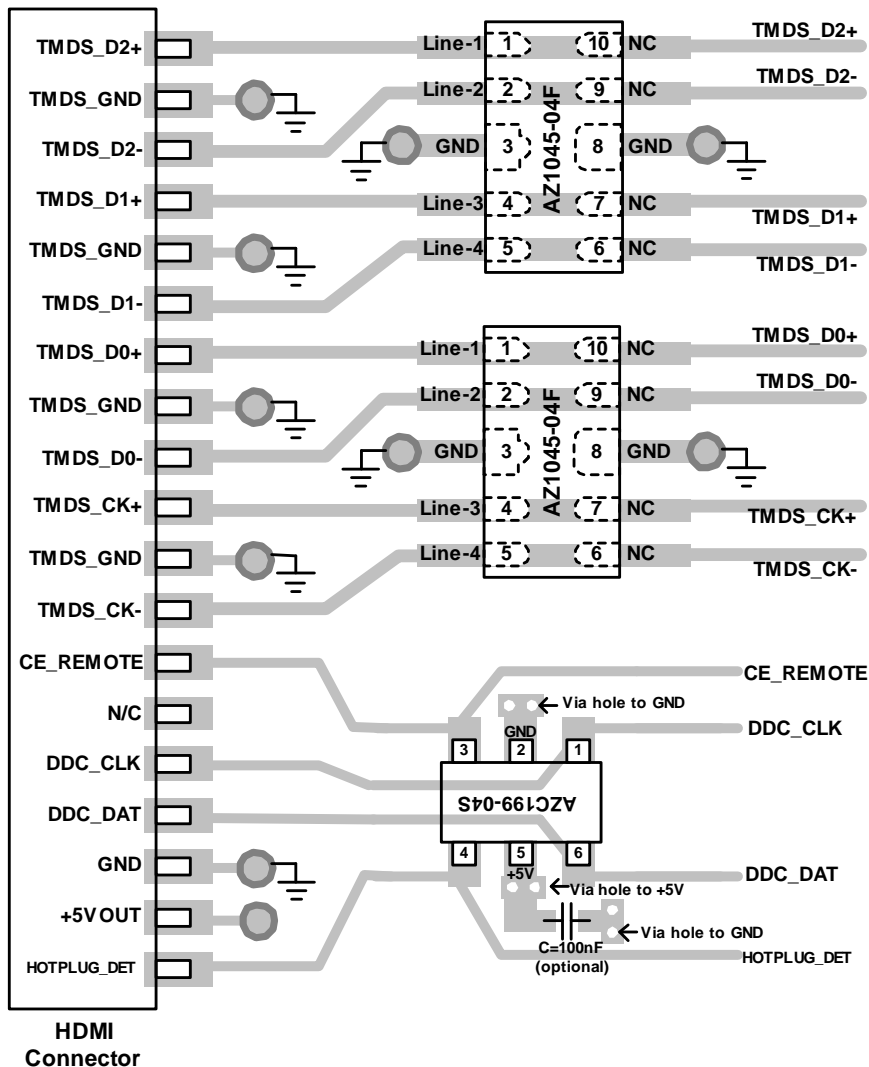
The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on a HDMI port will cause the impedance of the differential pair to drop. Thus, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The AZ1045-04F presents **0.5pF** capacitance to each differential signal while being rated to handle >8kV ESD contact

discharges (>15kV air discharge) as outlined in IEC 61000-4-2. Therefore, it is possible to **make none** adjustment to the board layout parameters to compensate for the added capacitance of the AZ1045-04F. Figure 2 shows how to implement the AZ1045-04F in a HDMI application.

The AZ1045-04F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Figure 2, the best way to design the PCB trace is using the flow through layout. The solid line represents the PCB trace. Note that the PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10,

pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. Lines 2, 3, and 4 have the same way of connection. The ground pins (pin3 and pin8) of AZ1045-04F are the negative reference pins. These pins should be directly connected to the GND plane of PCB. To get minimum parasitic inductance, the path length should keep as short as possible. **In Figure 2, the none-TMDS signals, DDC\_CLK, DDC\_DAT, CE\_REMOTE, and HOTPLUG\_DET, can be protected with another low cost part, e.g., AZC199-04S.**



**Fig. 2 HDMI Protection for High and Low speed signals.**

### C. Measurement Results on a HDMI port

Fig. 3 shows the differential impedance measurement result of a HDMI port without using ESD protection array. The range of the differential impedance is from  $104\Omega$  to  $110\Omega$ , which meets the spec of 100 Ohms +/- 15%. Fig. 4 shows the differential impedance measurement

result of the same HDMI port, but with using the AZ1045-04F ESD protection array. The range of the differential impedance becomes from  $98\Omega$  to  $107\Omega$ , which still meets the spec of 100 Ohms +/- 15%. This demonstrates that **none** adjustment to the board layout parameters is need to compensate for the added ultra small capacitance of the AZ1045-04F

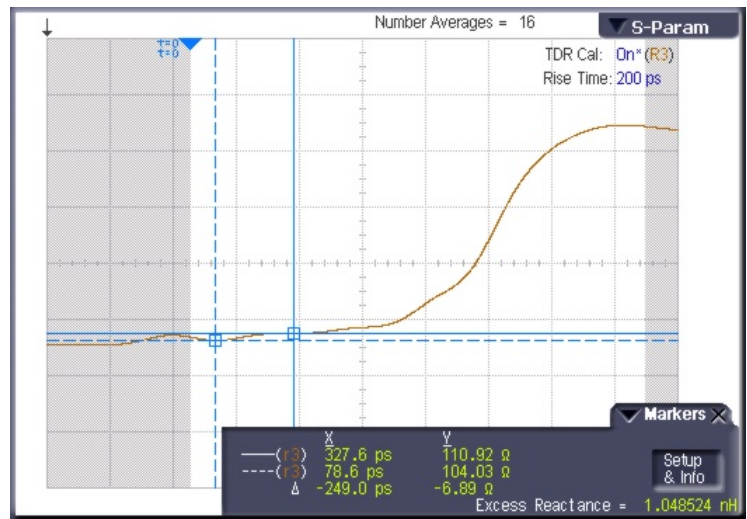
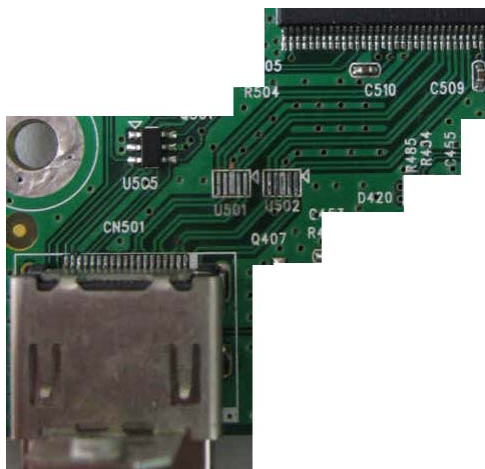


Fig. 3 The measured differential impedance of a HDMI port without using ESD protection array.

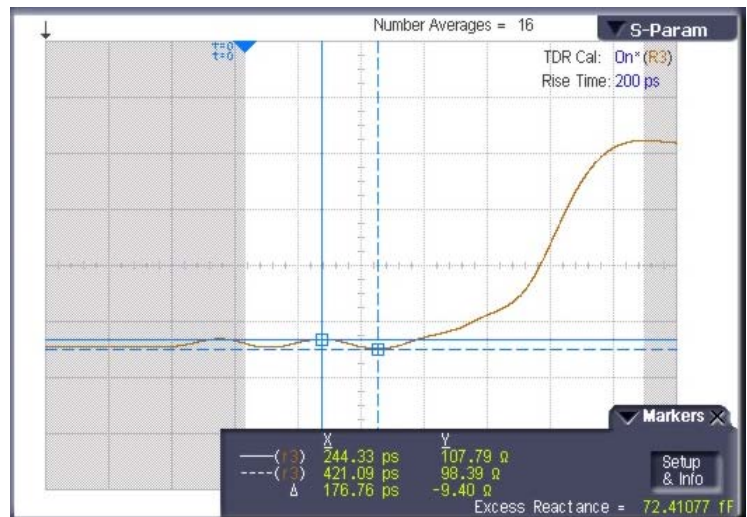
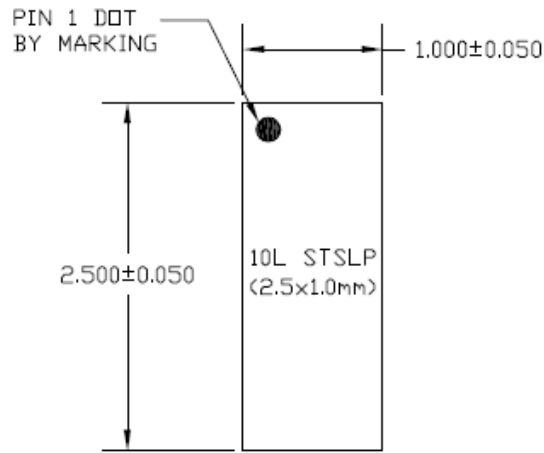
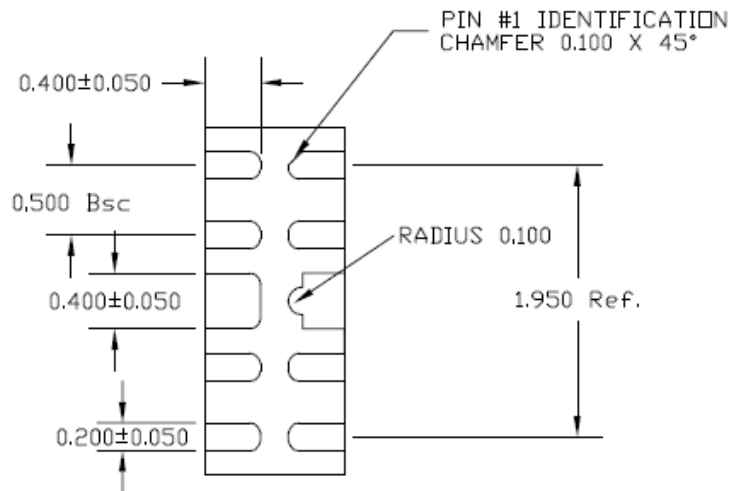


Fig. 4 The measured differential impedance of a HDMI port with using AZ1045-04F ESD protection array. **None** adjustment to the board layout parameters is need.

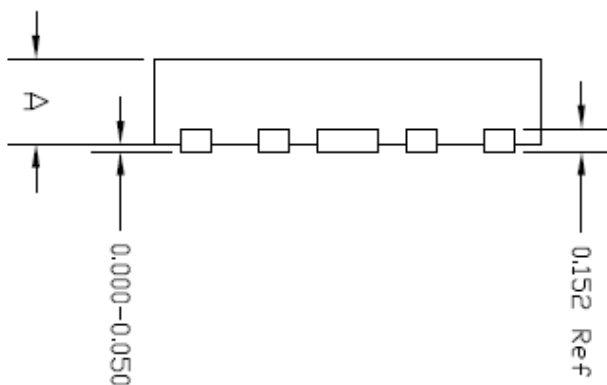
**PACKAGE OUTLINE  
(DFN2510P10E)**



**TOP VIEW (unit in mm)**



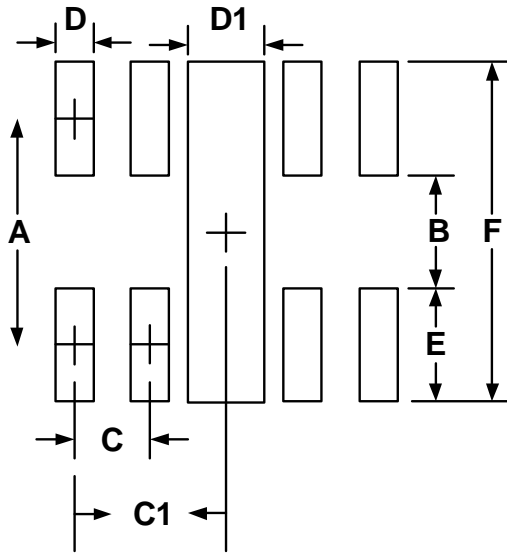
**BOTTOM VIEW (unit in mm)**



**SIDE VIEW (unit in mm)**

A	MIN	0.6 mm
	TYP	0.55 mm
	MAX	0.5 mm

## LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	0.875	0.034
B	0.20	0.008
C	0.50	0.02
C1	1.00	0.039
D	0.2	0.008
D1	0.4	0.016
E	0.675	0.027
F	1.55	0.061

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



117 = Device Code  
X = Date Code  
Y = Control Code

Part Number	Marking Code
AZ1045-04F	117XY



## Revision History

Revision	Modification Description
Revision 2008/12/09	Preliminary Release.
Revision 2009/01/16	The Initial Formal Release.