Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines and one V_{DD} line
- Provide ESD protection for each channel to **IEC 61000-4-2,(ESD) ±19kV (air), ±12kV (contact) IEC 61000-4-5 (Lightning) 4.7A (8/20μs)**
- **For below 5V operating voltage**
- **Ultra low capacitance : 0.55pF typical**
- 0.03pF matching capacitance between the TMDS intra-pair
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Back-drive protection for power-down mode
- Lead-free version available
- Green part available

Applications

- **High Definition Multi-Media Interface (HDMI) 1.3 version**
- **DisplayPort interface**
- **SATA and eSATA interface**
- Digital Visual Interface (DVI)
- USB2.0 up to 480Mb/s
- IEEE 1394 up to 3.2 Gb/s
- Ethernet port: 10/100/1000 Mb/s
- Desktop and Notebooks PCs
- Consumer Electronics
- Set Top Box
- DVDRW Players
- Graphics Cards

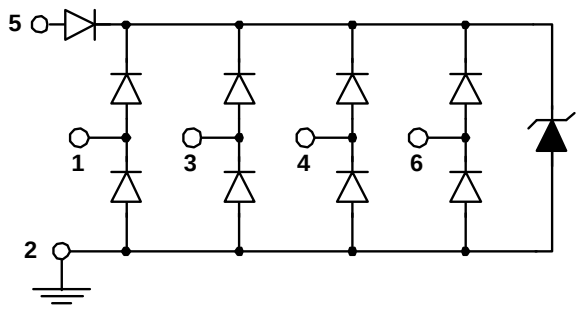
Description

AZ1045-04SU is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1045-04SU has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

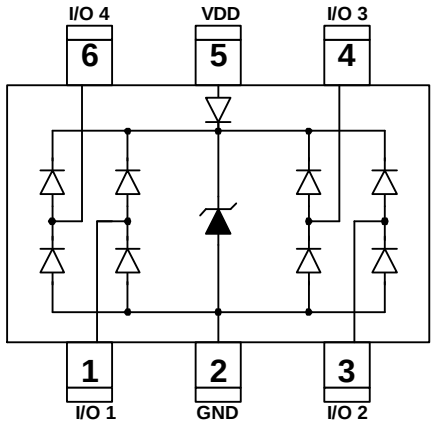
AZ1045-04SU is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. Besides, there is a back-drive protection design in AZ1045-04SU for power-down mode operation.

AZ1045-04SU may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



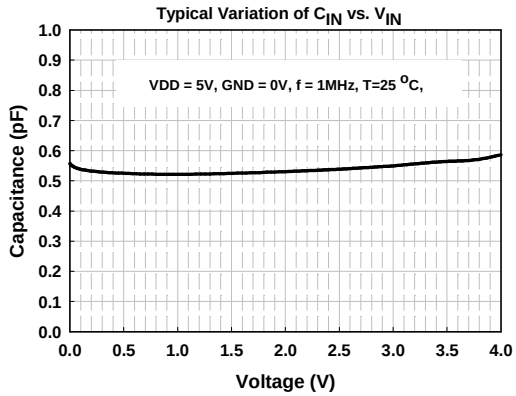
JEDEC SOT23-6L (Top View)

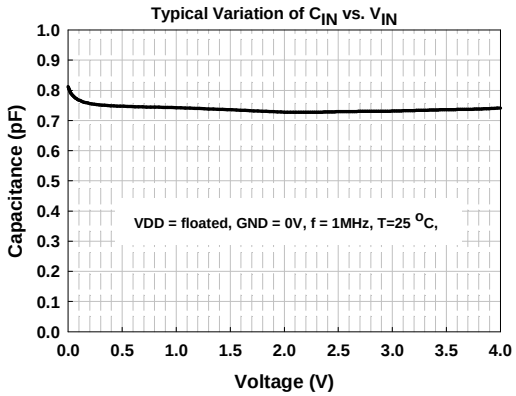
SPECIFICATIONS

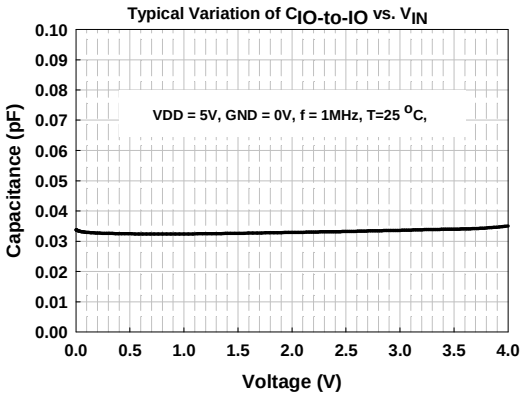
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs) (I/O pins)	I_{PP}	4.7	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air) (I/O pins) ESD per IEC 61000-4-2 (Contact) (I/O pins)	V_{ESD_IO}	19 12	**kV**
ESD per IEC 61000-4-2 (Air) (VDD, GND pins) ESD per IEC 61000-4-2 (Contact) (VDD, GND pins)	V_{ESD_PW}	30 30	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

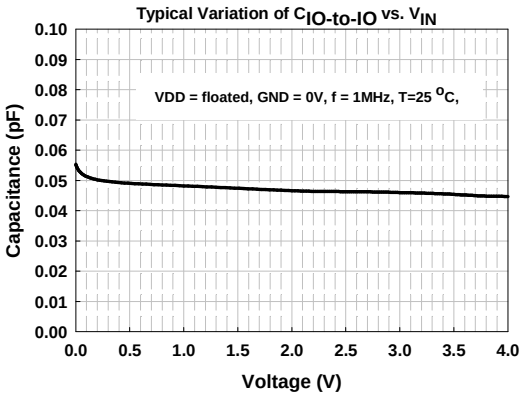
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	**μA**
Channel Leakage Current	$I_{CH-Leak}$	V_{Pin5} = 5V, V_{Pin2} = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 5 to Pin 2	6		9	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 2 to Pin 5		0.8	1	**V**
ESD Clamping Voltage –I/O	V_{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		12		**V**
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9		**V**
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic_io}$	IEC 61000-4-2 0~+6kV,T=25 °C, Contact mode,Any Channel pin to Ground		0.3		**Ω**
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic_VDD}$	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.14		**Ω**
Lightning Clamping Voltage	$V_{lightning}$	I_{PP}=4.7A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.5		**V**
Channel Input Capacitance -1	C_{IN-1}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, Any Channel pin to Ground		0.55	0.65	**pF**
Channel Input Capacitance - 2	C_{IN-2}	**V_{pin5}=floated**,V_{pin2}=0V,**V_{IN}=2.5V**,f=1MHz,T=25°C,Any Channel pin to Ground		0.7	0.9	**pF**
Channel to Channel Input Capacitance -1	$C_{CROSS-1}$	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Between Channel pins		0.03	0.06	**pF**
Channel to Channel Input Capacitance -2	$C_{CROSS-2}$	**V_{pin5} =floated**,V_{pin2} =0V,**V_{IN} =2.5V**,f =1MHz,T=25 °C,Between Channel pins		0.05	0.08	**pF**
Variation of Channel Input Capacitance -1	$\triangle C_{IN-1}$	**V_{pin5} =5V**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.03	0.06	**pF**
Variation of Channel Input Capacitance -2	$\triangle C_{IN-2}$	**V_{pin5} =floated**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.05	0.08	**pF**

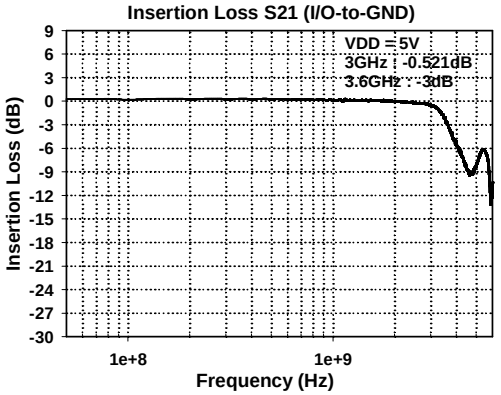
Typical Characteristics

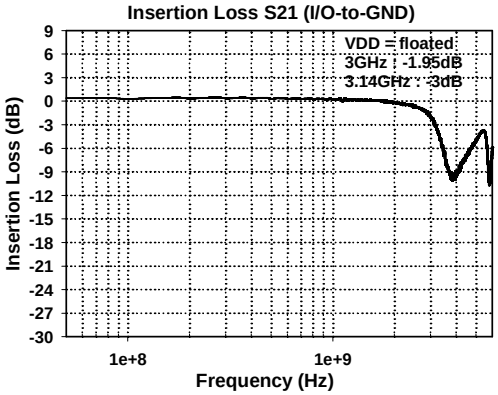


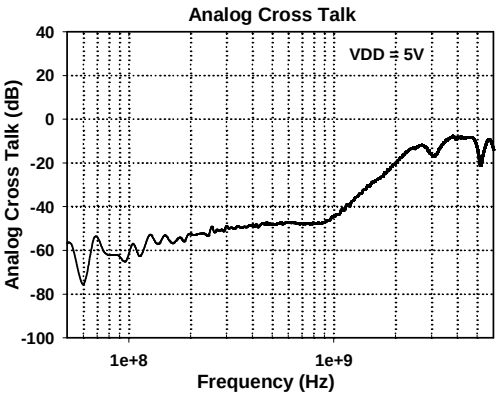


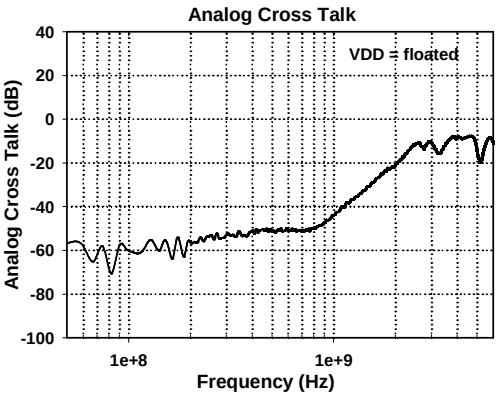


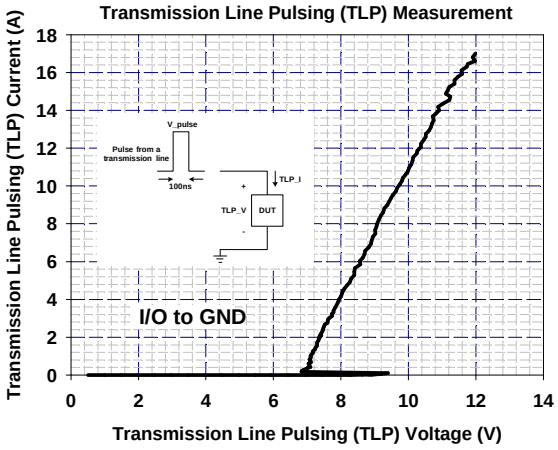


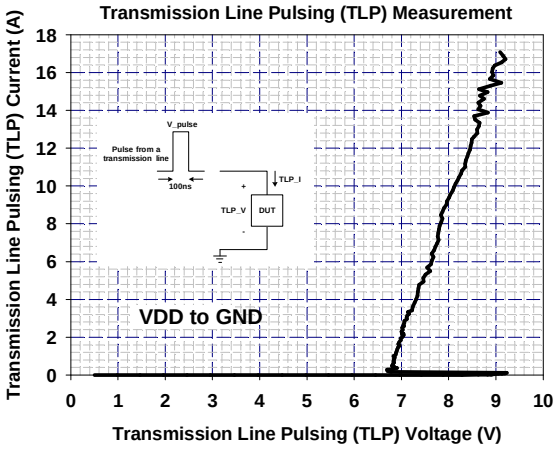









Transmission Line Pulsing (TLP) Measurement
Transmission Line Pulsing (TLP) Current (A)
Transmission Line Pulsing (TLP) Voltage (V)
V_pulse
Pulse from a transmission line
100ns
TLP_I
TLP_V
DUT
I/O to GND


Transmission Line Pulsing (TLP) Measurement
Transmission Line Pulsing (TLP) Current (A)
Transmission Line Pulsing (TLP) Voltage (V)
V_pulse
Pulse from a transmission line
100ns
TLP_I
TLP_V
DUT
VDD to GND

Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + Breakdown voltage drop of D3 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ1045-04SU has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

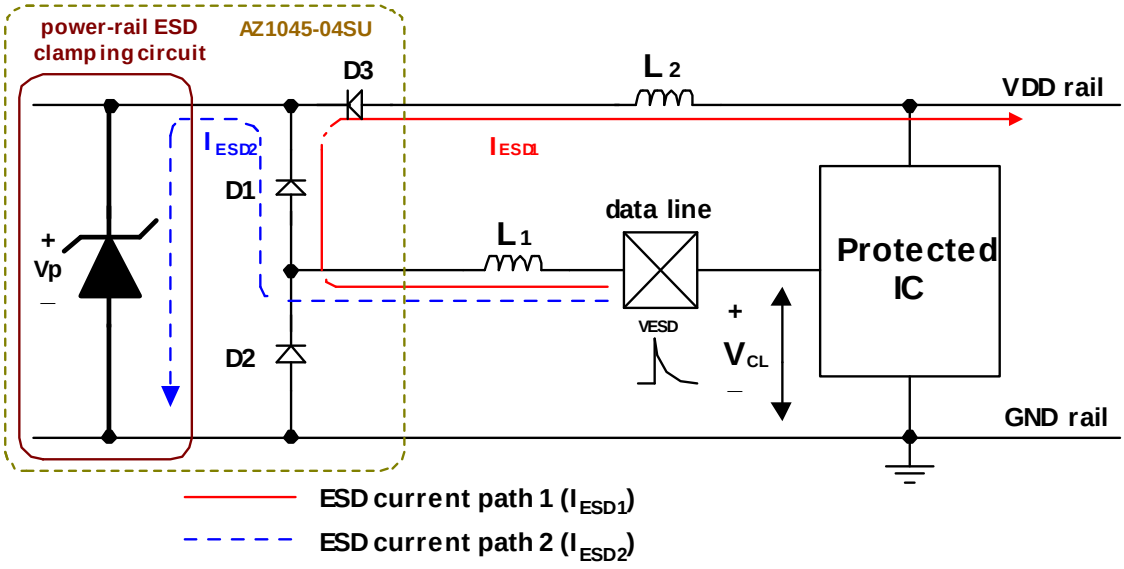


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ1045-04SU is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ1045-04SU is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZ1045-04SU. The ground pin (pin2) of AZ1045-04SU is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZ1045-04SU is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1045-04SU.

AZ1045-04SU can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1045-04SU.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZ1045-04SU can be left as floating. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

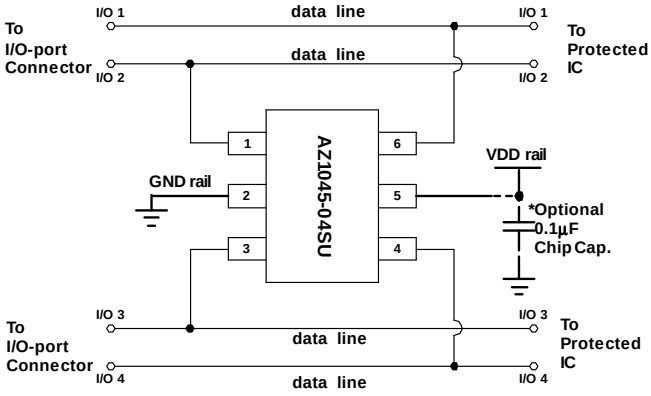


Fig. 2 Data lines and power rails connection of AZ1045-04SU.

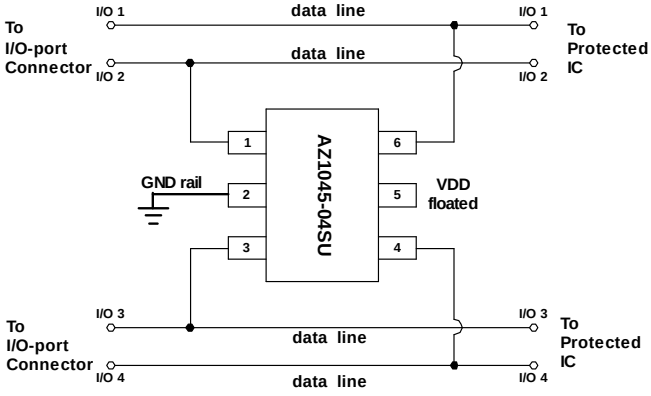


Fig. 3 Data lines and power rails connection of AZ1045-04SU. VDD pin is left as floating when no power rail presented on the PCB.

C. Application

AZ1045-04SU is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1045-04SU, especially, the HDMI port.

HDMI Protection for High and Low speed signals

The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on an HDMI port will cause the impedance of the differential pair to drop. Thus, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The AZ1045-04SU presents **0.55pF** capacitance to each differential signal while being rated to handle >8kV ESD contact discharges (>15kV air discharge) as outlined in IEC 61000-4-2. Therefore, it is possible to **make none or minor** adjustment to the board layout parameters to compensate for the added capacitance of the AZ1045-04SU. Figure 4 shows how to implement the AZ1045-04SU in an HDMI application. **In Figure 4, the none-TMDS signals, DDC_CLK, DDC_DAT, CE_REMOTE, and HOTPLUG_DET, can be protected with another low cost part, e.g., AZC099-04S.**

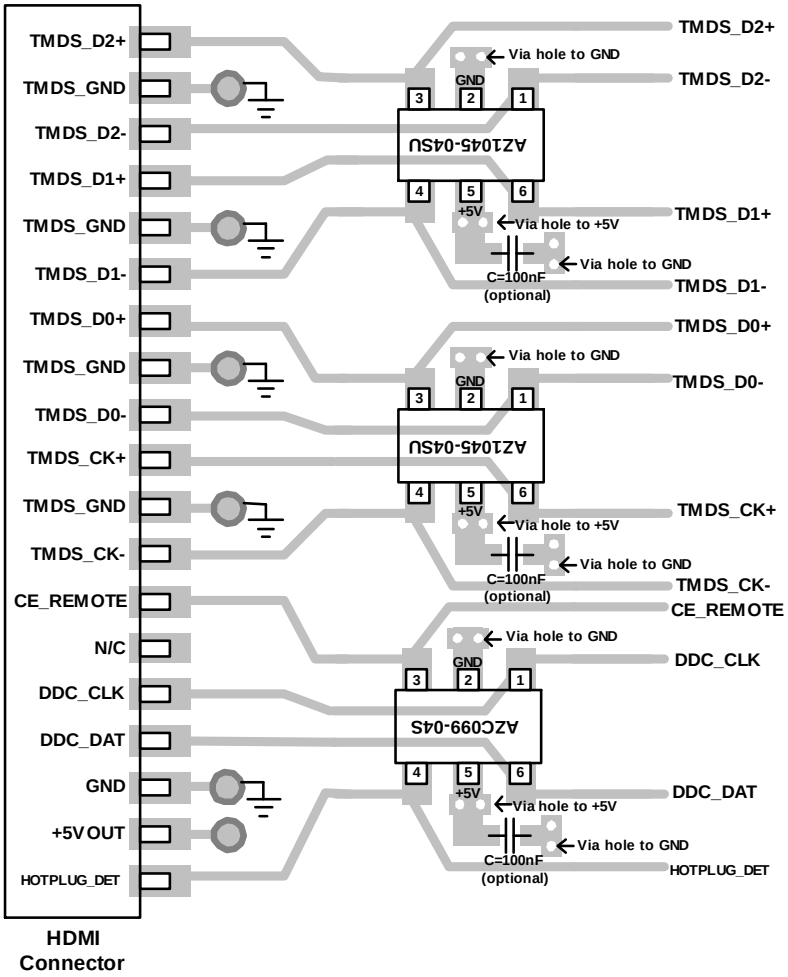


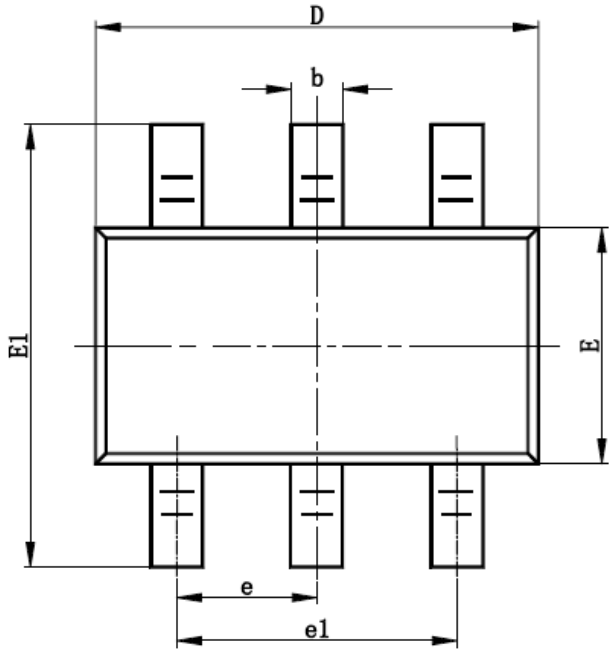
Fig. 4 HDMI Protection for High and Low speed signals.

Mechanical Details

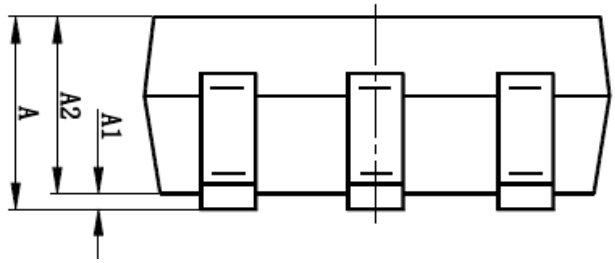
SOT23-6L

PACKAGE DIAGRAMS

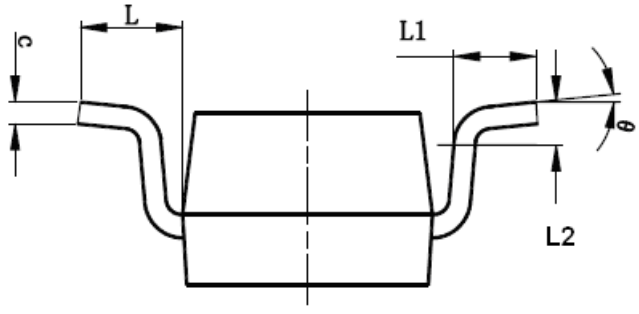
TOP VIEW



SIDE VIEW



END VIEW



PACKAGE DIMENSIONS

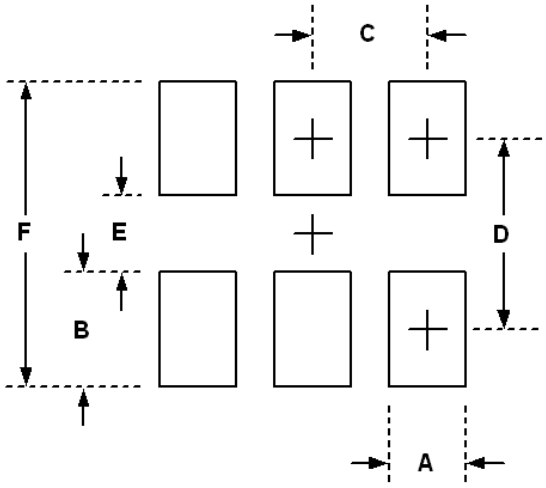
Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.9BSC		0.075BSC	
L1	0.3	0.6	0.012	0.024
L	0.7REF		0.028REF	
L2	0.25BSC		0.010BSC	
Θ	0	8	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

 ©2011 Amazing Micro.

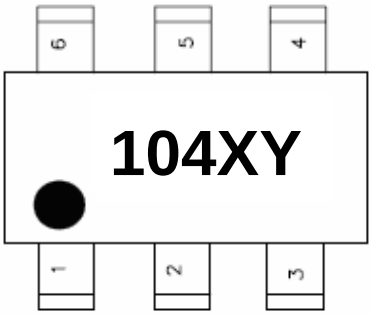
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



104 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ1045-04SU (RoHS)	104XY
AZ1045-04SU (Green part)	**110XY**

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ1045-04SU.R7G	Green	T/R	7 inch	4 reel= 12,000/box	6 box =72,000/carton

Revision History

Revision	Modification Description
Revision 2007/06/13	Original Release.
Revision 2007/06/22	Update the “Forward Voltage” in the Electrical Characteristics.
Revision 2007/09/17	1. Add the surge (8/20us) characteristic results. 2. Update the max. values of C_{IN-1} and C_{IN-2}.
Revision 2007/12/18	1. Add application for “DisplayPort” and “SATA” 2. Update “For HDMI Transceiver Port” to “For High Speed I/O Port” in headline
Revision 2008/01/23	Present the Mechanical Details by JEDEC formation.
Revision 2008/09/29	Add the marking code for Green part.
Revision 2009/10/20	Change the description of ESD level in the Features to be the same as that in ABSOLUTE MAXIMUM RATINGS.
Revision 2009/10/27	Update the PACKAGE DIMENSIONS.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.