Features

- ESD protect for 4 high-speed I/O channels
- Provide transient protection for each channel to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 30A (8/20μs) for any I/O-to-GND
  IEC 61000-4-5 (Lightning) 37A (8/20μs) for VDD-to-GND
- For low operating voltage applications: 5V maximum
- Low capacitance : 1.8pF typical
- Fast turn-on and low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Video graphics cards
- LAN application
- USB2.0 power and data lines protection
- Notebook and PC computers
- Monitors and flat panel displays

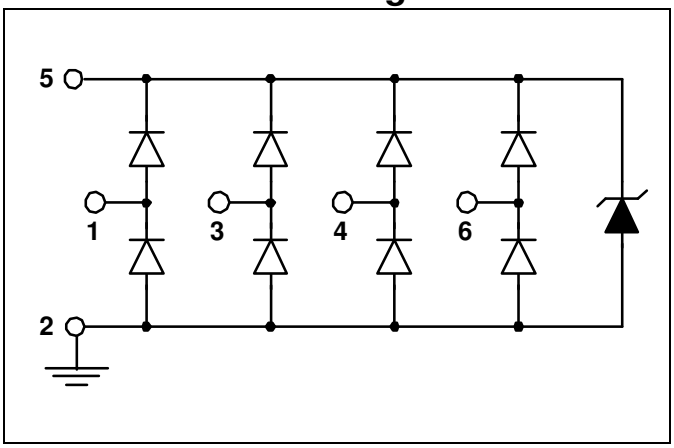
Description

AZ1515-04S is a high-performance design which includes surge rated diode arrays to protect high-speed data interfaces. The AZ1515-04S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

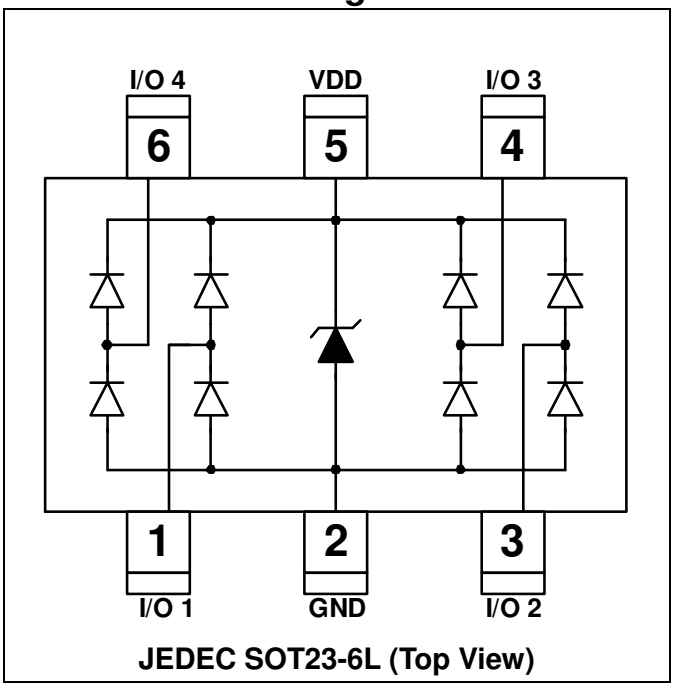
AZ1515-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ1515-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



JEDEC SOT23-6L (Top View)

SPECIFICATIONS

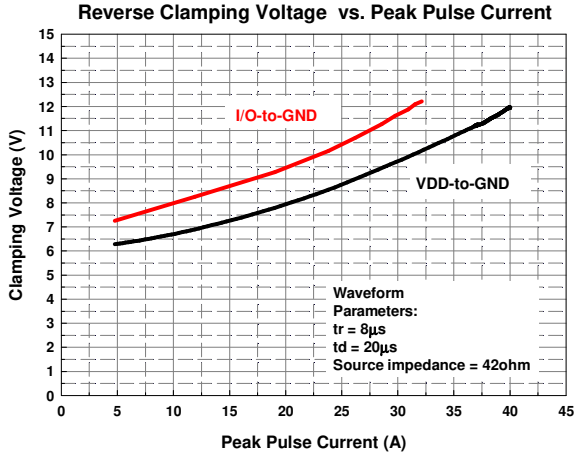
ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs, any I/O-to-GND)	I_{PP}	30	A
Peak Pulse Current (tp =8/20μs, VDD-to-GND)	I_{PP}	37	A
Operating Supply Voltage (VDD-to-GND)	V_{DC}	5.5	V
ESD per IEC 61000-4-2 (Air / Contact)	V_{ESD}	30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C.			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, pin 5 to pin 2.			1	μA
Channel Leakage Current	$I_{CH-Leak}$	V_{pin5} = 5V, V_{pin2} = 0V, T=25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin 5 to pin 2.	6		9.5	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin 2 to pin 5.		0.7	1	V
ESD Clamping Voltage –I/O (Note 1)	$V_{CL\_ESD\_I/O}$	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, any I/O pin to GND.		9		V
ESD Clamping Voltage –VDD (Note 1)	$V_{CL\_ESD\_VDD}$	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, VDD pin to GND.		7		V
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic\_I/O}$	IEC 61000-4-2, 0~+8kV, T=25 °C, Contact mode, any I/O pin to GND.		0.1		Ω
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2, 0~+8kV, T=25 °C, Contact mode, VDD pin to GND.		0.05		Ω
Surge Clamping Voltage –I/O	$V_{CL\_surge\_I/O}$	I_{PP}=30A, tp=8/20μs, T=25 °C, any I/O pin to GND.		11.5		V
Surge Clamping Voltage –VDD	$V_{CL\_surge\_VDD}$	I_{PP}=37A, tp=8/20μs, T=25 °C,VDD pin to GND.		11.2		V
Channel Input Capacitance	C_{IN}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, any I/O pin to GND.		1.8	2.5	pF
		V_{pin5} =floated, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, any I/O pin to GND.		2.3	3	pF
Channel to Channel Capacitance	$C_{I/O-to-I/O}$	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, between I/O pins.		0.18	0.3	pF
		V_{pin5} =floated, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, between I/O pins.		0.26	0.45	pF

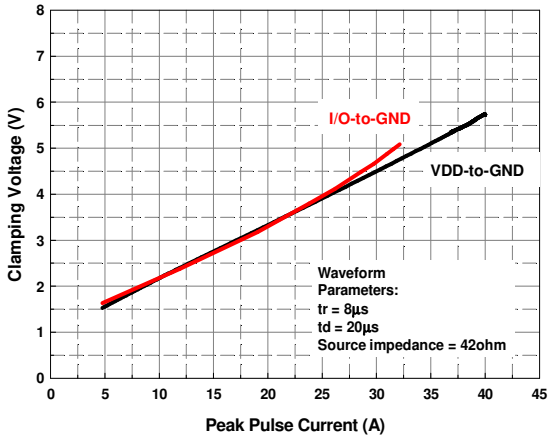
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

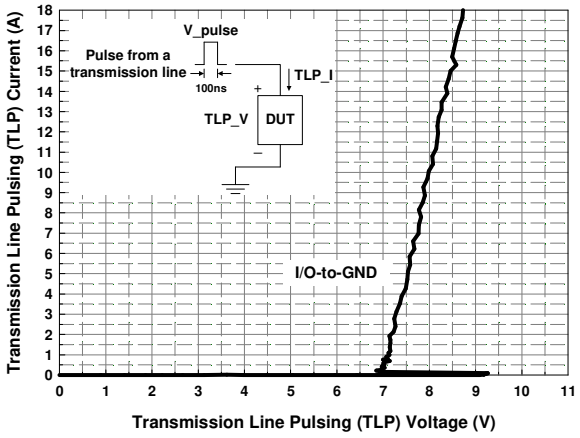
Reverse Clamping Voltage vs. Peak Pulse Current



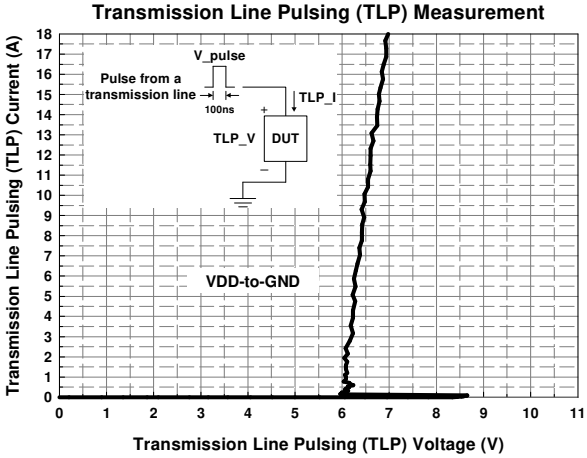
Forward Clamping Voltage vs. Peak Pulse Current



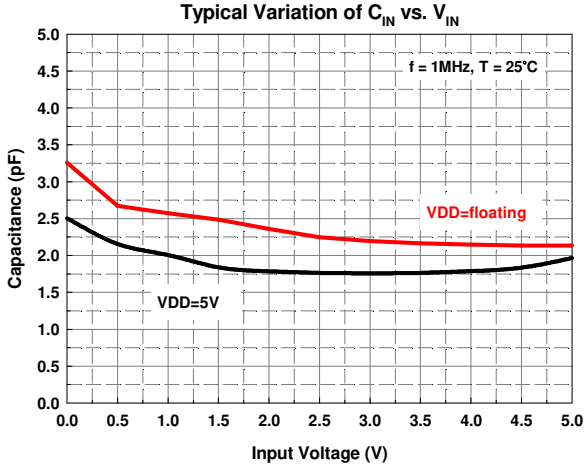
Transmission Line Pulsing (TLP) Measurement



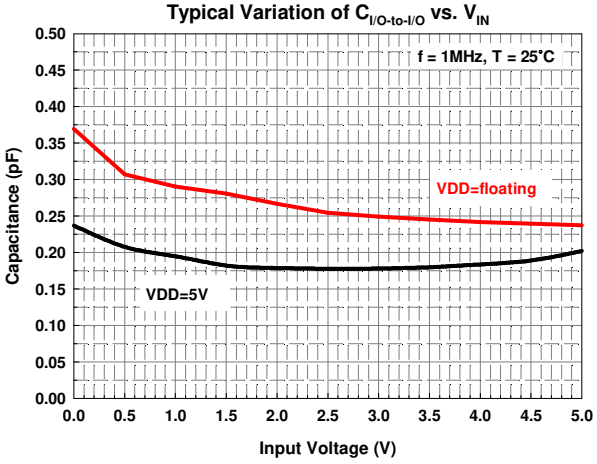
Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Typical Variation of $C_{I/O\text{-}to\text{-}I/O}$ vs. V_{IN}



Applications Information

A. Design Considerations

The ESD protection scheme for the system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are generally used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of the data line can be described as follow :

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ1515-04S has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

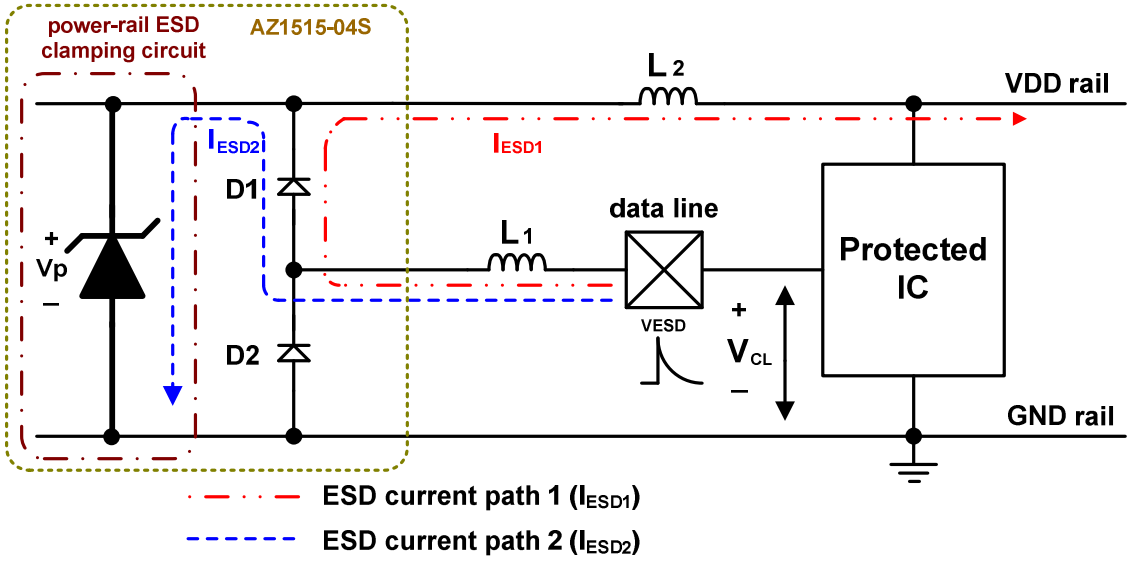


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ1515-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ1515-04S is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZ1515-04S. The ground pin (pin2) of AZ1515-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZ1515-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1515-04S.

AZ1515-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1515-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZ1515-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

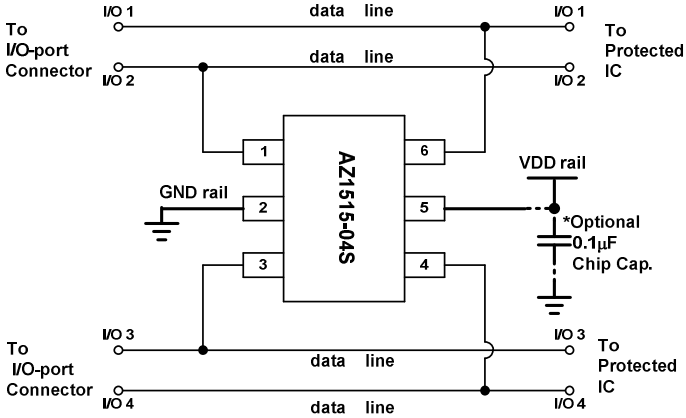


Fig. 2 Data lines and power rails connection of AZ1515-04S.

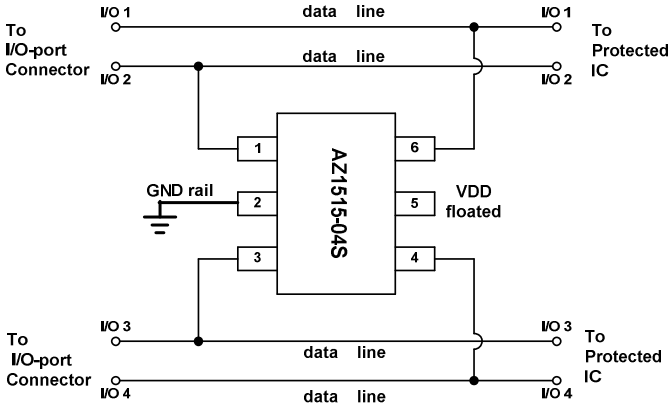


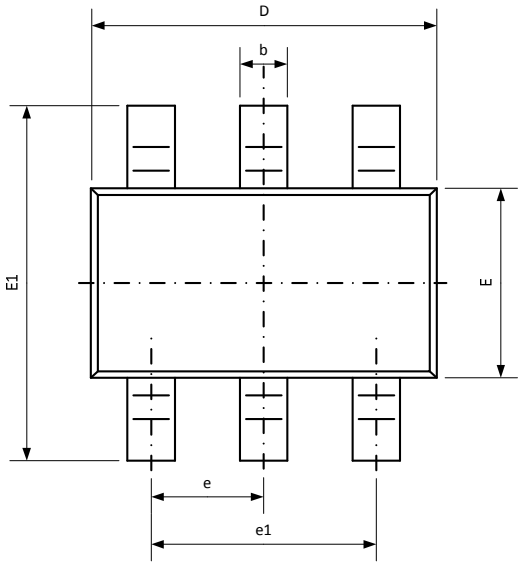
Fig. 3 Data lines and power rails connection of AZ1515-04S. VDD pin is left as floating when no power rail presented on the PCB.

Mechanical Details

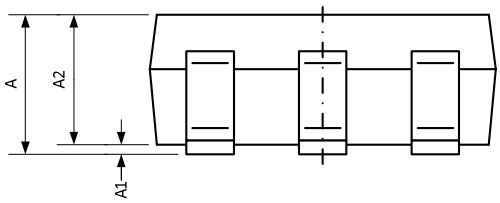
SOT23-6L

PACKAGE DIAGRAMS

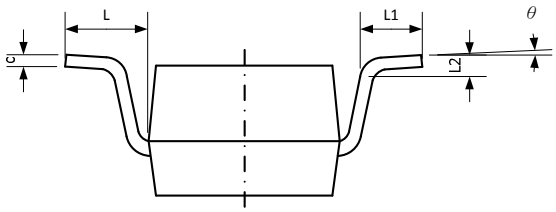
TOP VIEW



SIDE VIEW



END VIEW



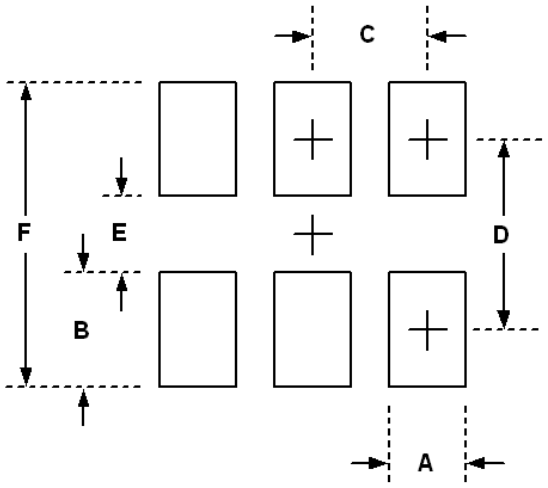
PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	--	1.25
A1	0.00	0.10
A2	0.90	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	1.40	1.80
E1	2.60	3.00
e	0.95BSC	
e1	1.90BSC	
L1	0.30	0.60
L	0.70REF	
L2	0.25BSC	
ϴ	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters.

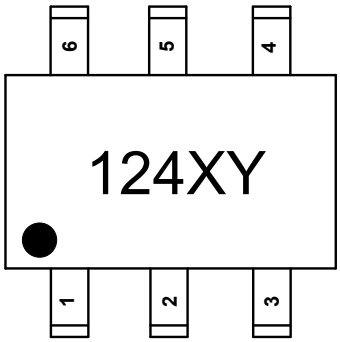
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



124 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ1515-04S.R7G (Green Part)	124XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1515-04S.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2018/01/23	Formal Release.