



Features

- ESD/Surge Protection for 1 Line with Bidirectional.
- Provide ESD protection for each line to **IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air / contact)**
IEC 61000-4-4 (EFT) 80A (5/50ns)
IEC 61000-4-5 (Lightning) 21A (8/20 μs)
- Suitable for, **5.0V** and below, operating voltage applications
- Low capacitance : 1.9pF typical
- High surge protection
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

Applications

- xDSL Line Protection
- WAN/LAN Device
- 10/100/1000 Ethernet
- Power Supply Protection
- USB Interface Protection
- RF Interface Protection
- Peripherals

Description

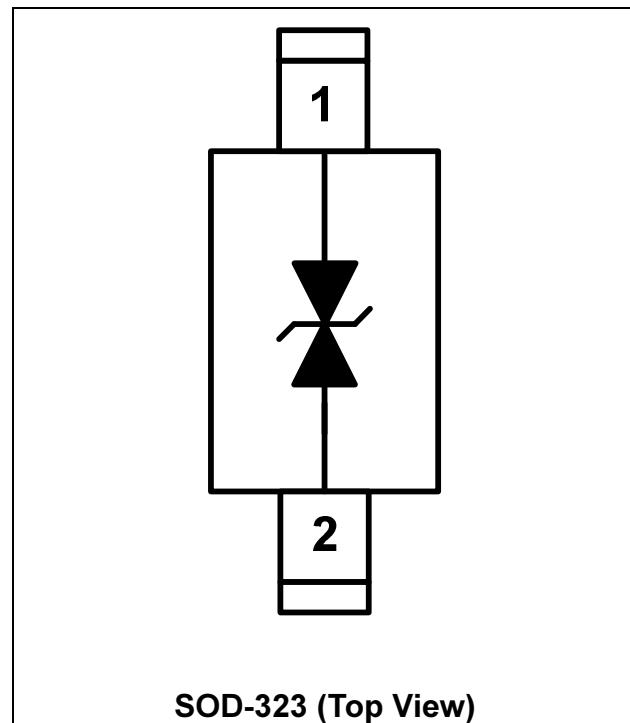
AZ1615-01L is a design which includes a bi-directional ESD rated clamping cell to protect one power line, or one control line, or one high speed data line in an electronic system. The AZ1615-01L has been specifically designed to protect sensitive components which are connected to data and transmission lines from

over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ1615-01L is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ1615-01L may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration



SOD-323 (Top View)



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current ($t_p=8/20\mu s$)	I_{PP}	21	A
Operating Supply Voltage	V_{DC}	± 5.5	V
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 30	kV
ESD per IEC 61000-4-2 (Contact)		± 30	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	$T=25\text{ }^{\circ}\text{C}$	-5.0		5.0	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = \pm 5\text{ V}, T=25\text{ }^{\circ}\text{C}$			0.5	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1\text{ mA}, T=25\text{ }^{\circ}\text{C}$	6		9	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP}= 5\text{ A}, t_p=8/20\mu\text{s}, T=25\text{ }^{\circ}\text{C}$		7.5		V
		$I_{PP}= 21\text{ A}, t_p=8/20\mu\text{s}, T=25\text{ }^{\circ}\text{C}$		12		
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2, +8kV ($I_{TLP} = 16\text{ A}$), Contact mode, $T=25\text{ }^{\circ}\text{C}$		9.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, $T=25\text{ }^{\circ}\text{C}$, Contact mode		0.16		Ω
Channel Input Capacitance	C_{IN}	$V_R = 0\text{ V}, f = 1\text{ MHz}, T=25\text{ }^{\circ}\text{C}$		1.9	3.0	pF

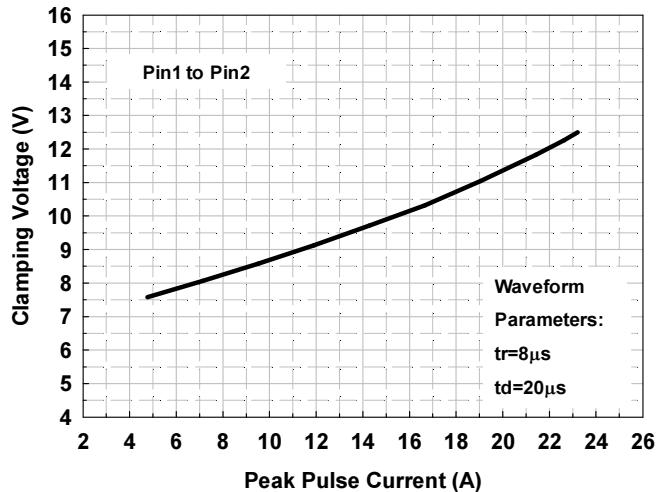
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100\text{ ns}$, $t_f = 1\text{ ns}$.

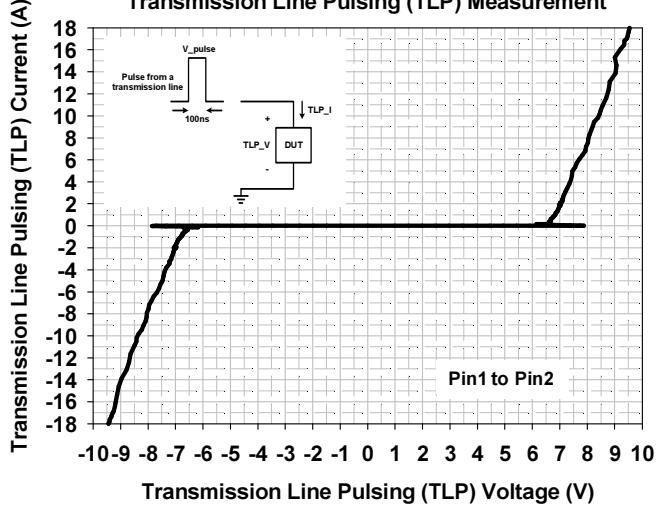


Typical Characteristics

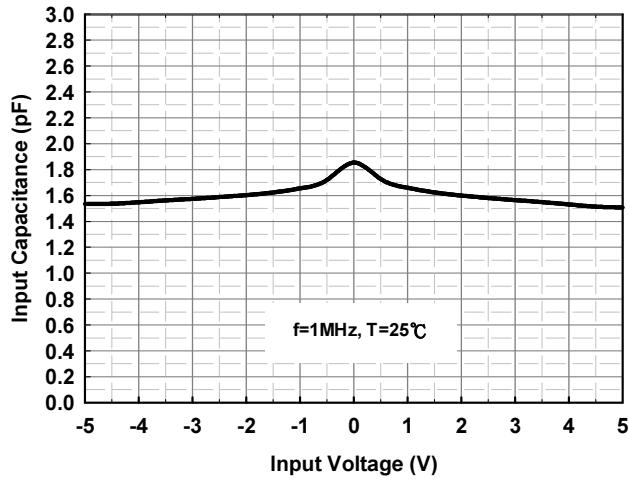
Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}





Applications Information

The AZ1615-01L is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.

The usage of the AZ1615-01L is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ1615-01L should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ1615-01L.
- Place the AZ1615-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

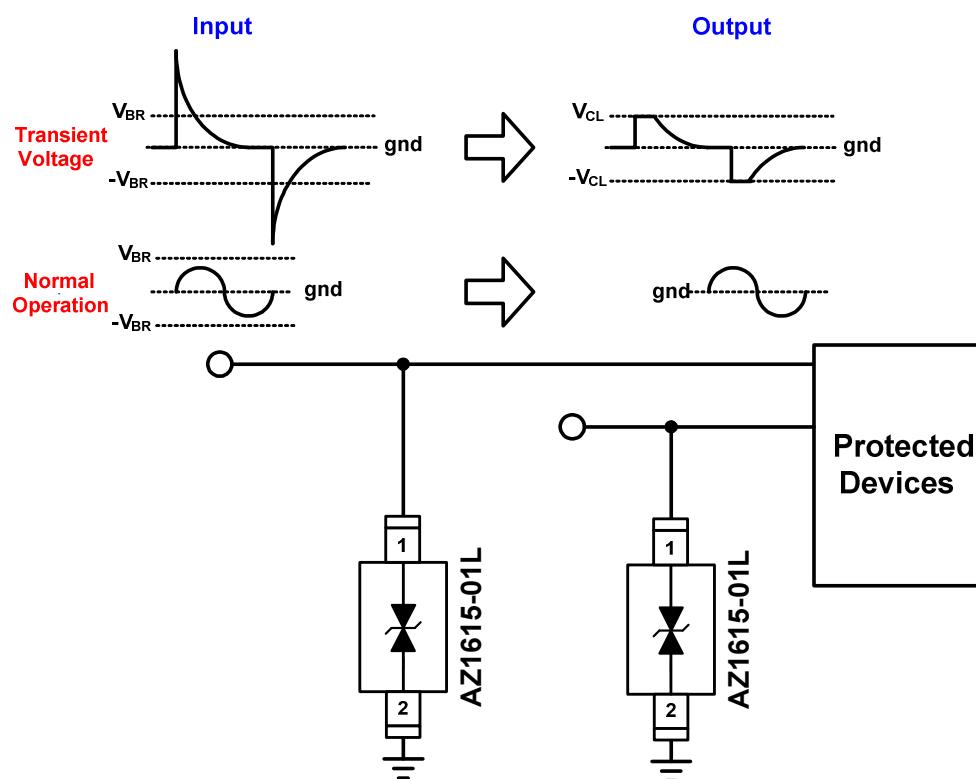


Fig. 1



Fig. 2 shows another simplified example of using AZ1615-01L to protect the control line, high

speed data line, and power line from ESD transient stress.

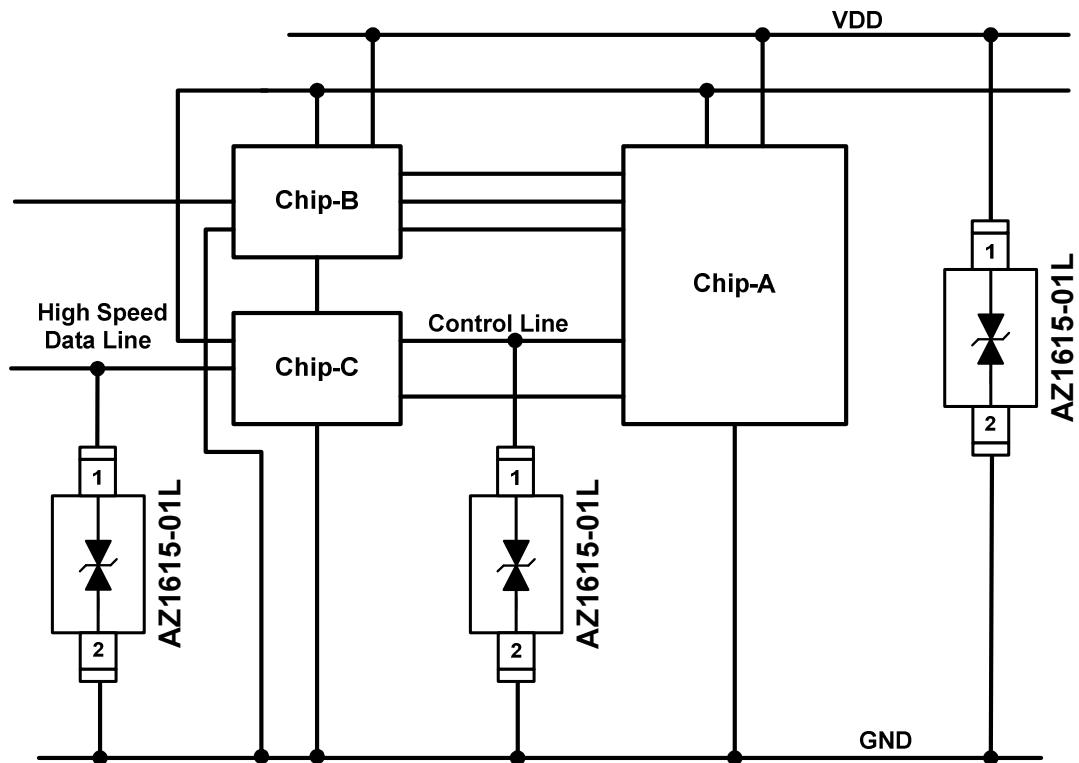


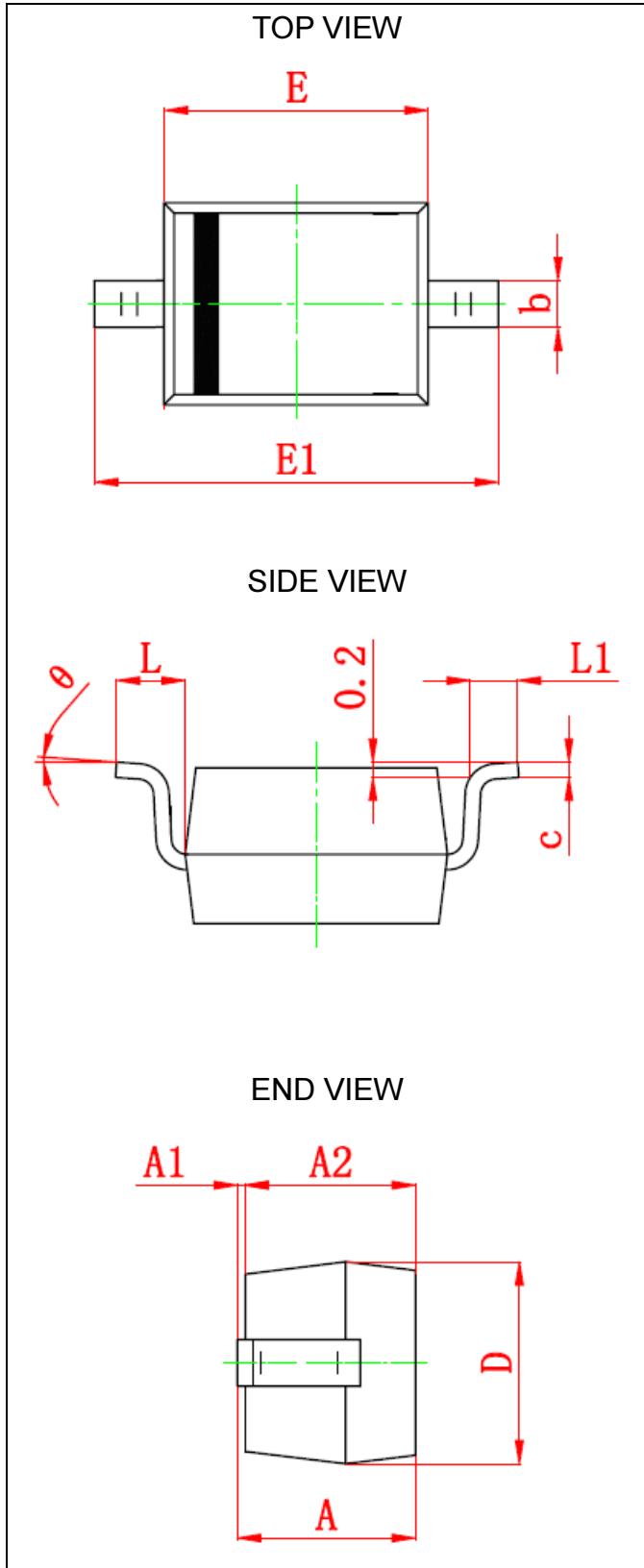
Fig. 2



Mechanical Details

SOD-323

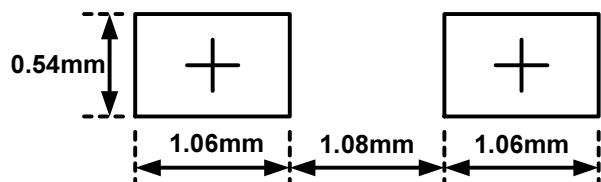
PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.8	1.0	0.031	0.039
A1	0	0.1	0.000	0.004
A2	0.8	0.9	0.031	0.035
b	0.25	0.35	0.010	0.014
C	0.08	0.15	0.003	0.006
D	1.2	1.4	0.047	0.055
E	1.6	1.8	0.063	0.071
E1	2.5	2.7	0.098	0.106
L	0.475REF		0.019 REF	
L1	0.25	0.4	0.010	0.016
θ	0°	8°	0°	8°

LAND LAYOUT

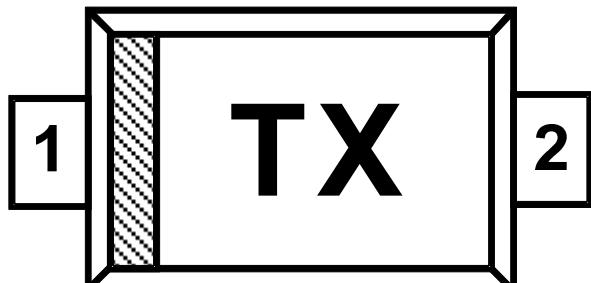


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



MARKING CODE



Top View

T = Device Code
X = Date Code

Part Number	Marking Code
AZ1615-01L.R7G (Green Part)	TX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1615-01L.R7G	Green	T/R	7 inch	3,000/reel	4 reels= 12,000/box	6 boxes =72,000/carton

Revision History

Revision	Modification Description
Revision 2016/10/14	Preliminary Release.
Revision 2017/05/11	Formal Release.