

Features

- ESD protection for 8 I/O channels
- Provide transient protection for each line to
IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 13\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 6A (8/20 μs)
- For low operating voltage of 3.3V and below
- Fast turn-on and ultra-low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Mini LED / Micro LED
- Power line protection
- Low speed data line protection
- Portable devices
- Peripheral products

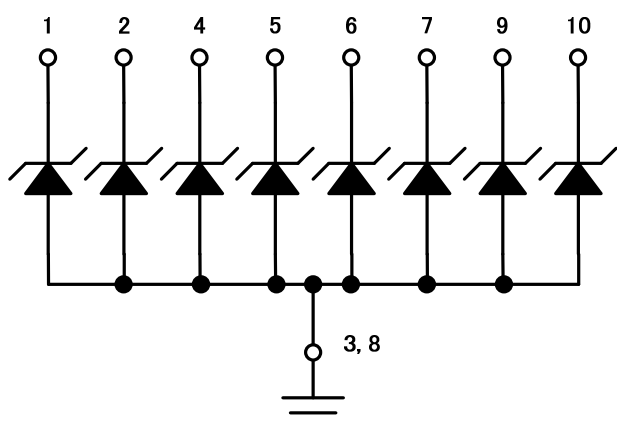
Description

AZ2113-08F is a design which includes ESD rated clamping cell arrays to protect the power lines or data/control lines in an electronic system. The AZ2113-08F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

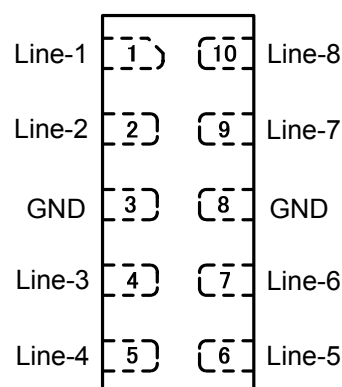
AZ2113-08F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ2113-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram



Pin Configuration



DFN2510P10E (Top View)

Specifications

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise specified)			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ($t_p = 8/20\mu\text{s}$)	I_{PP}	6	A
Operating Voltage (I/O pin-GND)	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 15	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 13	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^\circ\text{C}$
Operating Temperature	T_{OP}	-55 to +125	$^\circ\text{C}$
Storage Temperature	T_{STO}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2,-4,-5,-6,-7,-9,-10 to pin-3,-8, $T = 25^\circ\text{C}$.			3.3	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5,-6,-7,-9,-10} = 3.3\text{V}$, $V_{Pin-3,-8} = 0\text{V}$, $T = 25^\circ\text{C}$.			0.1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1\text{mA}$, pin-1,-2,-4,-5,-6,-7,-9,-10 to pin-3,-8, $T = 25^\circ\text{C}$.	4.5		7.0	V
Forward Voltage	V_F	$I_F = 15\text{mA}$, pin-3,-8 to pin-1,-2,-4,-5,-6,-7,-9,-10, $T = 25^\circ\text{C}$.	0.6		1.0	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 5\text{A}$, $T = 25^\circ\text{C}$, any I/O pin to GND.		5		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16\text{A}$), contact mode, $T = 25^\circ\text{C}$, any I/O pin to GND.		7		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, $T = 25^\circ\text{C}$, contact mode, any I/O pin to GND.		0.18		Ω
Channel Input Capacitance	C_{IN}	$V_{pin-3,-8} = 0\text{V}$, $V_{IN} = 0\text{V}$, $f = 1\text{MHz}$, $T = 25^\circ\text{C}$, any I/O pin to GND.		28	40	pF

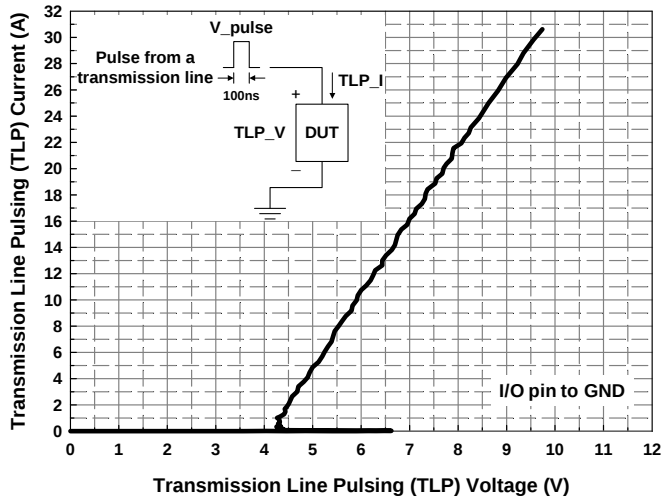
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100\text{ns}$, $t_r = 1\text{ns}$.

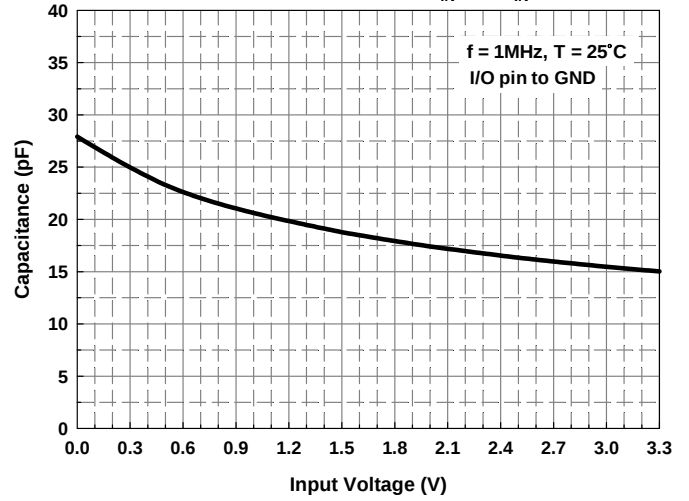


Typical Characteristics

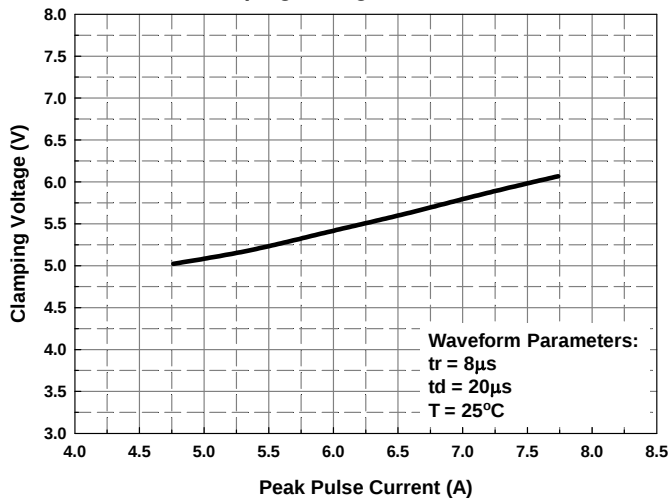
Transmission Line Pulsing (TLP) Measurement



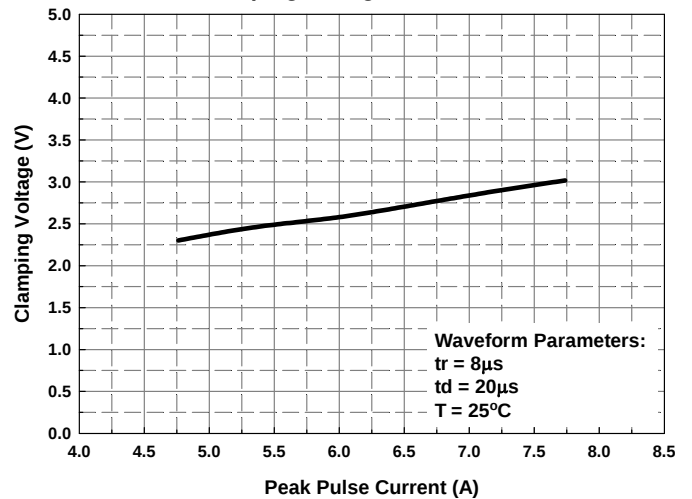
Typical Variation of C_{IN} vs. V_{IN}



Reverse Clamping Voltage vs. Peak Pulse Current



Forward Clamping Voltage vs. Peak Pulse Current





Application Information

The AZ2113-08F is designed to protect 8 low speed lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ2113-08F is shown in the Fig. 1. In Fig. 1, the 8 protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin6, pin7, pin9 and pin10) of AZ2113-08F. The ground pins (pin3 and pin8) of AZ2113-08F are the negative

reference pins. These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should be kept as short as possible.

AZ2113-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be simply left as NC pins.

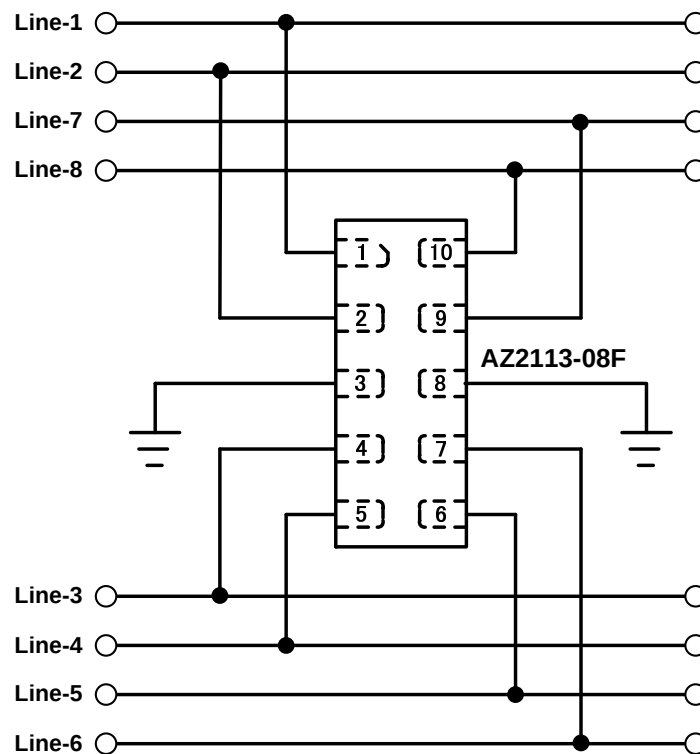
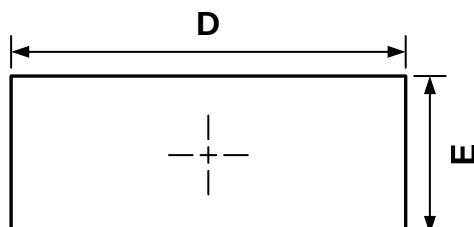


Fig. 1 Data lines connection of AZ2113-08F.

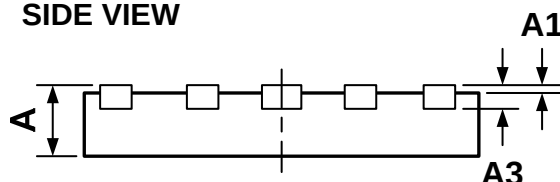
Mechanical Details

DFN2510P10E PACKAGE DIAGRAMS AND DIMENSIONS

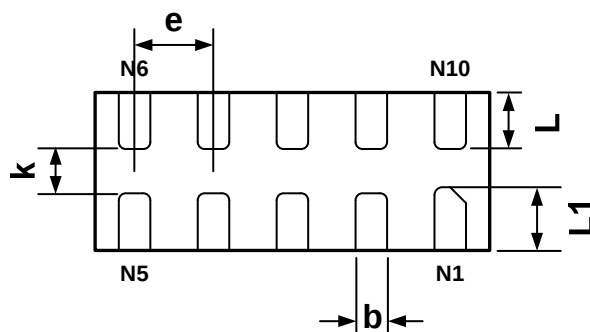
TOP VIEW



SIDE VIEW



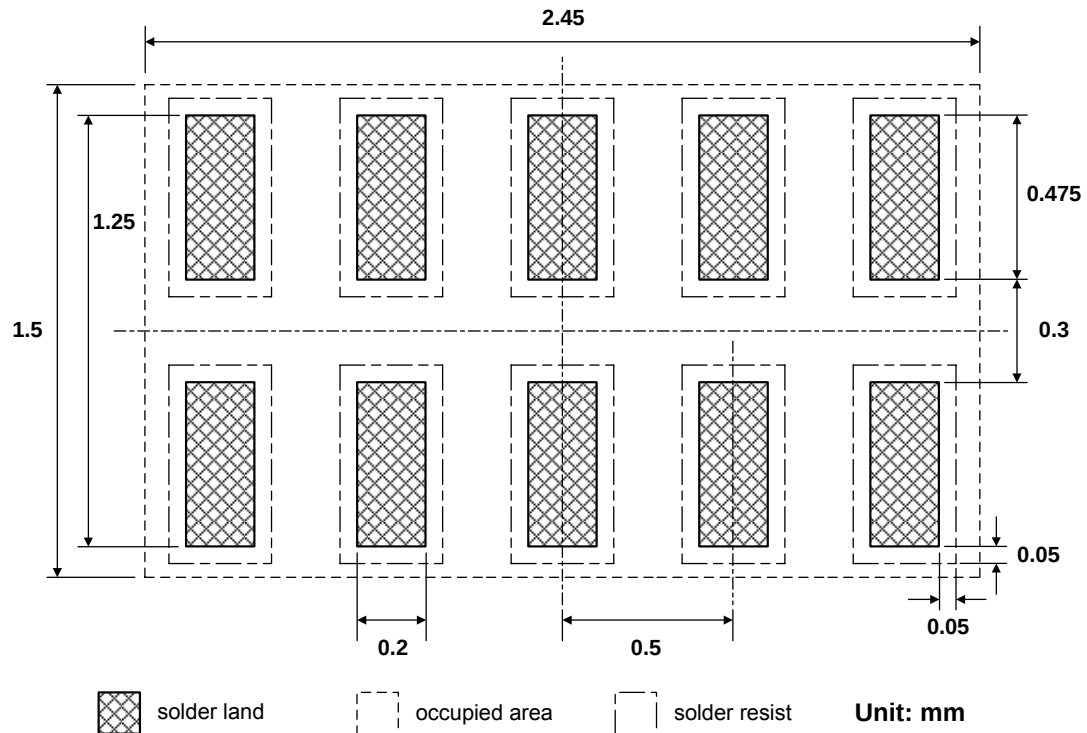
BOTTOM VIEW



SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	0.450	0.550
A1	-	0.050
A3	0.152 REF	
b	0.150	0.250
D	2.400	2.600
E	0.900	1.100
e	0.500 BSC	
L	0.300	0.400
L1	0.350	0.450
k	0.300 REF	



LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



211 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ2113-08F.R7G (Green Part)	211XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ2113-08F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2021/03/26	Formal Release.