



Features

- ESD Protect for 5 Lines with Unidirectional.
- Provide Transient protection for each line directly to
IEC 61000-4-2 (ESD) $\pm 16\text{kV}$ (air), $\pm 10\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 35A (5/50ns)
IEC 61000-4-5 (Lightning) 3.5~ 6A (8/20 μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, and 2.5V etc.
- Fast turn-on and Low clamping voltage
- Array of surge rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players
- Peripherals

Description

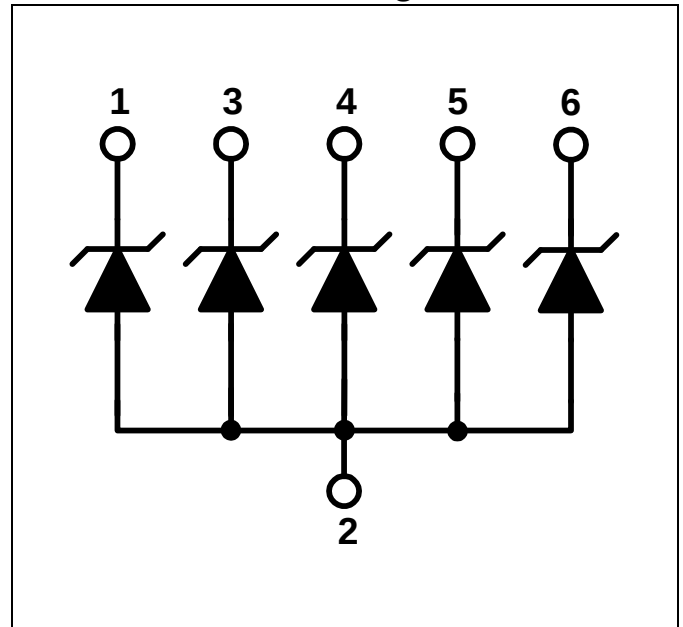
AZ2115-05F is a design which includes surge rated clamping cell arrays to protect the power lines or data/control lines in an electronic systems. The AZ2115-05F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZ2115-05F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

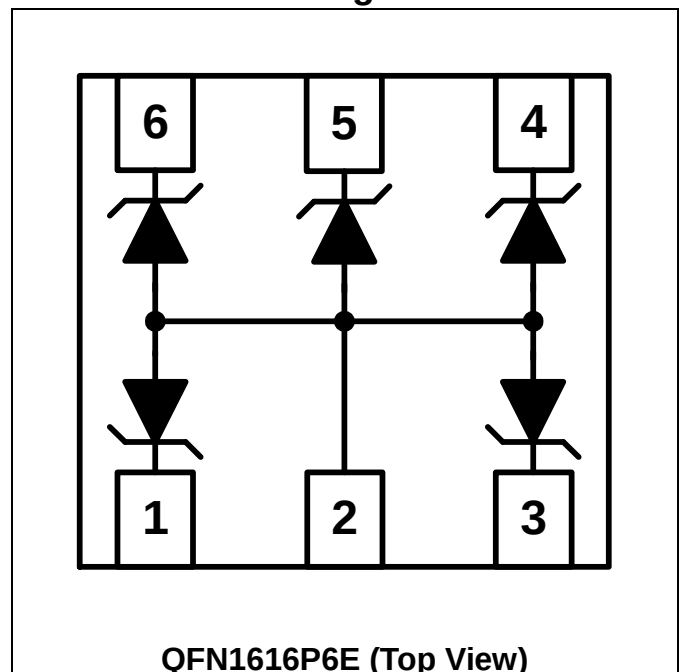
AZ2115-05F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4

($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram



Pin Configuration



QFN1616P6E (Top View)

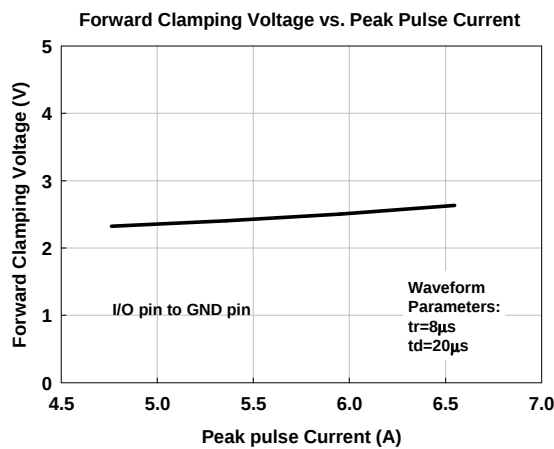
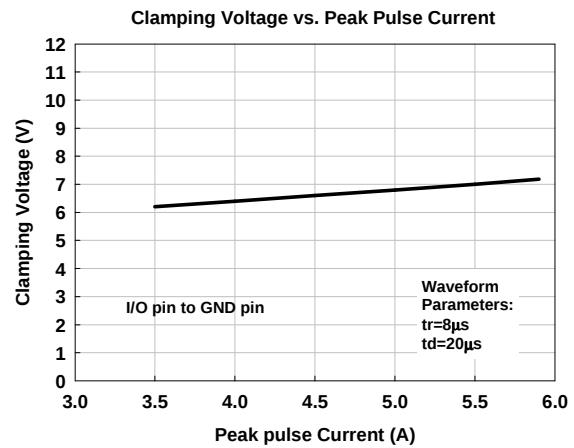
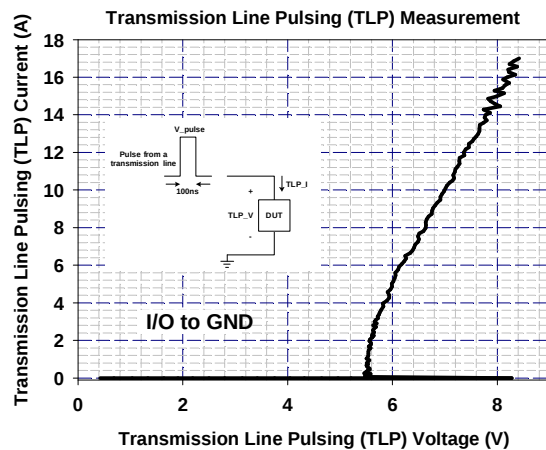
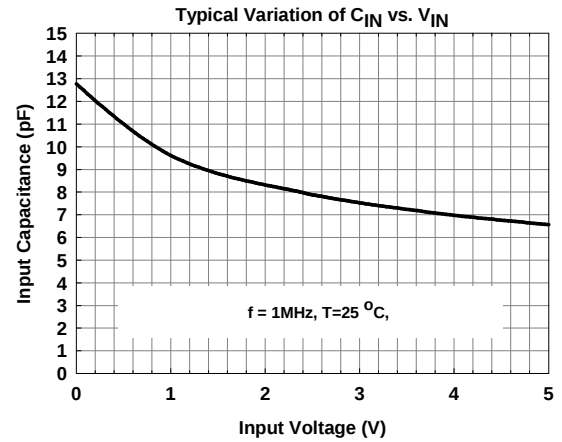
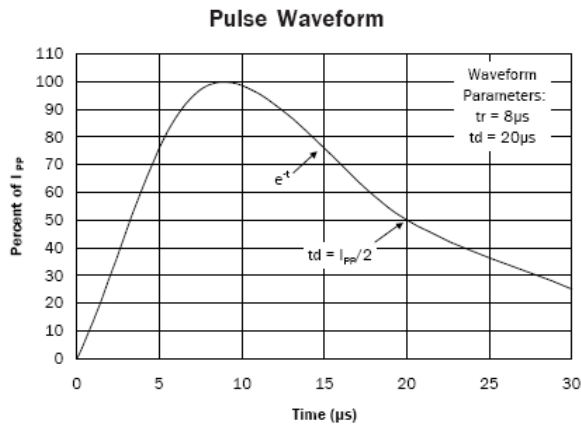
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20us)	I _{PP}	6 (pin-1, 3,4,6)	A
		3.5 (pin-5)	
Operating Supply Voltage (pin-1,-2 to pin-3)	V _{DC}	6	V
pin-1,-3, -4, -5, -6 to pin-2 ESD per IEC 61000-4-2 (Air)	V _{ESD-1}	16	kV
pin-1,-3, -4, -5, -6 to pin-2 ESD per IEC 61000-4-2 (Contact)		10	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	pin-1,-3, -4, -5, -6 to pin-2, T=25 °C.			5	V
Reverse Leakage Current	I _{Leak}	V _{RWM} = 5V, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2.			2.5	μA
Reverse Breakdown Voltage	V _{BV}	I _{EV} = 1mA, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2	6		9	V
Forward Voltage	V _F	I _F = 15mA, T=25 °C, pin-2 to pin-1,-3, -4, -5, -6	0.6	0.8	1	V
Surge Clamping Voltage	V _{CL-surge}	I _{PP} =5A, tp=8/20us, T=25 °C, pin-1, -3, -4, -6 to pin-2.		6.8		V
		I _{PP} =3.5A, tp=8/20us, T=25 °C, pin-5 to pin-2.		6.2		
ESD Clamping Voltage	V _{clamp}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, pin-1,-3, -4, -5, -6 to pin-2.		8.5		V
ESD Dynamic Turn-on Resistance	R _{dynamic}	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, pin-1,-3, -4, -5, -6 to pin-2.		0.2		Ω
Channel Input Capacitance	C _{IN}	V _R = 0V, f = 1MHz, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2.		13	15	pF



Typical Characteristics



Applications Information

The AZ2115-05F is designed to protect five lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ2115-05F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1, 3, 4, 5 and 6. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ2115-05F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2115-05F.
- Place the AZ2115-05F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

Fig. 2 shows an example of PCB layout with the AZ2115-05F.

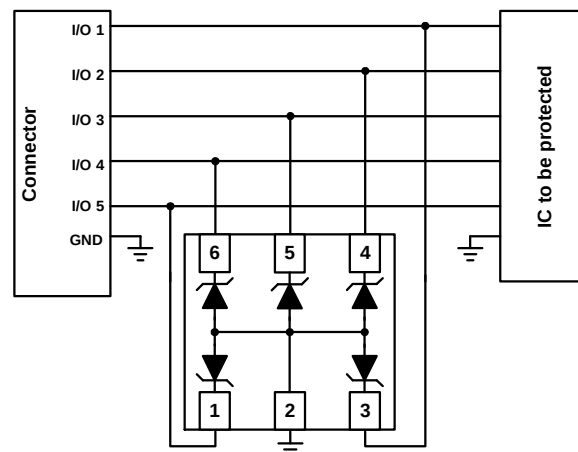


Fig. 1

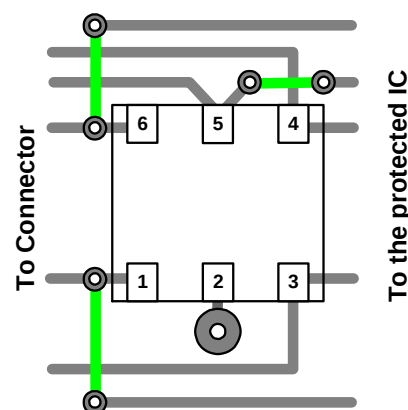


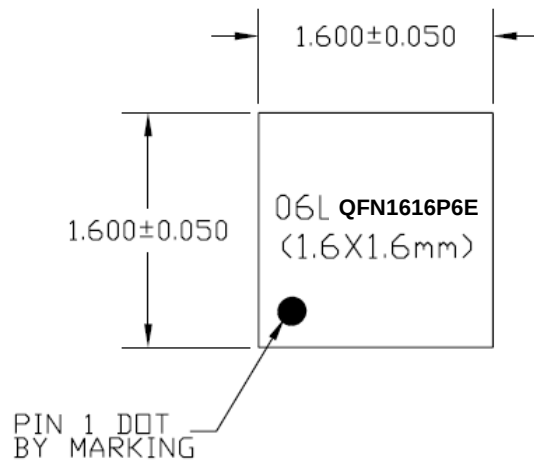
Fig. 2



Mechanical Details

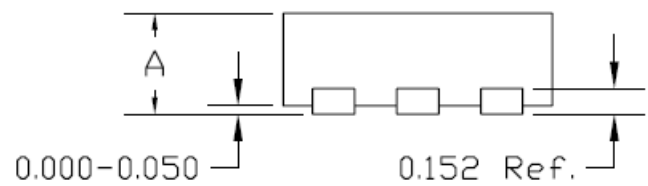
QFN1616P6E

PACKAGE DIAGRAMS and DIMENSIONS (unit : mm)

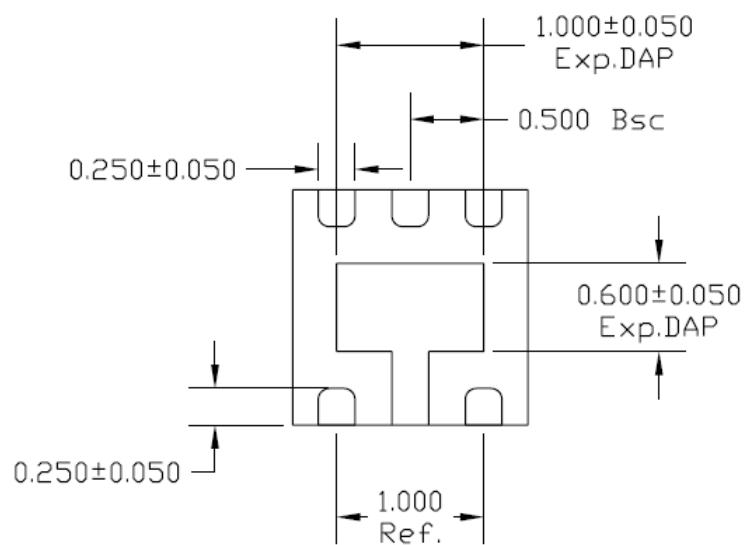


TOP VIEW

A	MAX.	0.600
	NOM.	0.550
	MIN.	0.500



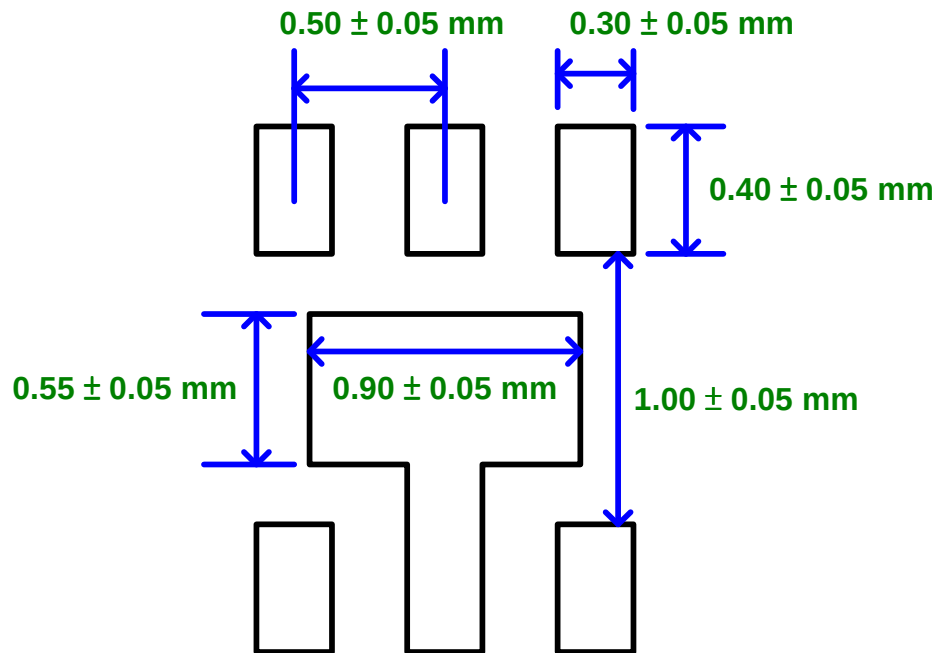
SIDE VIEW



BOTTOM VIEW



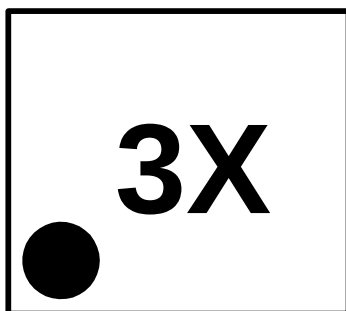
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



3 = Device Code
X = Date Code

Part Number	Marking Code
AZ2115-05F (Rohs part)	3X
AZ2115-05F (Green part)	5X

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ2115-05F.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton



Revision History

Revision	Modification Description
Revision 2008/03/28	Original Release.
Revision 2008/10/14	Add marking code for the Green part.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.