

Features

- ESD/Surge Protection for 1 Line with Bi-directional
- Provide ESD protection for each line to
IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air / contact)
IEC 61000-4-4 (EFT) 80A (5/50ns)
IEC 61000-4-5 (Lightning) 100A (8/20 μs)
- For operating voltage of 5.0V and below
- **1.6mm x 1.0mm DFN package** saves board space
- High surge protection
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Vbat Pin for Mobile Device
- Power Line Protection
- Audio Protection
- Mobile Phones
- Hand Held Portable Applications

Description

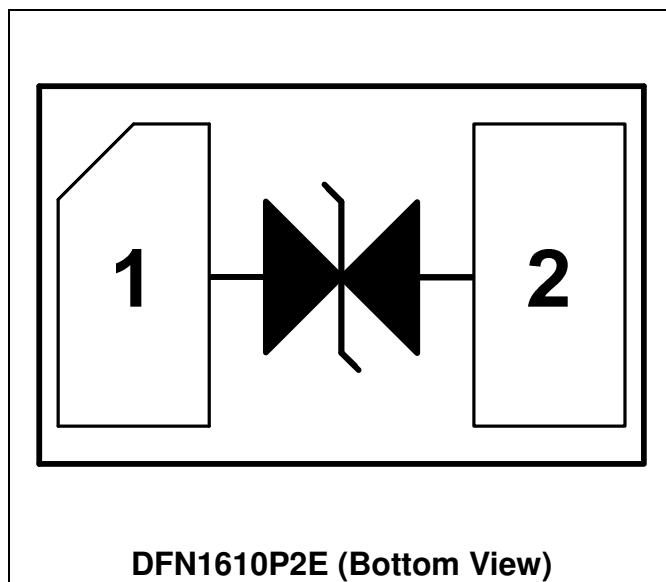
AZ3205-01F is a design which includes a bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic system. The AZ3205-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ3205-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ3205-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ3205-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current	I_{PP-1} (Note 1)	100	A
	I_{PP-2} (Note 2)	80	
Operating Supply Voltage	V_{DC}	± 5.5	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 30	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 30	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +85	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	$T=25^{\circ}C$.	-5.0		5.0	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = \pm 5.0V$, $T=25^{\circ}C$.			1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, $T=25^{\circ}C$.	6.0		9.0	V
Surge Clamping Voltage (Note 1)	V_{CL}	$I_{PP} = 50A$, $t_p=8/20\mu s$, $T=25^{\circ}C$.		8		V
		$I_{PP} = 100A$, $t_p=8/20\mu s$, $T=25^{\circ}C$.		11.5		
ESD Clamping Voltage (Note 3)	V_{clamp}	IEC 61000-4-2 +8kV ($I_{TLP} = 16A$), Contact mode, $T = 25^{\circ}C$.		6.0		V
Channel Input Capacitance	C_{IN}	$V_R = 0V$, $f = 1MHz$, $T=25^{\circ}C$.		140	200	pF

Note 1: The Peak Pulse Current measured conditions: $t_p = 8/20\mu s$, 2Ω source impedance.

Note 2: The Peak Pulse Current measured conditions: $t_p = 8/20\mu s$, 42Ω source impedance.

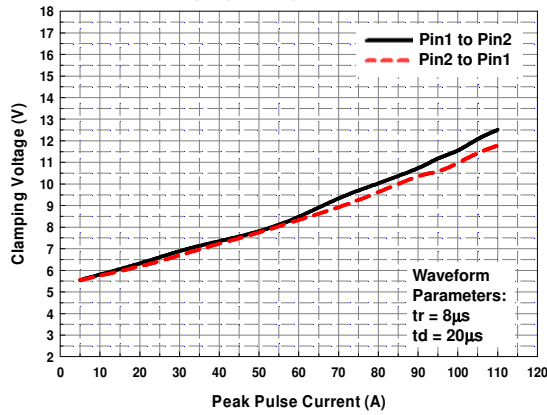
Note 3: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 1ns$.

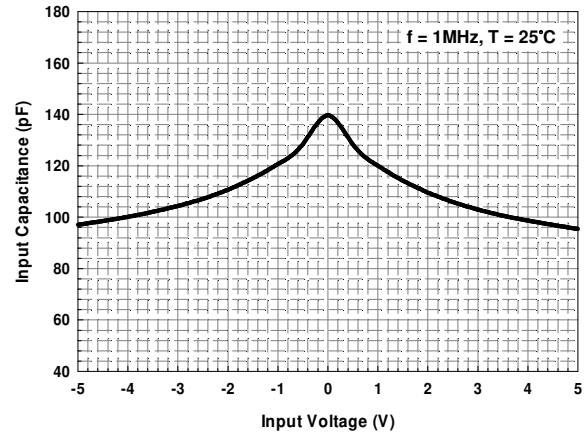


Typical Characteristics

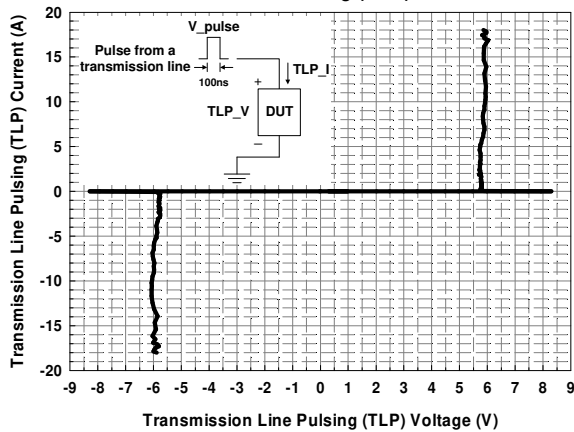
Reverse Clamping Voltage vs. Peak Pulse Current



Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement





Applications Information

The AZ3205-01F is designed to protect one line against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ3205-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ3205-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3205-01F.
- Place the AZ3205-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

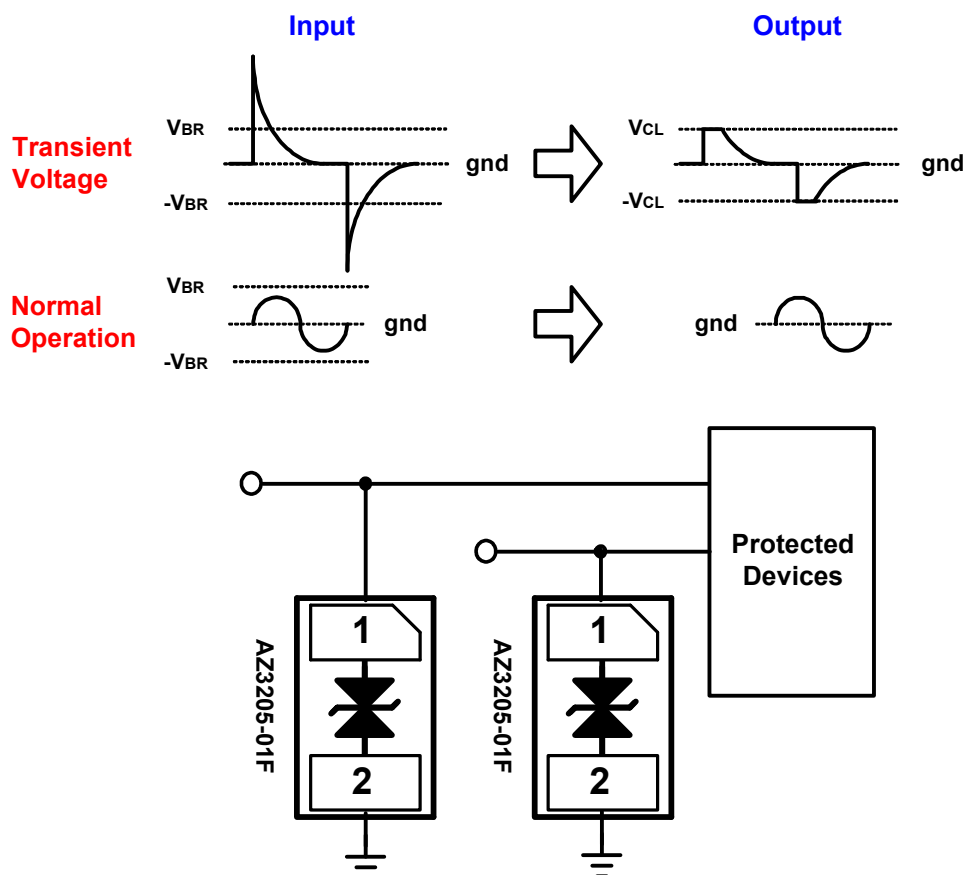
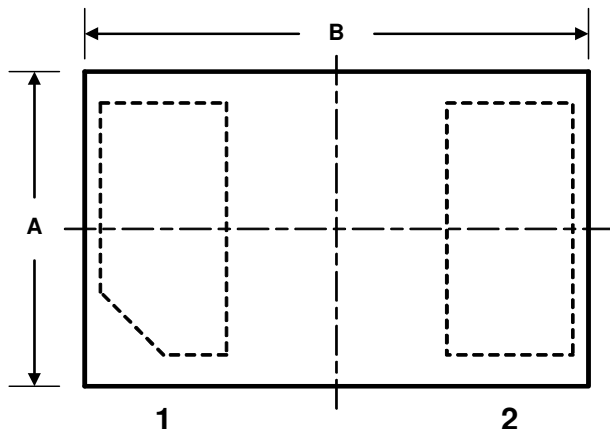


Fig. 1 ESD protection scheme by using AZ3205-01F.

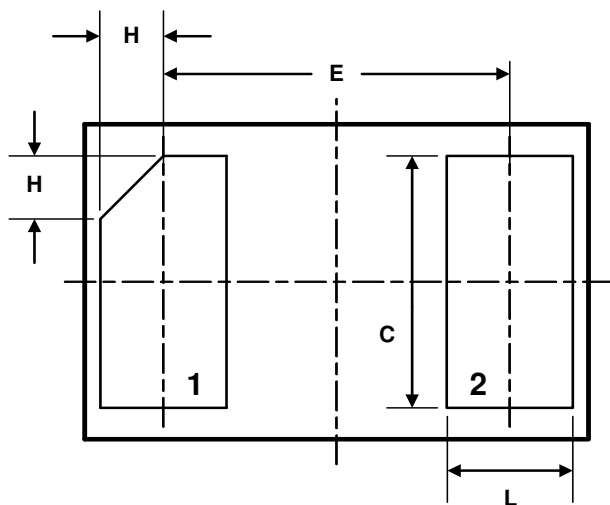


Mechanical Details

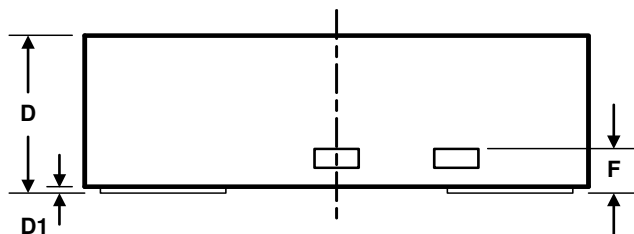
DFN1610P2E PACKAGE DIAGRAMS



Top View



Bottom View

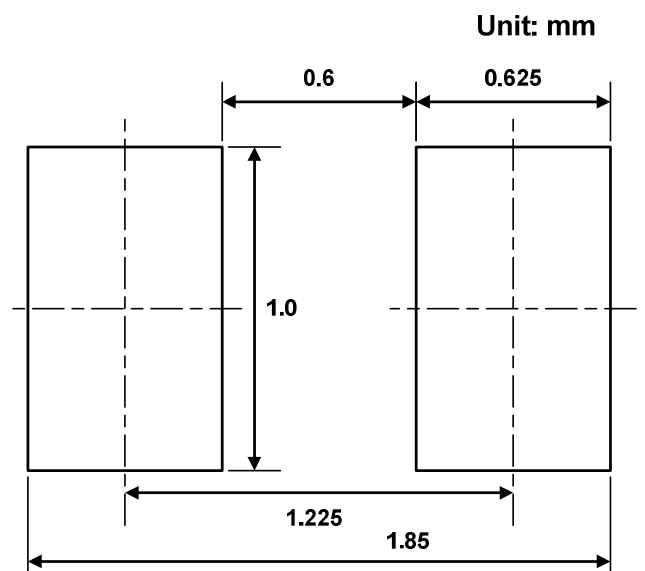


Side View

PACKAGE DIMENSIONS

SYMBOL	Millimeter		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
B	1.55	1.60	1.65
C	0.75	0.80	0.85
D	0.45	0.50	0.55
D1	-	0.02	0.05
E	1.10BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

LAND LAYOUT

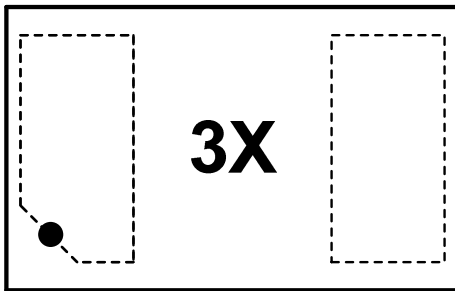


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



MARKING CODE



Top View

3 = Device Code

X = Date Code

Part Number	Marking Code
AZ3205-01F.R7G (Green Part)	3X

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3205-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2016/03/15	Preliminary Release.
Revision 2017/05/16	Formal Release.