Features

- ESD Protect for 2 Lines with Bi-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±15kV (air), ±15kV (contact)
  IEC 61000-4-4 (EFT) 50A (5/50ns)
  Cable Discharge Event (CDE)
- Ultra-small DFN1006P3X package (1.0mmx0.6mmx0.45mm) saves board space
- Protect two I/O lines or two power lines
- Fast turn-on and Low clamping voltage
- Low operating voltage: 5V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***

Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

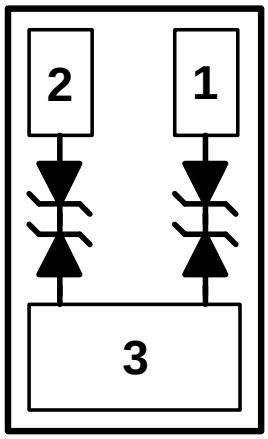
AZ5125-02F is a design which includes two bi-directional ESD rated clamping cells to protect two power lines, or two control lines, or two low speed data lines in an electronic systems. The AZ5125-02F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ5125-02F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control/data lines, protecting any downstream components.

AZ5125-02F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ5125-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



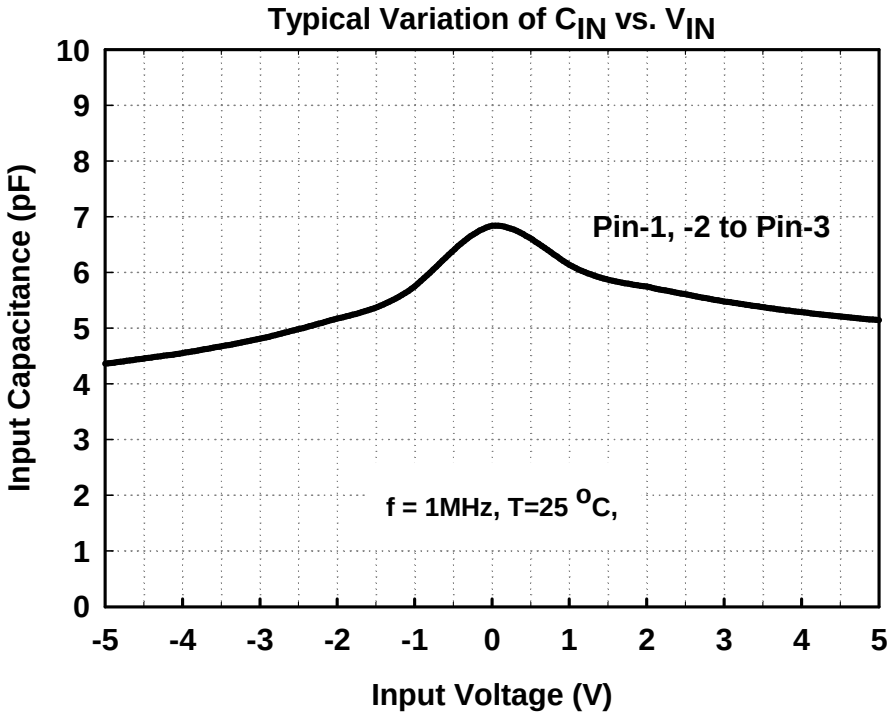
DFN1006P3X (Bottom View)
(1.0mm x 0.6mm x 0.45mm)

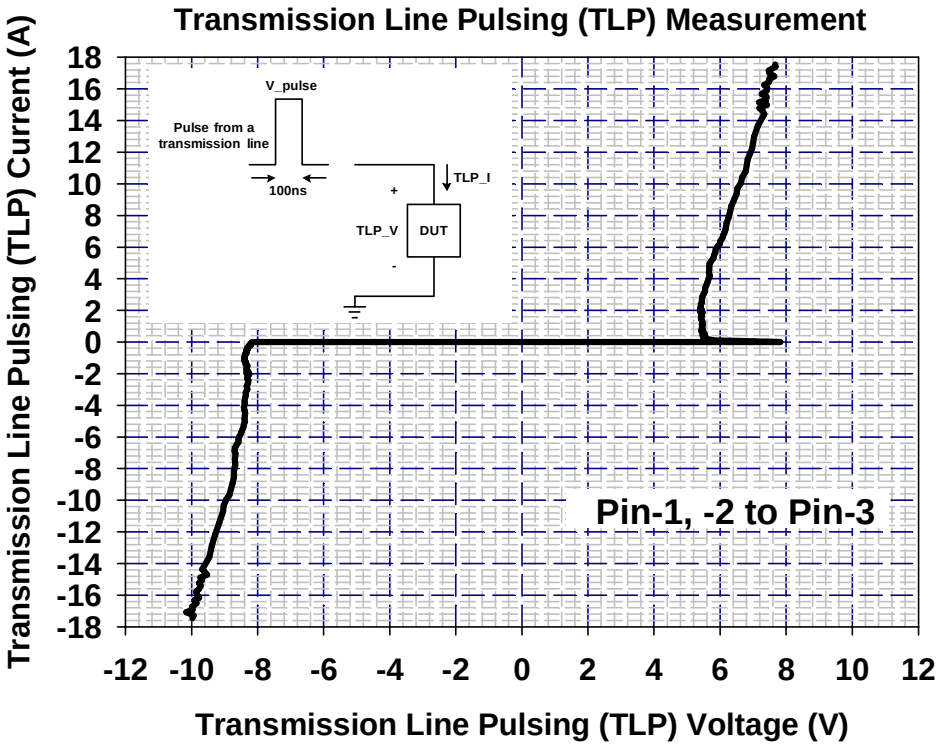
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Operating Supply Voltage (pin-1,-2 to pin-3)	V_{DC}	±5.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±15	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C	-5		5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±5V, T=25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	5.7		9	V
ESD Clamping Voltage	V_{ESD_CL}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode		11		V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C.		7	8.5	pF

Typical Characteristics





Applications Information

The AZ5125-02F is designed to protect two lines against System ESD/EFT/Cable-Discharging pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5125-02F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin 2 respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5125-02F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5125-02F.
- Place the AZ5125-02F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

Fig. 2 shows an example of PCB layout for speaker.

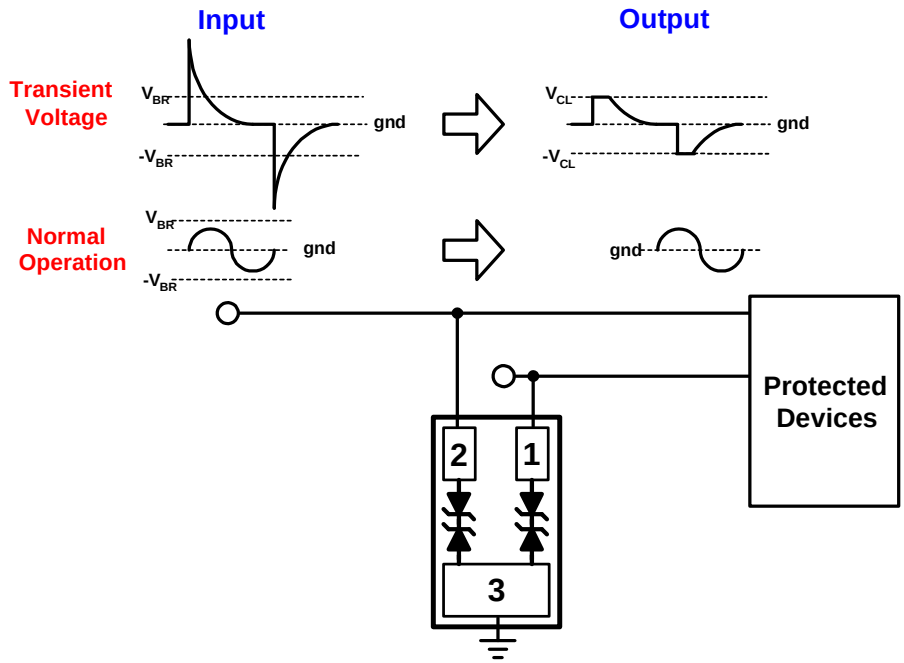


Fig. 1

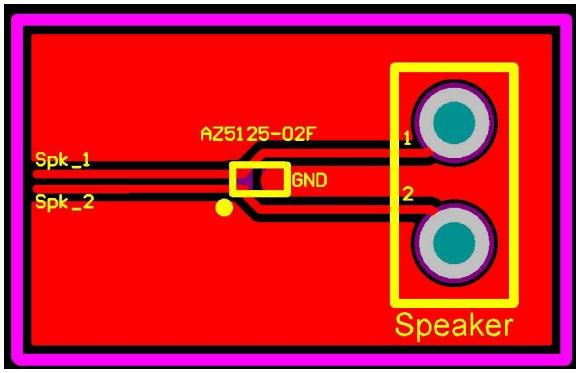
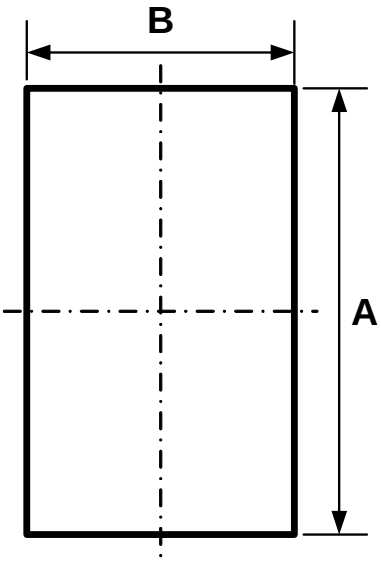


Fig. 2

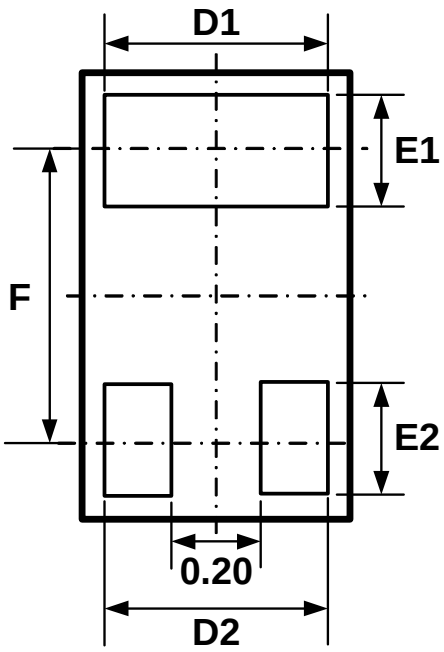
Mechanical Details

DFN1006P3X

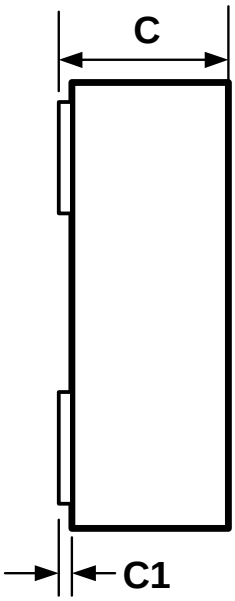
PACKAGE DIAGRAMS AND DIMENSIONS



TOP VIEW



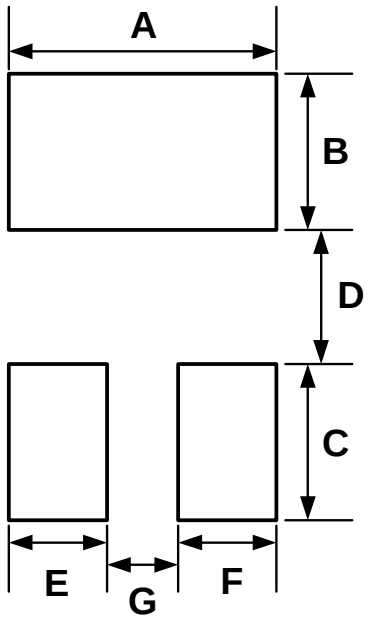
BOTTOM VIEW (unit in mm)



SIDE VIEW

SYMBOL	Millimeters		
	MIN.	NOM.	MAX.
A	0.95	1.00	1.05
B	0.55	0.60	0.65
C	0.41	0.45	0.50
C1	0.00	0.02	0.05
D1	0.45	0.50	0.55
D2	0.45	0.50	0.55
E1	0.20	0.25	0.30
E2	0.20	0.25	0.30
F	0.65		

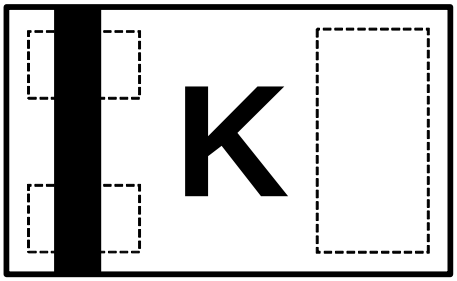
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.600	0.024
B	0.350	0.014
C	0.350	0.014
D	0.300	0.012
E	0.225	0.009
F	0.225	0.009
G	0.150	0.006

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

Part Number	Marking Code
AZ5125-02F	K

Revision History

Revision	Modification Description
Revision 2012/07/18	Preliminary Release.
Revision 2012/08/31	Formal Release.
Revision 2012/09/19	Add an example of PCB layout.