Features

- ESD/Surge Protection for 1 Line with Unidirectional.
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-5 (Lightning) 60A (8/20μs)
- For operating voltage of 5.0V and below
- 1.6mm x 1.0mm DFN package saves board space
- High surge protection
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***
- ***AEC-Q101 qualified***

Applications

- **Power Line Protection**
- **Power Management Systems**
- **Hand Held Portable Applications**
- **Mobile Device Applications**
- **Control Signal Lines Protection**
- **Battery Protection**
- **Latchup Protection**

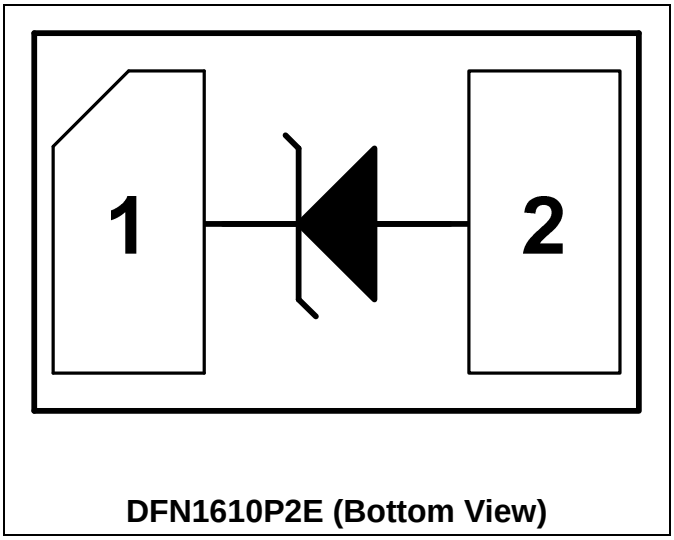
Description

AZ9315-01F is a design which includes a unidirectional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ9315-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ9315-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ9315-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1610P2E (Bottom View)

SPECIFICATIONS

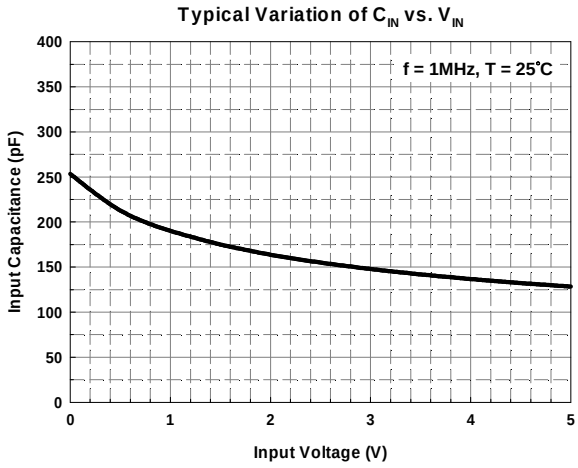
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp=8/20μs)	I_{PP}	60	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	5.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

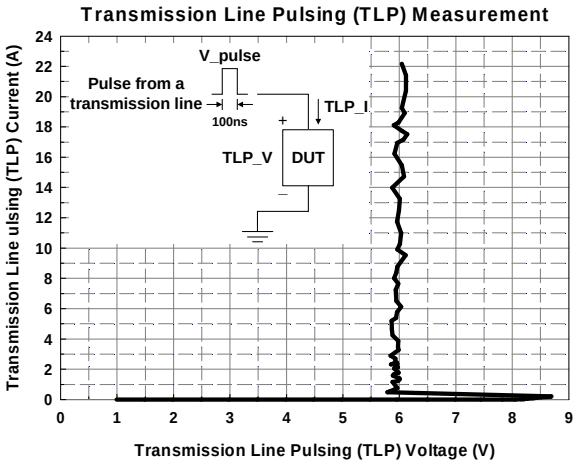
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T=25 °C.			5.0	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5.0V, T=25 °C, pin-1 to pin-2.			2.0	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1 to pin-2.	6.0		9.0	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-2 to pin-1.	0.4		1	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}= 40A, tp=8/20μs, T=25 °C, pin-1 to pin-2.		7.5		V
		I_{PP}= 60A, tp=8/20μs, T=25 °C, pin-1 to pin-2.		9.5		
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T=25 °C, pin-1 to pin-2.		6.0		V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C, pin-1 to pin-2.		250	300	pF

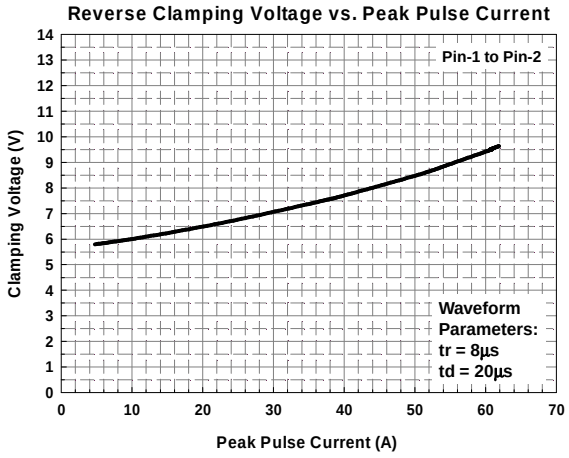
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

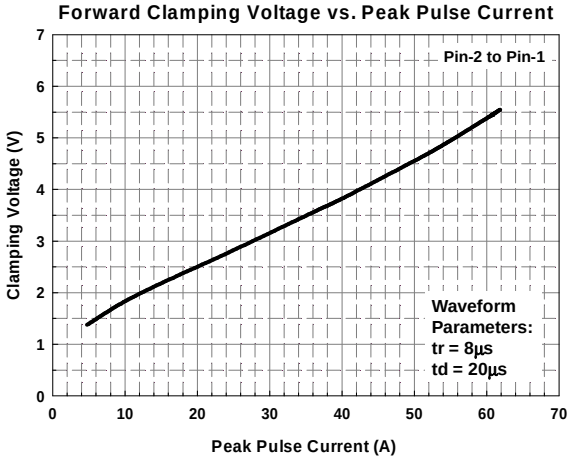
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics









Applications Information

The AZ9315-01F is designed to protect one line against System ESD/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ9315-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ9315-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9315-01F.
- Place the AZ9315-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to PCB internal circuit.

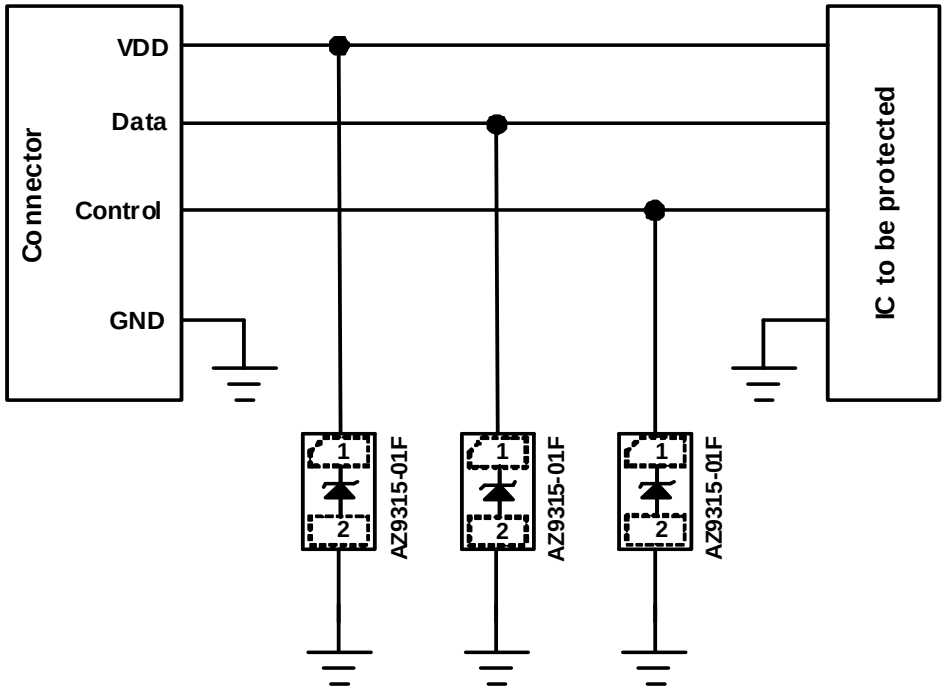
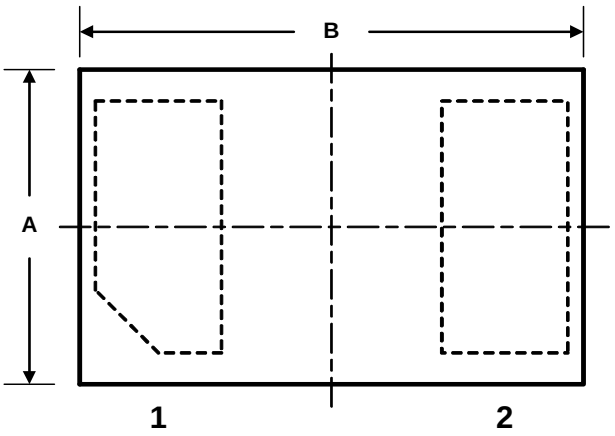


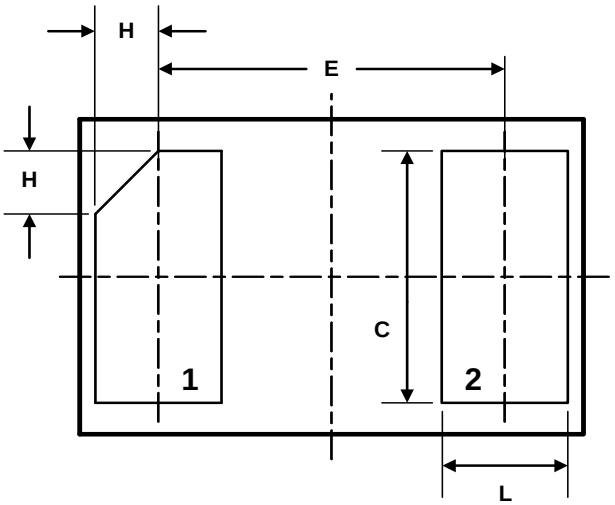
Fig. 1 ESD protection scheme by using AZ9315-01F.

Mechanical Details

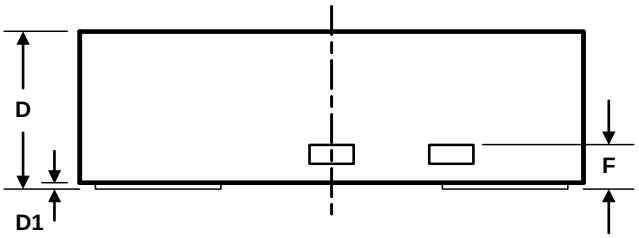
DFN1610P2E
PACKAGE DIAGRAMS



Top View



Bottom View



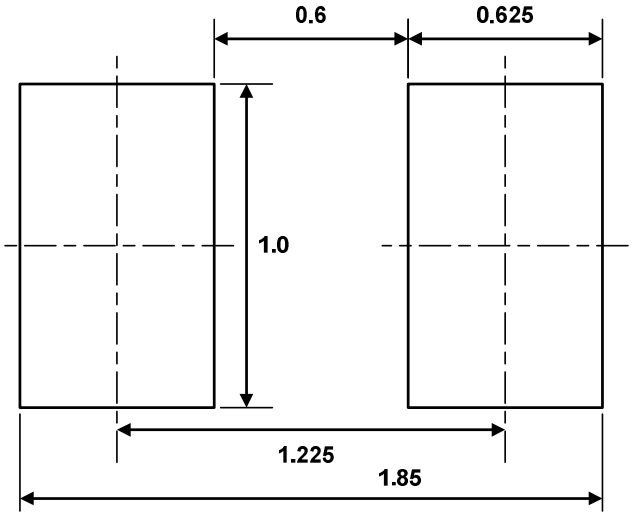
Side View

PACKAGE DIMENSIONS

SYMBOL	Millimeter		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
B	1.55	1.60	1.65
C	0.75	0.80	0.85
D	0.45	0.50	0.55
D1	-	0.02	0.05
E	1.10BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

LAND LAYOUT

Unit: mm



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.