

## Features

- ESD Protect for 1 Line with Bi-directional
- Provide ESD protection for a line to **IEC 61000-4-2 (ESD) ±16kV (air/contact) Cable Discharge Event (CDE)**
- Suitable for, **12V and below**, operating voltage applications
- 0402 small DFN package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**
- **AEC-Q101 qualified**

## Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players
- Peripherals

## Description

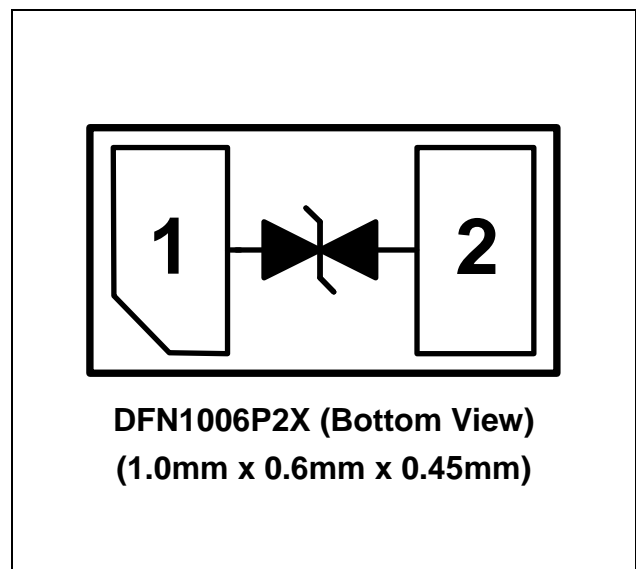
AZ9812-01F is a design which includes a unidirectional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ9812-01F has been specifically designed to protect sensitive components which are

connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), and Cable Discharge Event (CDE).

AZ9812-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ9812-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration



**DFN1006P2X (Bottom View)**  
**(1.0mm x 0.6mm x 0.45mm)**

## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Operating Supply Voltage	$V_{DC}$	$\pm 13.2$	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	$\pm 16$	kV
ESD per IEC 61000-4-2 (Contact)		$\pm 16$	kV
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	$^{\circ}C$
Operating Temperature	$T_{OP}$	-55 to +125	$^{\circ}C$
Storage Temperature	$T_{STO}$	-55 to +150	$^{\circ}C$

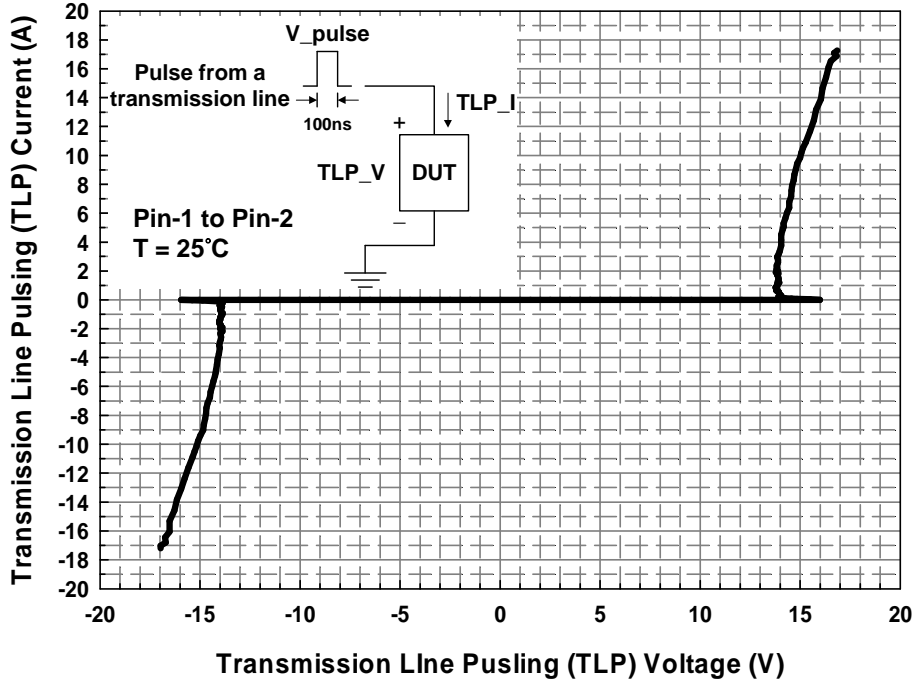
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	$V_{RWM}$	$T=25^{\circ}C$ .	-12		12	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = \pm 12V, T=25^{\circ}C$			1	$\mu A$
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1mA, T=25^{\circ}C$	13.5		16	V
ESD Clamping Voltage (Note 1)	$V_{clamp}$	IEC 61000-4-2 +8kV ( $I_{TLP} = 16A$ ), Contact mode, $T=25^{\circ}C$ , pin-1 to pin-2.		17		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, $T= 25^{\circ}C$ , Contact mode, pin-1 to pin-2.		0.25		$\Omega$
Channel Input Capacitance	$C_{IN}$	$V_R = 0V, f = 1MHz, T=25^{\circ}C$ , pin-1 to pin-2.		3.5	5.0	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

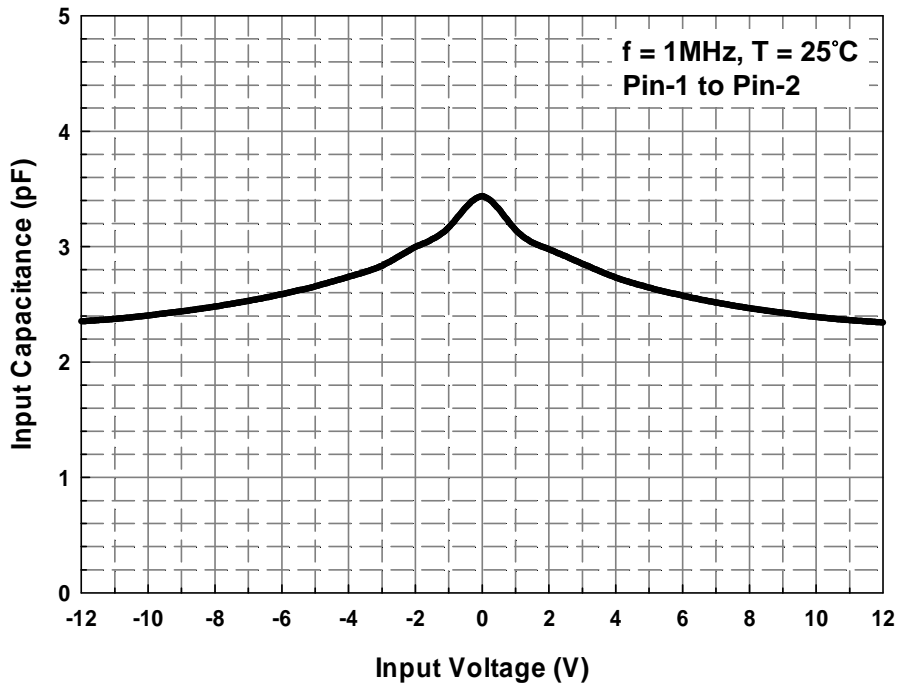
TLP conditions:  $Z_0 = 50\Omega$ ,  $t_p = 100ns$ ,  $t_r = 2ns$ .

## Typical Characteristics

**Transmission Line Pulsing (TLP) Measurement**



**Typical Variation of  $C_{IN}$  vs.  $V_{IN}$**



## Applications Information

The AZ9812-01F is designed to protect one line against System ESD/CDE pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9812-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9812-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9812-01F.
- Place the AZ9812-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

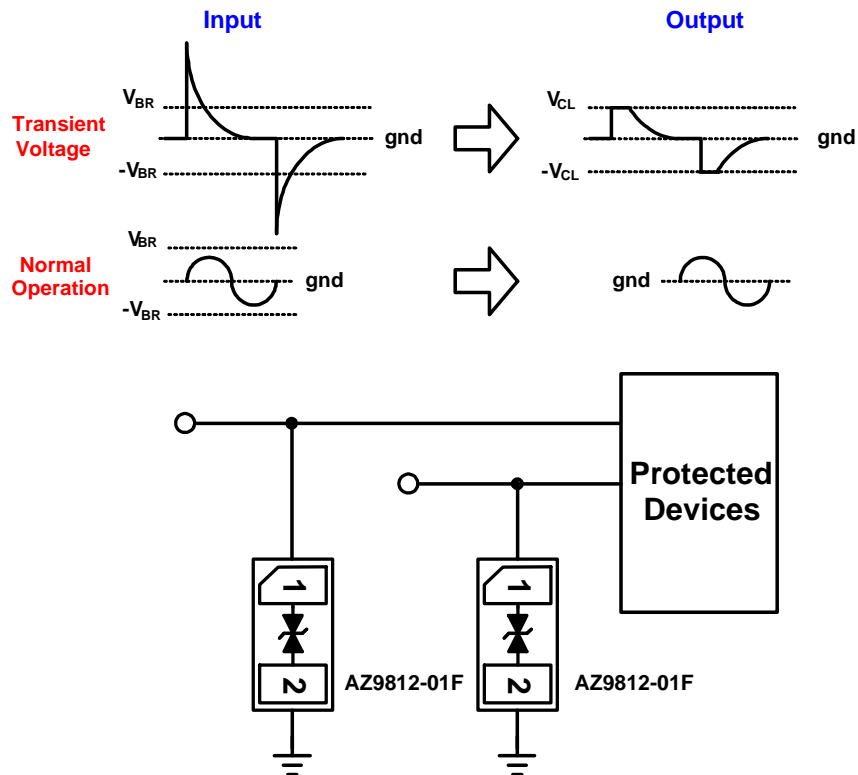
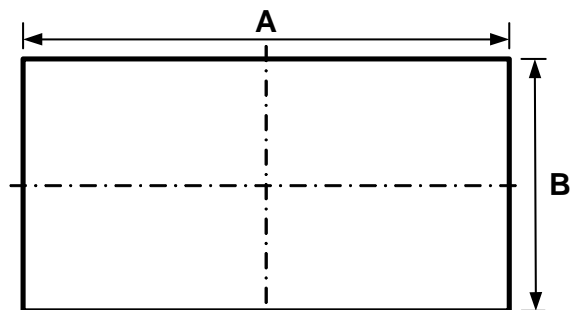


Fig. 1 ESD protection scheme by using AZ9812-01F.

**Mechanical Details**

DFN1006P2X

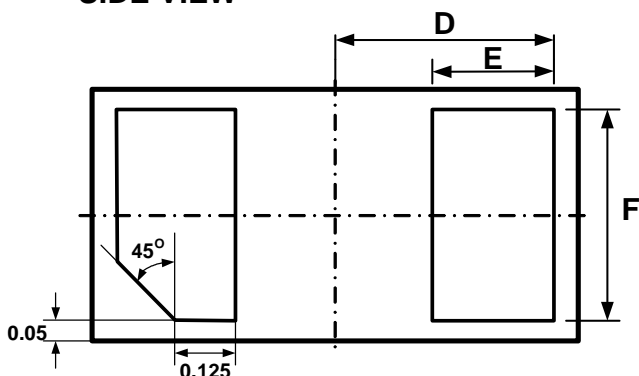
**PACKAGE DIAGRAMS**



TOP VIEW

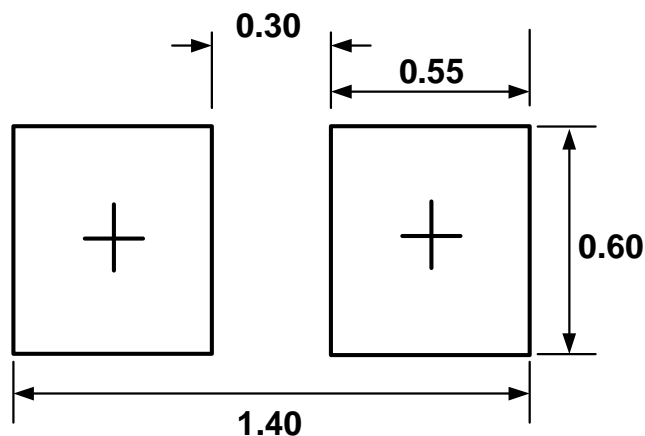


SIDE VIEW



BOTTOM VIEW

**LAND LAYOUT**



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

**PACKAGE DIMENSIONS**

Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.41	0.55	0.016	0.022
D	0.45		0.018	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022