



Features

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant for 2 Mbps and 5 Mbps CAN FD with wake-up pattern wake-up
- Fault voltage up to ± 70 V for bus pins
- Integrated ESD and Surge Transient Voltage Suppressor (TVS) for bus pins
- TVS protection Immunities for bus terminals:
 ±12 kV IEC 61000-4-2, Contact Discharge
 ±16 kV IEC 61000-4-2, Air Discharge
 ±100 V IEC 61000-4-5, Surge (8/20 μ s, 2 Ω)
- HBM ±5 kV ESD protection for all pins
- HBM ±8 kV ESD protection for bus pins
- MM ±400 V ESD protection for all pins
- High CDM protection up to ±800 V for all pins
- Latch up immunity up to ±400 mA for all pins
- High IEC 61000-4-4 Electrical Fast Transient (EFT) coupling immunity for bus pins under communication
- Capability for both low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Low standby current (12 μ A, typical) for power saving
- V_{IO} input allows for direct interfacing with 1.8 V to 5 V microcontrollers
- Ideal passive behavior to CAN bus with supply power off
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on the pins of V_{CC} and V_{IO} power
- Current-limitation and thermal shutdown for the driver design

Applications

- Industrial Control and Instrumentation Networks
- Motor Control
- Building Automation
- Security Systems
- Medical Equipments
- Battery Control

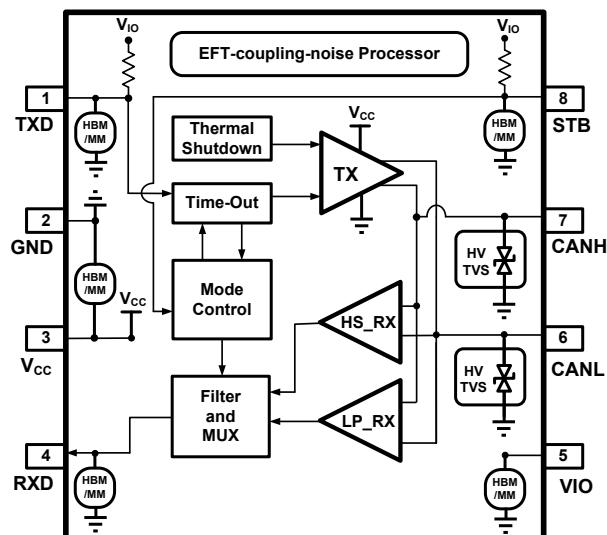
Description

AZKN6129P is a ±12 kV IEC 61000-4-2 protected Controller Area Network (CAN) transceiver IC. It serves as an interface between a CAN protocol controller (MCU) and the physical two-wire CAN bus. This device operates at 5 V power supply and is fully compliant with ISO 11898-2:2016 standard for CAN FD application. The data rate of both driver and receiver is up to 5 Mbps to support the high-speed application of the CAN FD.

AZKN6129P has the capabilities of both the ±40 V common mode range of the receiver and the low EME of the transmitter, which has been patented as the Amazing's intellectual property. Moreover, the whole-chip design of the AZKN6129P can sustain high EFT coupling under communication.

AZKN6129P is a robust CAN transceiver, which features ±70 V fault protection to sustain the DC short voltage on the bus pins. Moreover, AZKN6129P has ±100 V protection immunity to avoid the possible damage from the EOS events. In addition, the whole-chip ESD protection immunity of AZKN6129P can sustain HBM ±5 kV, MM ±400 V and CDM ±800 V, which is satisfied to overcome the ESD zapping under the worst manufacture environment.

Functional Block of AZKN6129P





Thermal Characteristics

PARAMETER	SYMBOL	Conditions	Value	UNIT
Thermal resistance from virtual junction to ambient	θ_{JA} ^[1]	$P_H = 70\text{mW}$ under the air flow rate = 0 (m/s) in the ambient temperature ^[2]	90.97	°C/W

[1] The thermal resistance between virtual junction and ambient is $\theta_{JA} = (T_J - T_{AMB})/P_H$, where T_J is the virtual junction temperature and T_{AMB} is the ambient temperature under the power dissipation of P_H .

[2] According to JEDEC JESD51-2 and JESD51-7 at natural convection on 2s2p board with two inner copper layers (Power/Ground thickness: 35 um; Signal thickness: 70 um).

Absolute Maximum Ratings ^[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC voltage on CANH, CANL	V_{CANH}, V_{CANL}	-70	70	V
DC voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-50	50	V
DC voltage on all other pins	V_X	-0.3	7	V
System-level ESD (IEC 61000-4-2, Unpowered Contact Discharge) -- at pins CANH, CANL	$V_{ESD(\text{contact})}$	-12	12	kV
System-level ESD (IEC 61000-4-2, Powered on Contact Discharge) -- at pins CANH, CANL	$V_{ESD(\text{contact})}$	-12	12	kV
System-level ESD (IEC 61000-4-2, Unpowered Air-Gap Discharge) -- at pins CANH, CANL	$V_{ESD(\text{air})}$	-16	16	kV
System-level ESD (IEC 61000-4-2, Powered on Air-Gap Discharge) -- at pins CANH, CANL	$V_{ESD(\text{air})}$	-16	16	kV
Surge (IEC 61000-4-5) at pins CANH, CANL ^[2]	V_{SURGE}	-100	100	V
HBM ESD (Human Body Model; 100 pF; 1.5 kΩ) -- at any pins ^[3]	V_{HBM}	-5	5	kV
HBM ESD (Human Body Model; 100pF; 1.5 kΩ) -- at pins CANH, CANL ^[3]	V_{HBM}	-8	8	kV
MM ESD (Machine Model; 200 pF) -- at any pins ^[4]	V_{MM}	-400	400	V
CDM ESD (Charged Device Model; field induced charge) -- at any pins ^[5]	V_{CDM}	-800	800	V
Virtual junction temperature	T_J	-40	150	°C
Storage temperature	T_{STO}	-55	150	°C

[1] Stresses listed above may cause permanent damage to the device under "Maximum Ratings". This is a stress rating only and functional operation of the device at those or other conditions above those indicated in the operational listings of this specification are not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Applied surge source voltage: $tp = 8/20 \mu\text{s}$, 2Ω source impedance.

[3] Verified by thirty-party referred to MIL-STD-883J Method 3015.9.

[4] Verified by thirty-party referred to JESEC EIA/JESD22-A115.

[5] Verified by thirty-party referred to JESD22-C101-D.



DC Electrical Characteristics

($V_{CC} = 4.75$ V to 5.25 V; $V_{IO} = 1.7$ V to 5.25 V; $T_{AMB} = -40$ °C to +125 °C; $R_L = 60 \Omega$ unless otherwise noted.
Typical values are at $V_{CC} = 5$ V; $V_{IO} = 3.3$ V and $T_{AMB} = 25$ °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Supply : V_{CC}						
Supply voltage	V_{CC}		4.75	-	5.25	V
Undervoltage detection voltage on pin V_{CC}	$V_{UVD(VCC)}$		3.5	4.0	4.5	V
Supply current	I_{CC}	Standby mode				
		$V_{TXD} = V_{IO}$	-	12	20	μA
		Normal mode				
		Recessive; $V_{TXD} = V_{IO}$	2.5	5	12	mA
		Dominant; $V_{TXD} = 0$ V	20	40	70	mA
		Dominant; $V_{TXD} = 0$ V; Short circuit on bus lines; $-3V < (V_{CANH} = V_{CANL}) < +18V$	2.5	90	120	mA
Internal Supply : V_{IO}						
Supply voltage on pin V_{IO}	V_{IO}		1.7	-	5.25	V
Undervoltage detection voltage on pin V_{IO}	$V_{UVD(VIO)}$		-	1.4	-	V
Supply current	I_{IO}	Standby mode				
		$V_{TXD} = V_{IO}$	-	0.07	1	μA
		Normal mode				
		Recessive; $V_{TXD} = V_{IO}$	-	20	80	μA
		Dominant; $V_{TXD} = 0$ V	-	120	350	μA
Bus lines : CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	Normal Mode; $V_{TXD} = 0$ V; $t < t_{IO(dom)TXD}$				
		pin CANH; $R_L = 50 \Omega$ to 65Ω	2.75	3.5	4.5	V
		pin CANL; $R_L = 50 \Omega$ to 65Ω	0.5	1.5	2.25	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym} = V_{CANH} + V_{CANL}$; ^[2] $f_{TXD} = 250$ KHz, 1 MHz and 2.5 MHz; ^[3] $C_{SPLIT} = 4.7$ nF	0.9 V_{CC}	-	1.1 V_{CC}	



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Bus differential output voltage	$V_{O(\text{dif})\text{bus}}$	Normal Mode; $V_{\text{TXD}} = 0 \text{ V}$; $t < t_{\text{lo}(\text{dom})\text{TXD}}$				
		$R_L = 50 \Omega \text{ to } 65 \Omega$	1.5	-	3	V
		$R_L = 45 \Omega \text{ to } 70 \Omega$	1.4	-	3.3	V
		$R_L = 2240 \Omega$	1.5	-	5	V
		recessive; no load				
		Normal mode; $V_{\text{TXD}} = V_{\text{IO}}$	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
Recessive output voltage	$V_{O(\text{rec})}$	Normal mode; $V_{\text{TXD}} = V_{\text{IO}}$; no load	2	0.5 V_{CC}	3	V
		Standby mode; no load	-0.1	-	+0.1	V
Receiver recessive voltage	$V_{\text{rec}(\text{RX})}$	$V_{\text{CM}(\text{CAN})} = -40 \text{ V to } +40 \text{ V}$ ^[1]				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V
Receiver dominant voltage	$V_{\text{dom}(\text{RX})}$	$V_{\text{CM}(\text{CAN})} = -40 \text{ V to } +40 \text{ V}$ ^[1]				
		Normal mode	0.9	-	9	V
		Standby mode	1.15	-	9	V
Differential receiver threshold voltage	$V_{\text{th}(\text{RX})\text{dif}}$	$V_{\text{CM}(\text{CAN})} = -40 \text{ V to } +40 \text{ V}$ ^[1]				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.78	1.15	V
Differential receiver hysteresis voltage	$V_{\text{hys}(\text{RX})\text{dif}}$	$V_{\text{CM}(\text{CAN})} = -40 \text{ V to } +40 \text{ V}$ ^[1]		120		mV
Dominant short-circuit output current	$I_{O(\text{SC})\text{dom}}$	Normal Mode; $V_{\text{TXD}} = 0 \text{ V}$; $t < t_{\text{lo}(\text{dom})\text{TXD}}$; $V_{\text{CC}} = 5 \text{ V}$				
		Pin CANH; $V_{\text{CANH}} = -15 \text{ V to } 40 \text{ V}$	-115	-80		mA
		Pin CANL; $V_{\text{CANL}} = -15 \text{ V to } 40 \text{ V}$		80	115	mA
Recessive short-circuit output current	$I_{O(\text{SC})\text{rec}}$	Normal mode; $V_{\text{TXD}} = V_{\text{IO}}$ $V_{\text{CANH}} = V_{\text{CANL}} = -27 \text{ V to } +32 \text{ V}$	-5	-	+5	mA
Leakage current	I_L	$V_{\text{CC}} = V_{\text{IO}} = 0 \text{ V}$ or $V_{\text{CC}} = V_{\text{IO}} = \text{shorted to ground via } 47 \text{ k}\Omega$; $V_{\text{CANH}} = V_{\text{CANL}} = 5 \text{ V}$	-5	-	+5	μA
Input resistance	R_i	$-2 \text{ V} \leq V_{\text{CANH}} \leq +7 \text{ V}$; $-2 \text{ V} \leq V_{\text{CANL}} \leq +7 \text{ V}$	9	15	28	$\text{k}\Omega$
Input resistance deviation	ΔR_i	$0 \text{ V} \leq V_{\text{CANH}} \leq +5 \text{ V}$; $0 \text{ V} \leq V_{\text{CANL}} \leq +5 \text{ V}$ ^[2]	-3	-	+3	%
Differential input resistance	$R_{i(\text{dif})}$	$-2 \text{ V} \leq V_{\text{CANH}} \leq +7 \text{ V}$; $-2 \text{ V} \leq V_{\text{CANL}} \leq +7 \text{ V}$	19	30	52	$\text{k}\Omega$
Common-mode input capacitance	$C_{i(\text{cm})}$		^[2]	-	20	pF



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Differential input capacitance	$C_{i(dif)}$	[2]	-	-	10	pF
Temperature Protection						
Shutdown temperature	$T_{J(sd)}$	[2]	-	190	-	°C
Standby mode control input : STB						
High-level input voltage	V_{IH}		$0.7V_{IO}$	-	$V_{IO} + 0.3$	V
Low-level input voltage	V_{IL}		$-0.3V_{IO}$	-	$+0.3V_{IO}$	V
High-level input current	I_{IH}	$V_{STB} = V_{IO}$	-1	-	+1	μA
Low-level input current	I_{IL}	$V_{STB} = 0 \text{ V}$	-15	-4	-0.7	μA
Transmit data input : TXD						
High-level input voltage	V_{IH}		$0.7V_{IO}$	-	$V_{IO} + 0.3$	V
Low-level input voltage	V_{IL}		$-0.3V_{IO}$	-	$+0.3V_{IO}$	V
High-level input current	I_{IH}	$V_{TXD} = V_{IO}$	-5	-	+5	μA
Low-level input current	I_{IL}	$V_{TXD} = 0 \text{ V}$	-300	-90	-10	μA
Input capacitance	C_i	[2]	-	5	10	pF
Receive data output : RXD						
High-level output current	I_{OH}	$V_{RXD} = V_{IO} - 0.4 \text{ V}$	-11	-4.5	-1	mA
Low-level output current	I_{OL}	$V_{RXD} = 0.4 \text{ V}; \text{bus dominant}$	0.7	6.5	15	mA

[1] $V_{CM(CAN)}$ is the common mode voltage of CANH and CANL.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in [Figure 8](#).

Switching Characteristics

($V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $V_{IO} = 1.7 \text{ V to } 5.25 \text{ V}$; $T_{AMB} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$; $R_L = 60 \Omega$ unless otherwise noted.
Typical values are at $V_{CC} = 5 \text{ V}$; $V_{IO} = 3.3 \text{ V}$ and $T_{AMB} = 25 \text{ }^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 1 and Figure 6						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	40	-	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	55	-	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	65	-	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	85	-	ns
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	50	-	230	ns
Bit time on Bus	$t_{bit(Bus)}$	$t_{bit(TXD)} = 500\text{ns}$ [1]	435	-	530	ns
		$t_{bit(TXD)} = 200\text{ns}$ [1]	155	-	210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)} = 500\text{ns}$ [1]	400	-	550	ns
		$t_{bit(TXD)} = 200\text{ns}$ [1]	120	-	220	ns
Receiver timing symmetry	Δt_{Rec}	$\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(Bus)}$				
		$t_{bit(TXD)} = 500\text{ns}$	-65	-	+40	ns
		$t_{bit(TXD)} = 200\text{ns}$	-45	-	+15	ns



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
TXD dominant time-out time	$t_{to(dom)TXD}$	$V_{TXD} = 0 \text{ V}$; Normal mode	0.8	3	8	ms
Bus dominant wake-up time	$t_{wake(busdom)}$	Standby mode [2]	0.5	1.15	1.8	μs
Bus recessive wake-up time	$t_{wake(busrec)}$	Standby mode [2]	0.5	1.15	1.8	μs
Bus wake-up time-out time	$t_{to(wake)bus}$	Standby mode [2]	0.8	3.5	8	ms
Bus wake-up filter time	$t_{filtr(wake)bus}$	Standby mode [2]	0.5	1.15	1.8	μs
Standby to normal mode delay time	$t_{d(stb-norm)}$	[3]	20	34	55	μs

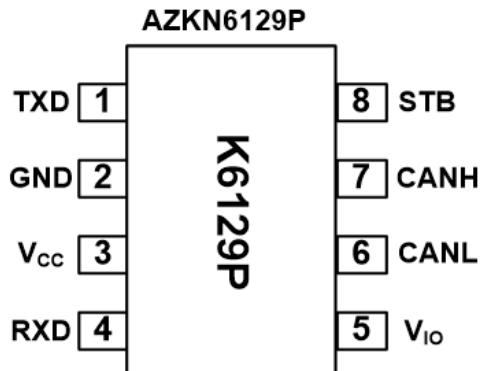
[1] See [Figure 2](#).

[2] See [Figure 3](#).

[3] See [Figure 4](#).



Pin Configuration



AZKN6129P : SOP8

Pin Function Description

Pin Number	Mnemonic	Function
1	TXD	Transmit data input
2	GND	Ground supply
3	V _{cc}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	V _{io}	Supply voltage for I/O level adapter.
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	Standby mode control input



Detail Description of Part

AZKN6129P is a high-speed CAN transceiver compliant with the ISO 11898-2:2016. The V_{IO} supply pin should be connected to supply voltage of microcontroller (see [Figure 5](#)). The V_{IO} allows the supply range from 1.7 V to 5.25 V of the microcontroller to adjust the I/O signal levels of the TXD, RXD, and STB pins.

Operation Modes

The normal and standby are two operating modes for AZKN6129P, which are selected by STB pin. The detail description of the operating modes related to both bus pins and RXD pin is listed in the [Table 1](#).

● Normal mode

When STB pin ties to logic LOW, AZKN6129P will switch to the normal mode. In the normal mode, the driver will translate the logic state of TXD to differential output of HS CAN. The data rate of driver is up to the 5 Mbps with both the controlled slew rate and common mode voltage, which is Amazing's property. So that the driver performs the low common mode noise and has the low EME performance, which is evaluated by IEC 61967-4.

The normal receiver with the ±40 V common mode range operates in the normal mode, which is also Amazing's property. The normal receiver translates the differential signal of HS CAN to the digital output of RXD with data rate up to 5 Mbps. The EM Immunity of normal receiver is evaluated by IEC 62132-4.

The loop delay symmetry from TXD to RXD is optimized by both driver and normal receiver in AZKN6129P.

● Standby mode

When the STB ties to logic HIGH, AZKN6129P will switch to the standby mode. In the standby mode, both the driver and normal receiver are turned off so that the bus pins are biased to GND to save V_{CC} power. Only the low power receiver operates to monitor the activity of the bus so as to inform the microcontroller if go to the normal mode or not.

In standby mode, the wake-up filter on the output of the low-power receiver ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD after

a wake-up pattern has been detected. Therefore, the data on RXD is not exact but is a wake-up signal to microcontroller.

The bus pins of AZKN6129P bias to GND via input resistor so that it is passive behavior in the standby mode.

● Remote wake-up via the CAN bus

For avoiding spurious wake-up event, AZKN6129P could be awake from standby mode only when a wake-up pattern defined by ISO 11898-2:2016 is detected on bus.

This dedicated wake-up pattern consists of three states.

- a dominant state $> t_{wake(busdom)}$ followed by
- a recessive state $> t_{wake(busrec)}$ followed by
- a dominant state $> t_{wake(busdom)}$

Before a complete wake-up pattern is detected, dominant and recessive bits which are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively will be ignored and pin RXD will be kept logic high.

This dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ (see [Figure 3](#)). Otherwise, the internal wake-up logic will be reset. Therefore, the complete wake-up pattern must be resent again to trigger a valid wake-up event.

After a complete wake-up pattern is detected, bus dominant or bus recessive states that persist longer than $t_{fltr(wake)bus}$ will be reflected on pin RXD. AZKN6129P will remain in standby mode until microcontroller ties STB pin to logic LOW.

Fail-safe Protection

● TXD dominant time-out function

The function of "TXD dominant time-out" prevents the failure of the hardware or software from keeping the bus in the dominant state. The failure causes the bus to be blocked all communication. The timer of "TXD dominant time-out" is started when TXD pin is set to LOW. If the time of TXD pin in the LOW state is longer than $t_{to(dom)TXD}$, the driver will be turn off to release the bus. The timer of "TXD dominant time-out" will be reset when TXD pin is set to HIGH. Therefore, the minimum data rate of 25 kbps is defined by the function of "TXD dominant time-out".



- **Pull-up of TXD and STB input pins**

The pins of both TXD and STB with internal pull-ups to V_{IO} are safe-guarantee design due to one or both of these pins in floating condition. When TXD pin is internally pulled up, the transmitter is forced into the recessive state. When STB pin is internally pulled up, AZKN6129P is forced into the low power standby mode. By the way, the pull-up currents will be generated if the pins are biased to low state. In standby mode, both pins should be held HIGH to reduce the current.

- **Undervoltage detection on pins V_{CC} and V_{IO}**

When V_{CC} drops below the V_{CC} undervoltage detection level $V_{UVD(VCC)}$ or V_{IO} drops below the V_{IO} undervoltage detection level $V_{UVD(VIO)}$, the transceiver will switch to off mode. The logic state of STB and TXD pins will be ignored and the transceiver will switch off and disengage from the bus (zero load) until V_{CC} and V_{IO} have been recovered. The undervoltage detection is the protection function to avoid the abnormal operation of V_{CC} and V_{IO} power.

- **Overtemperature protection**

When the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, the output of the drivers will be disabled to protect AZKN6129P from burn out issue. In this state, both CANH and CANL are biased to the recessive level no matter what the logic level of TXD pin is and the receiver still remains operational. When the temperature falls below $T_{J(SD)}$, the overtemperature protection will be released. The typical $T_{J(SD)}$ is designed as 190 °C under $V_{CC} = 5.0$ V.

High-Immunity Communication

- **High EFT coupling Immunity**

AZKN6129P has high EFT coupling immunity on the bus line under the normal operation. The output of transmitter (CANH and CANL) and the output of receiver (RXD) could be recovered after next bit when the high voltage the pulse of EFT coupled to

the bus line through the coupling box (CCC method), as [Figure 7](#). So the AZKN6129P has more ability to communicate with low Bit-Error-Rate (BER) under the high noise environment.

High Protection for All Pins

- **±12 kV System-level ESD for CANH and CANL**

AZKN6129P is embedded high voltage ±70 V TVS on the pins of CANH and CANL to achieve IEC 61000-4-2 contact ±12 kV of the system-level ESD protection. In the evaluation of system-level ESD, both CANH and CANL of AZKN6129P are zapped by ESD gun referred to GND on the evaluation board.

- **Basic surge protection for CANH and CANL**

AZKN6129P pass ±100 V of the IEC 61000-4-5 (8/20 μ s) with 2 Ω of source impedance for directly injection. With both the surge and fault protection, AZKN6129P can efficiently prevent the EOS event in the harsh environment.

- **HBM 5 kV, MM 400 V and CDM 800 V for all pins**

To achieve the high reliability and high assembly yield rate, AZKN6129P have high ESD specification of the component-level for both HBM and MM. With the high robust whole-chip ESD protection, AZKN6129P can still sustain no matter the ESD pulse comes from power pin or the I/O pins. For the IC self-discharge issue, the CDM protection level of AZKN6129P is up to ±800 V.

[Table 1. Operating modes](#)

STB Pin		Low	High
Mode		Normal	Standby
Bus pins (CANH, CANL)		Dominant / Recessive	Bias to GND ^[1]
RXD	High	Recessive	No Wake-up
	Low	Dominant	Wake-up ^[1]

[1] In standby mode, the standby RX is active to wake-up MCU.

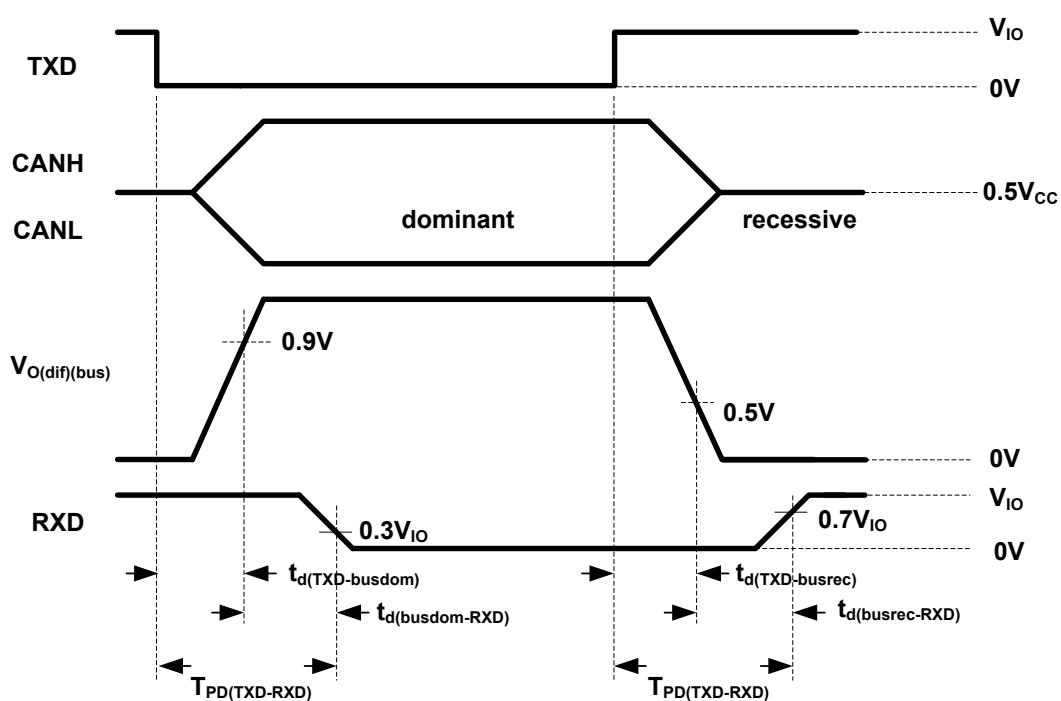


Figure 1. Timing diagram of the CAN transceiver.

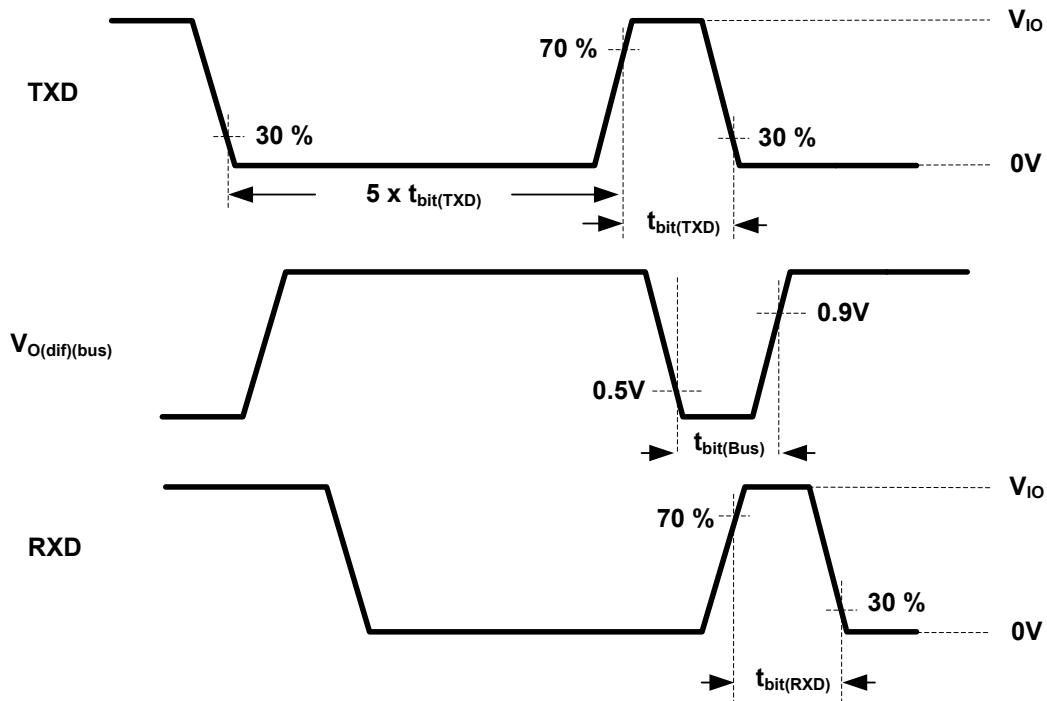


Figure 2. Timing diagram for loop delay symmetry.

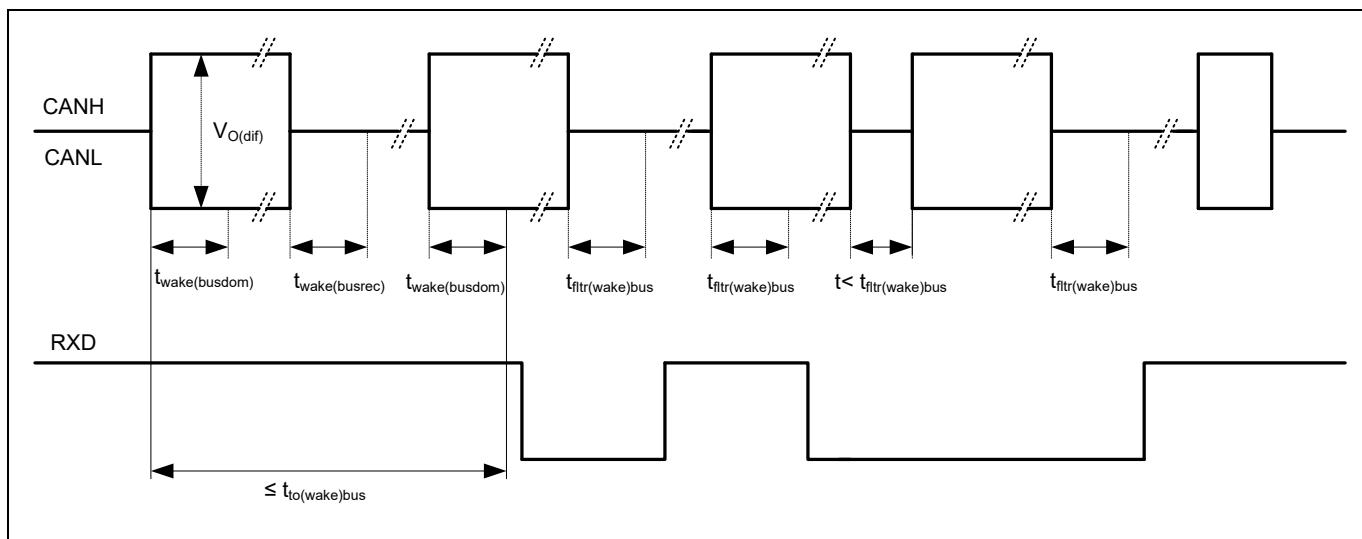


Figure 3. Timing diagram for wake-up pattern.

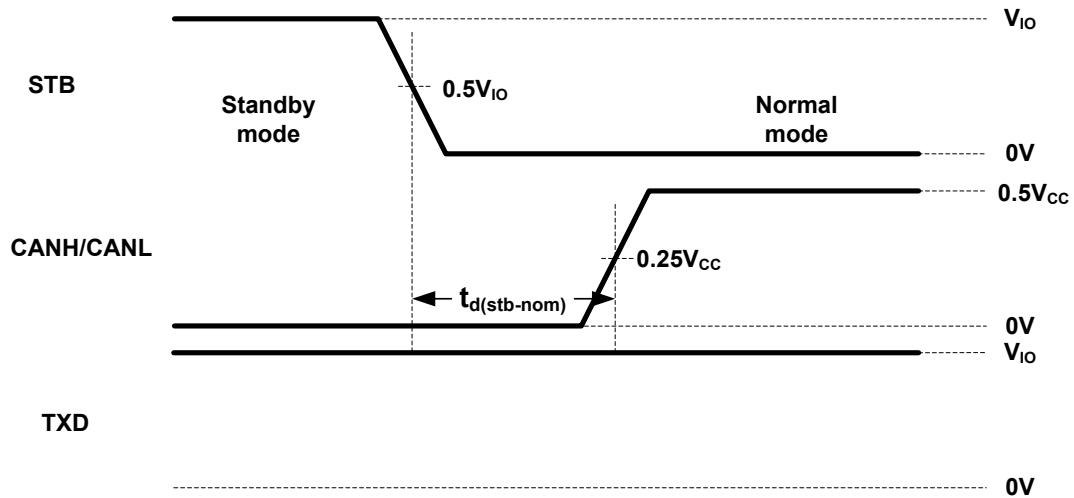


Figure 4. Timing diagram for the delay of the standby to normal mode.

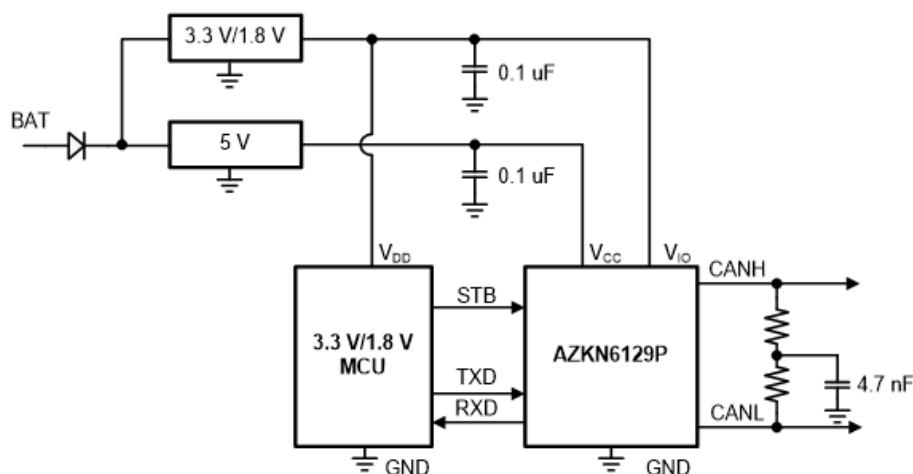


Figure 5. Typical application circuit for AZKN6129P with 3.3 V or 1.8 V MCU.

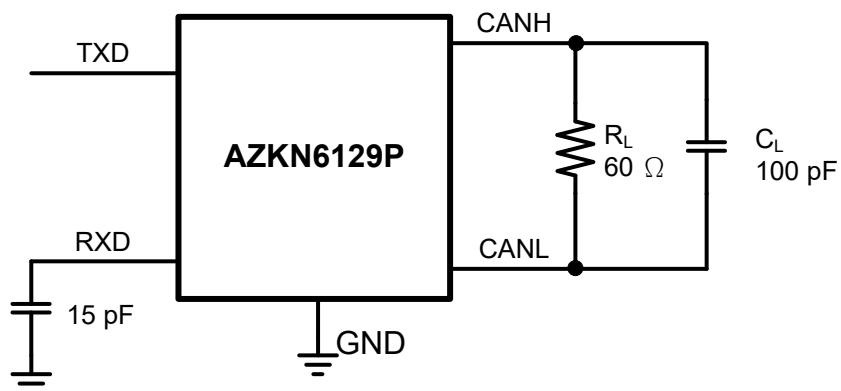


Figure 6. CAN transceiver timing test circuit.

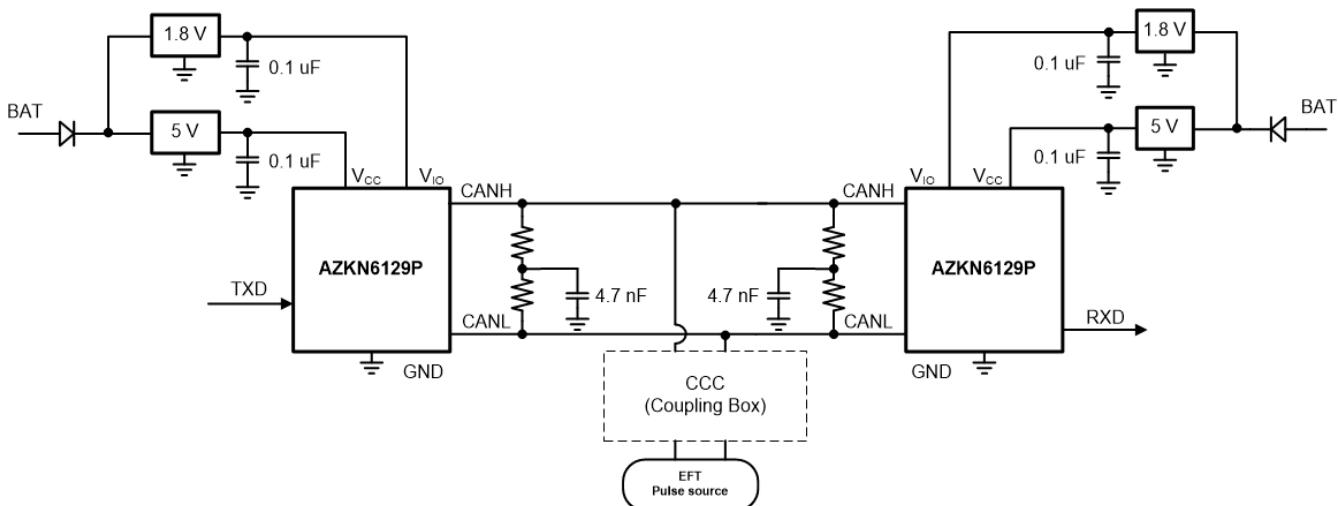


Figure 7. EFT coupling test circuit for AZKN6129P.

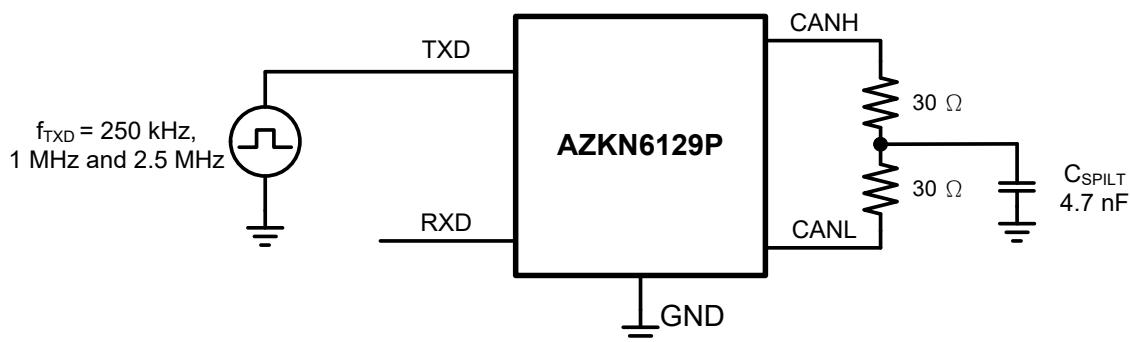


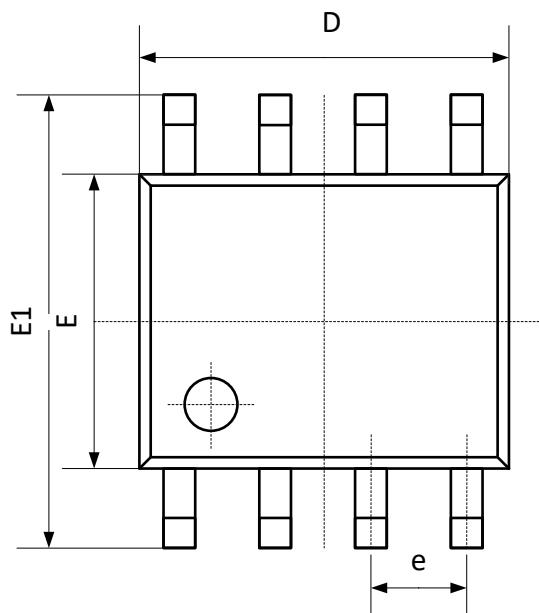
Figure 8. Test circuit for measuring transmitter driver symmetry.



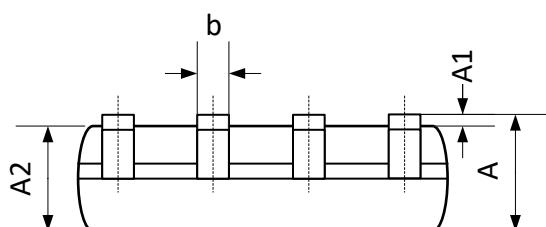
Mechanical Details

PACKAGE DIAGRAMS

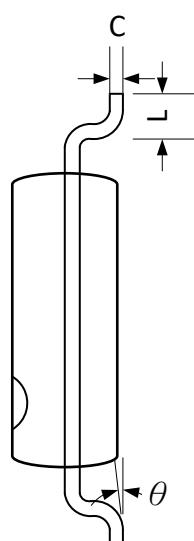
TOP VIEW



SIDE VIEW



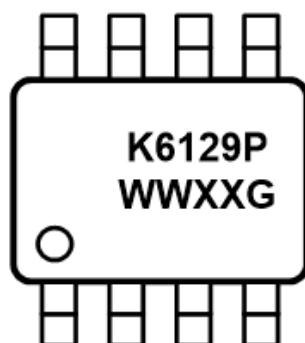
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

MARKING CODE



K6129P = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZKN6129P.RDG	K6129P WWXXG



Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZKN6129P.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes = 12,500/carton

Revision History

Revision Date	Modification Description
2024/07/10	Formal Release