

# AZP94

## ECL/PECL $\div 1$ , $\div 2$ Clock Generation Chip with Tristate Compatible Outputs

### FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Package Available
- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Tristate Compatible Outputs
- Input Buffer Powers Down when Disabled
- Selectable Input Biasing
- High Bandwidth for  $\geq 1$ GHz
- Available in a MLP 8 (2x2) Package
- IBIS Model File Available on Arizona Microtek Website

### PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZP94NAG	J4G <Date Code>	1,2
DIE	AZP94XP	N/A	3,4

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" for year followed by "WW" for week.
- 3 Waffle Pack, die thickness 180 $\mu$ .
- 4 Contact factory for availability.

### DESCRIPTION

The AZP94 is a specialized  $\div 1$  or  $\div 2$  clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the AZP94 functions as a standard receiver. If DIV-SEL is connected to  $V_{EE}$ , it functions as a  $\div 2$  divider.

Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC),  $V_{EE}$ , or connected to  $V_{EE}$  via a 20k $\Omega \pm 20\%$  resistor. Leaving EN-SEL open or connecting it to  $V_{EE}$  allows the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75k $\Omega$  pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to  $V_{EE}$ , an internal 75k $\Omega$  pull-down resistor is selected which disables the outputs whenever EN is left open.

Connecting the EN-SEL to  $V_{EE}$  with a 20k $\Omega$  resistor will allow the EN pin/pad to function as an active low PECL/ECL enable with an internal 75k $\Omega$  pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). The default logic condition can be overridden by connecting the EN to  $V_{CC}$  with an external resistor of  $\leq 20$ k $\Omega$ . If the enable signal is CMOS (rail-to-rail) and the logic sense is active low (EN-SEL connected to  $V_{EE}$  with a 20k $\Omega$  resistor), the EN pin/pad voltage swing must be reduced using two external resistors. Contact the factory for details.

When the AZP94 is disabled, the Q and Q outputs are forced LOW and the input buffer is powered down to minimize feed through. This feature allows tristate compatible parallel output connections. Multiple AZP94 chip outputs can be wired together. Since both outputs are forced LOW in the disable mode, an enabled AZP94 can drive the output lines without interference from the unselected units. In addition, the AZP94 can be used in parallel connection with PECL/ECL parts whose outputs are high impedance when disabled.

The EN pin/pad also functions as a reset when the  $\div 2$  mode is selected. In the  $\div 2$  mode, the counter resets when the outputs are disabled.

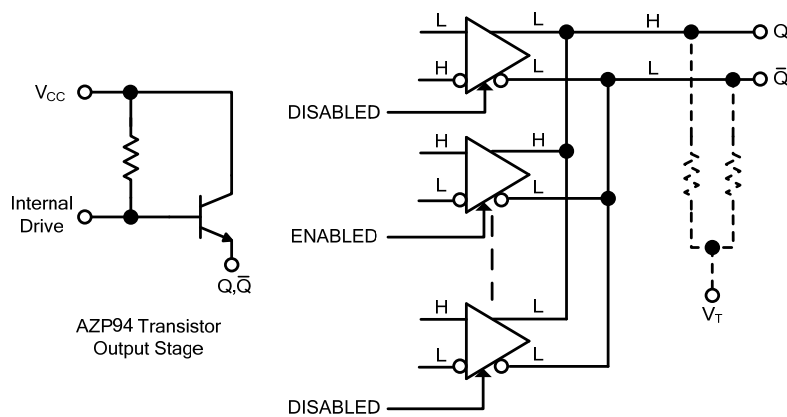
## AZP94

### MLP 8, 2x2 mm Package (AZP94NA)

The AZP94NA provides a  $V_{BB}$  with an 1880 $\Omega$  internal bias resistor from D to  $V_{BB}$ . This feature allows AC coupling with minimal external components. The  $V_{BB}$  pin supports 1.5mA sink/source current and should be bypassed to ground or  $V_{CC}$  with a 0.01  $\mu$ F capacitor.

### DIE (AZP94X)

The AZP94X provides a  $V_{BB}$  and a BIAS pad with 940 $\Omega$  internal resistors from D to BIAS and D to BIAS. Connecting the BIAS pad to  $V_{BB}$  allows D and D to be AC coupled with minimal external components. For single ended applications, D or D may be connected directly to  $V_{BB}$  to form a single 1880 $\Omega$  bias resistor. The  $V_{BB}$  pin supports 1.5mA sink/source current. Whenever used, the  $V_{BB}$  should be bypassed to ground or  $V_{CC}$  with a 0.01  $\mu$ F capacitor.



### TYPICAL TRISTATE COMPATIBLE OPERATION

#### Tristate Compatible Operation

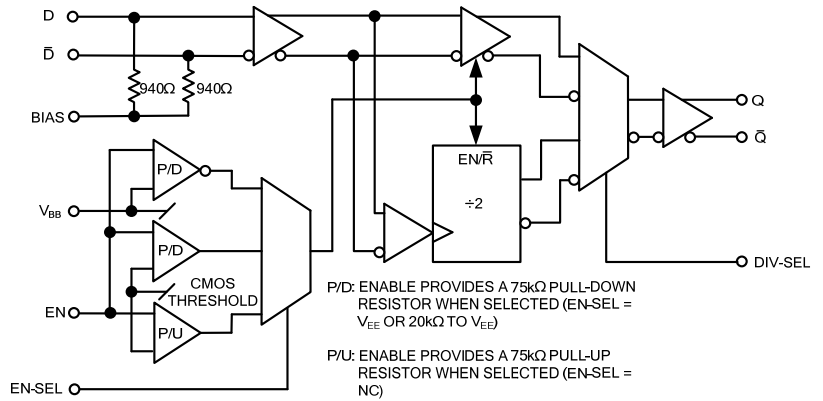
The outputs of the AZP94 are emitter followers as shown in the left side of the drawing. When a part is disabled, both outputs are set in the LOW state. This allows a HIGH output from an enabled part to override a disabled output and pull the combined line HIGH as seen in the right hand side of the drawing. When the enabled part output is LOW, the combined line remains LOW.

If all connected AZP94 parts are disabled, both output lines will be in the LOW state.

NOTE: The specifications in the ECL/PECL tables are valid when thermal equilibrium has been established.

**SIGNAL DESCRIPTION**

PIN/PAD	FUNCTION
D/D	Data Inputs
Q/Q	Data Outputs
V <sub>BB</sub>	Reference Voltage Output
BIAS	Input Bias Return
EN	Enable/Reset Input
EN-SEL	Enable Logic Select
DIV-SEL	Divide Ratio Select
V <sub>EE</sub>	Negative Supply
V <sub>CC</sub>	Positive Supply



**ENABLE TRUTH TABLE**

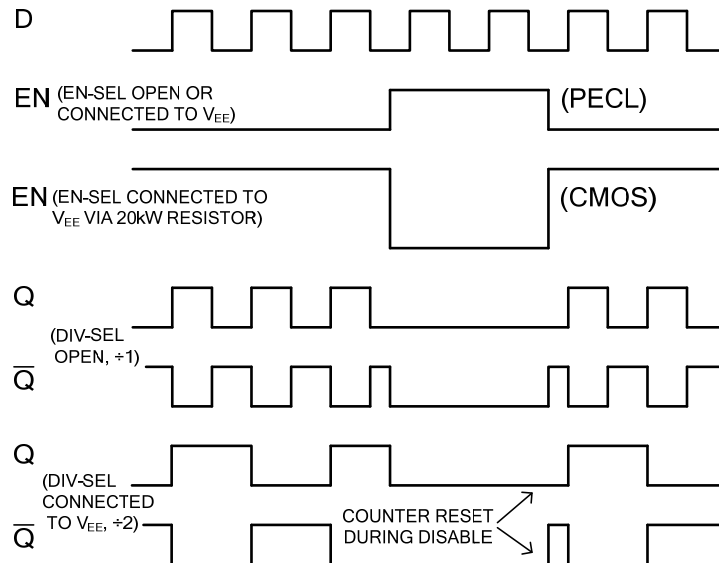
EN-SEL	EN	Q	Q̄
NC	CMOS Low or V <sub>EE</sub> <sup>1</sup>	Low	Low
NC	CMOS High, V <sub>CC</sub> or NC	Data	Data
V <sub>EE</sub>	CMOS Low, V <sub>EE</sub> or NC <sup>1</sup>	Low	Low
V <sub>EE</sub>	CMOS High or V <sub>CC</sub>	Data	Data
20kΩ to V <sub>EE</sub>	PECL Low, V <sub>EE</sub> or NC <sup>1</sup>	Data	Data
20kΩ to V <sub>EE</sub>	PECL High or V <sub>CC</sub>	Low	Low

<sup>1</sup> Counter Reset for ÷2 Ratio

**DIVIDE TRUTH TABLE**

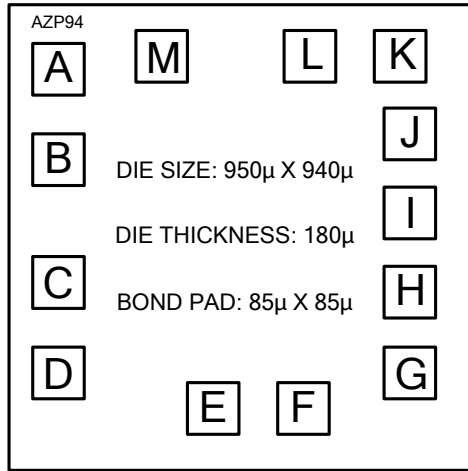
DIV-SEL	DIVIDE RATIO
NC	÷1
V <sub>EE</sub> <sup>1</sup>	÷2

<sup>1</sup> DIV-SEL connection must be ≤1Ω.



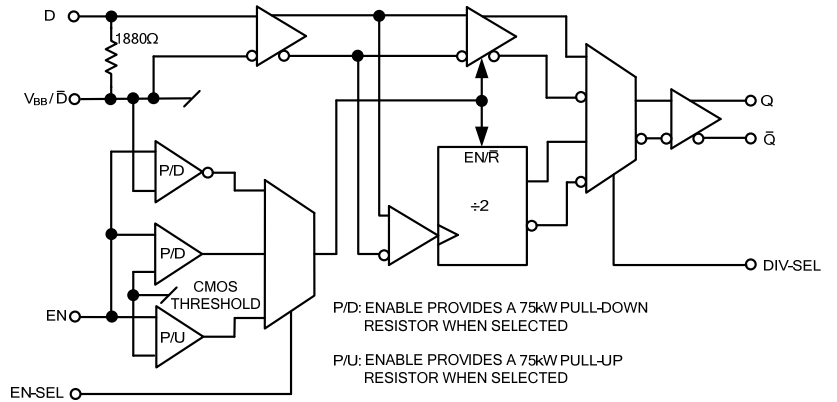
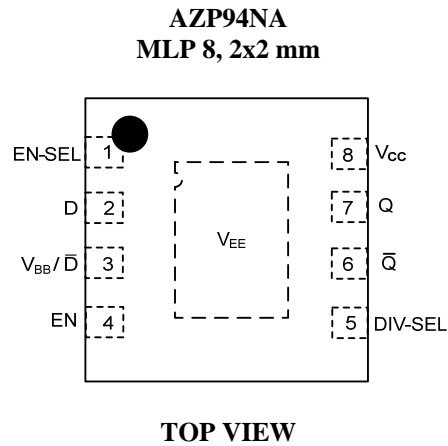
**TIMING DIAGRAM**

**DIE PAD COORDINATES**



NAME	SIGNAL	X (Microns)	Y (Microns)
A	D	-342.5	312.5
B	D	-342.5	144.5
C	BIAS	-342.5	-87.0
D	V <sub>BB</sub>	-342.5	-255.0
E	EN	-33.5	-312.5
F	V <sub>EE</sub>	126.5	-312.5
G	DIV-SEL	312.5	-248.5
H	Q	312.5	-98.5
I	Q	312.5	51.5
J	NC	312.5	201.5
K	V <sub>CC</sub>	302.5	342.5
L	V <sub>CC</sub>	142.5	342.5
M	EN-SEL	-140.5	342.5

Note: 1. The die backside may be left open or connected to V<sub>EE</sub>.



**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
V <sub>CC</sub>	PECL Power Supply (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>I</sub>	PECL Input Voltage (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>EE</sub>	ECL Power Supply (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
V <sub>I</sub>	ECL Input Voltage (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
I <sub>HGOUT</sub>	Output Current — Continuous — Surge	50 100	mA
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

**100K ECL DC Characteristics (V<sub>EE</sub> = -3.0V to -5.5V, V<sub>CC</sub> = GND)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1</sup>	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1</sup>	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage D/D, EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	-1165 V <sub>EE</sub> +2000	-740 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-740 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-740 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-740 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage D/D, EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	-1900 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1900 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1900 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1900 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	mV
V <sub>BB</sub>	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I <sub>IH</sub>	Input HIGH Current EN		150		150		150		150	µA
I <sub>IL</sub>	Input LOW Current EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		µA
I <sub>EE</sub>	Power Supply Current <sup>1</sup>		34		34		34		37	mA

1. Specified with outputs terminated through 50Ω resistors to V<sub>CC</sub> - 2V.
2. EN-SEL connected to V<sub>EE</sub> through a 20kΩ resistor
3. EN-SEL connected V<sub>EE</sub> or left open (NC)

**100K LVPECL DC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.3V)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1,2</sup>	2215	2420	2275	2420	2275	2420	2275	2420	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1,2</sup>	1400	1745	1400	1680	1400	1680	1400	1680	mV
V <sub>IH</sub>	Input HIGH Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	mV
V <sub>BB</sub>	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
I <sub>IH</sub>	Input HIGH Current EN		150		150		150		150	µA
I <sub>IL</sub>	Input LOW Current EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		µA
I <sub>EE</sub>	Power Supply Current <sup>2</sup>		34		34		34		37	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V<sub>CC</sub> - 2V.
3. EN-SEL connected to V<sub>EE</sub> through a 20kΩ resistor
4. EN-SEL connected V<sub>EE</sub> or left open (NC)

**100K PECL DC Characteristics** ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +5.0\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3915	4120	3975	4120	3975	4120	3975	4120	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3100	3445	3100	3380	3100	3380	3100	3380	mV
$V_{IH}$	Input HIGH Voltage <sup>1</sup>									
	D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage <sup>1</sup>									
	D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current									
	EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		34		34		34		37	mA

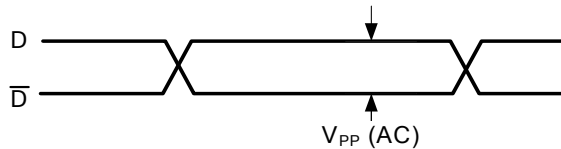
1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to  $V_{CC} - 2\text{V}$ .
3. EN-SEL connected to  $V_{EE}$  through a 20kΩ resistor
4. EN-SEL connected  $V_{EE}$  or left open (NC)

**AC Characteristics** ( $V_{EE} = -3.0\text{V}$  to  $-5.5\text{V}$ ;  $V_{CC} = \text{GND}$  or  $V_{EE} = \text{GND}$ ;  $V_{CC} = +3.0\text{V}$  to  $+5.5\text{V}$ )

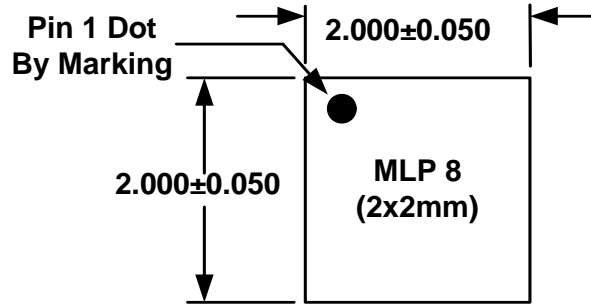
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH} / t_{PHL}$	Propagation Delay													ps
	D to Q/Q Outputs <sup>1</sup> (SE) EN to Q/Q Outputs <sup>1,2</sup>			450 3000			450 3000			450 3000			450 3000	
$t_{SKEW}$	Duty Cycle Skew <sup>3</sup> (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}(\text{AC})$	Differential Input Swing <sup>4</sup>	150		1000	150		1000	150		1000	150		1000	mV
$t_r / t_f$	Output Rise/Fall <sup>1</sup> (20% - 80%)	100		240	100		240	100		240	100		240	ps

1. Specified with outputs terminated through 50Ω resistors to  $V_{CC} - 2\text{V}$ .
2. Specified from 50% EN input edge to  $V_{OH}$  min or  $V_{OL}$  max of the Q/Q outputs
3. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
4. The peak-to-peak differential input swing is the range for which AC parameters are guaranteed. The device has a voltage gain of  $\approx 100$ .

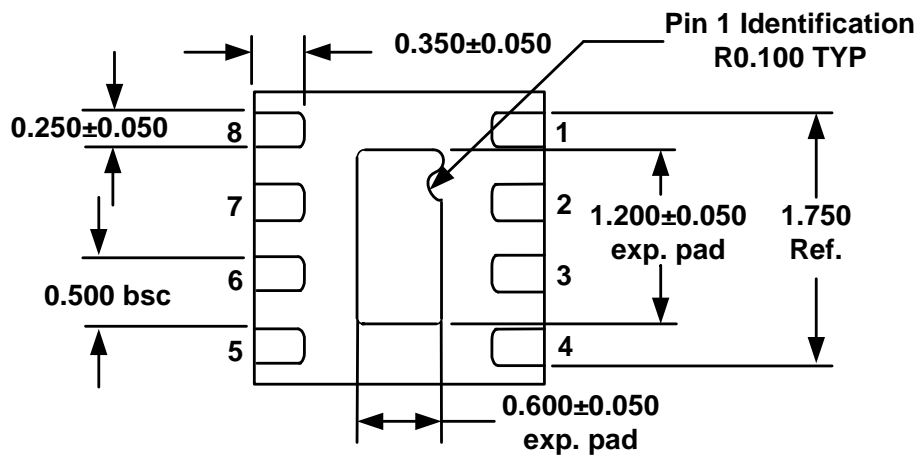
**AC PP INPUT**



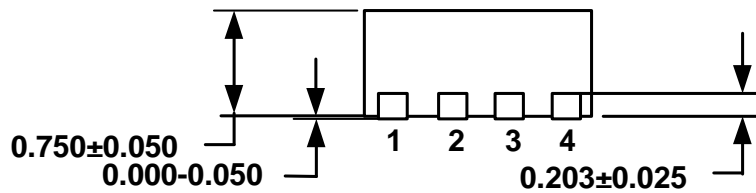
**PACKAGE DIAGRAM**  
**MLP 8 2x2mm**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

**Note: All dimensions are in mm**

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