Features

- Meet EIA/TIA-232-F standards from a +3.0V to +5.5V power supply
- Guaranteed data rate 2Mbps under loading
- Two Transmitters and Two Receivers design
- Latch-up free
- External Capacitor : 4 x 0.1μF
- Accepts 5V Logic Input under 3.3V supply
- Integrated ESD Transient Voltage Suppressor (TVS) in the Transceiver IC
- TVS protection Immunities for Bus Terminals:
  ± 8 kV IEC 61000-4-2 Contact Discharge
  ±15kV IEC 61000-4-2 Air Discharge

Applications

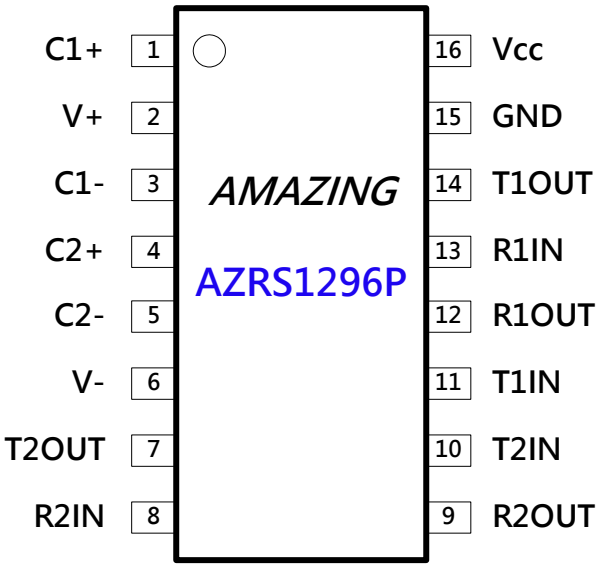
- Portable Computers
- Battery-Powered Systems
- Production Data Acquisition (PDA) and Point of Sale (POS) terminal
- Routers and HUBs
- Peripherals and Printers
- Industrial Controlled Machine

Description

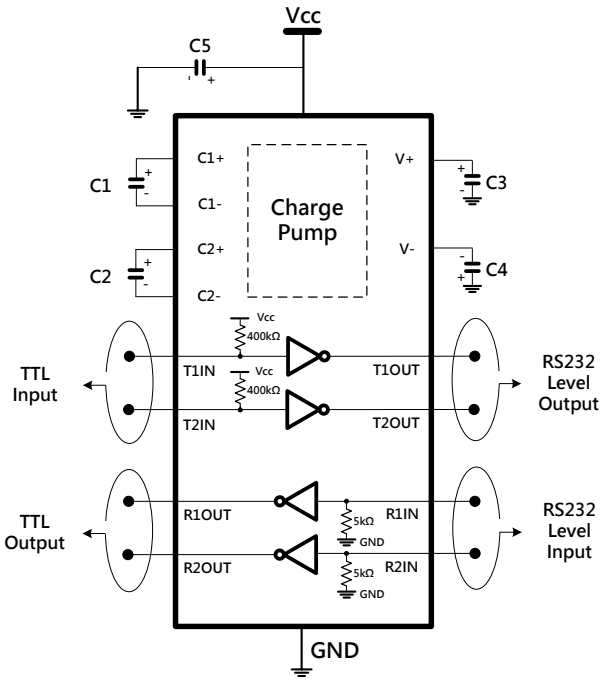
AZRS1296P is an RS-232 transceiver that meets the EIA/TIA-232-F standards under supply power +3.0V to +5.5V. AZRS1296P is a 2-transmitter and 2-receiver device with a high-efficient charge pump circuit embedded. This high-efficient charge pump circuit with 0.1μF external capacitors provides the bipolar output to the transmitters.

AZRS1296P operates with ultra low power consumption under guaranteed data rate of 2Mbps. AZRS1296P is ideal transceiver IC for portable application such as notebook or PDA.

AZRS1296P is also a high reliable device with both latch-up free and enhanced ESD protection. All the outputs of transmitters and the inputs of receivers can meet the specifications of IEC 61000-4-2 contact ±8kV, and air ±15kV.



Pin Configuration for AZRS1296P



Functional Block of AZRS1296P

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNIT**
Power Supply Vcc	Vcc	-0.3 to +6.0	V
Charge Pump Positive Output V+	V+	-0.3 to +9.5	V
Charge Pump Negative Output V-	V-	+0.3 to -9.5	V
V+, V- Supply voltage difference	|V+ - V-|	19	V
Transmitter Input	TxIN	-0.3 to (Vcc +0.3)	V
Receiver Input	RxIN	±25	V
Transmitter Output	TxOUT	±13.2	V
Receiver Output	RxOUT	-0.3 to (Vcc +0.3)	V
Operating Temperature	T_{OP}	-40 to +125	°C
Storage Temperature	T_{STO}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

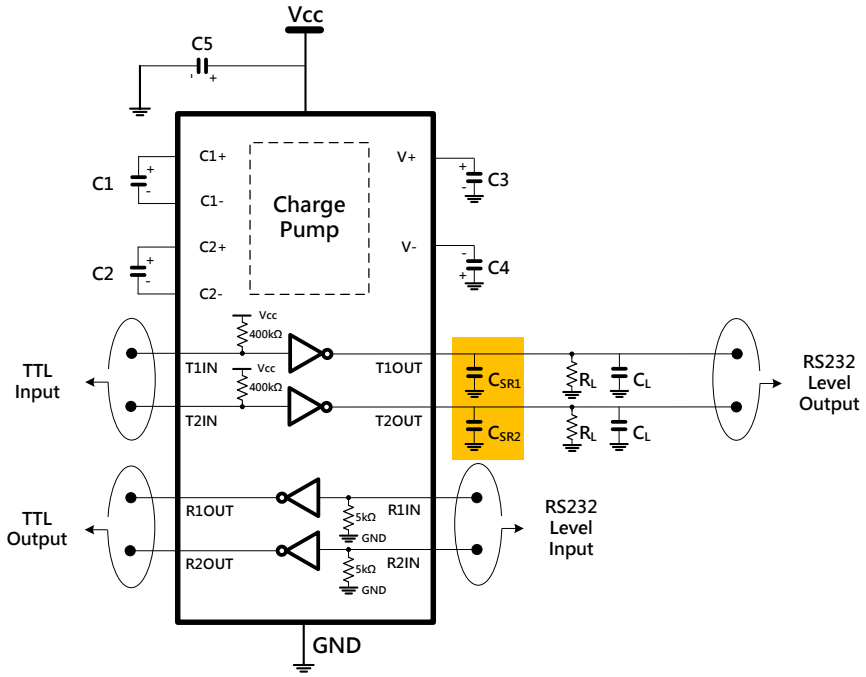
Unless otherwise noted, the following specifications apply for Vcc=+3.0V to +5.5V with T_{AMB}= -40 °C to +125 °C. C1 to C4=0.1μF. Typical values apply at Vcc=+5V and T_{AMB}=25 °C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTIC					
Supply Current	TxIN=Floating or Vcc or GND, No Load		0.3	3	mA
LOGIC INPUTS					
Logic Input Voltage Low	TxIN, Vcc=3.3V			0.8	V
	TxIN, Vcc=5V			0.8	V
Logic Input Voltage High	TxIN, Vcc=3.3V	2.0			V
	TxIN, Vcc=5V	2.4			V
Logic Input Pull-up Current	TxIN=GND		12	25	uA
TRANSMITTER OUTPUTS					
Output Voltage Swing	3kΩ load to ground, Vcc=3.3V	±4.4	±5		V
	3kΩ load to ground, Vcc=5V	±5	±8		V
Output Resistance	Vcc=V+=V-=0V, V_{OUT}=±2V	300			Ω
Output Short-Circuit Current	V_{OUT}=0V		±25	±60	mA
Output Leakage Current	V_{OUT}=±12V, Vcc=0V.		±10		uA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVER INPUTS and OUTPUTS					
Input Voltage Range		-25		25	V
Positive-going input threshold voltage	Vcc=3.3V		1.7	2.4	V
	Vcc=5.0V		2.0	2.4	
Negative-going input threshold voltage	Vcc=3.3V	0.8	1.4		V
	Vcc=5.0V	0.8	1.7		
Input Hysteresis			0.3		V
High-level output voltage	I_{OH}=-1mA	Vcc -0.6	Vcc – 0.1		V
Low-level output voltage	I_{OL}=+1.6mA			0.4	V
Input Resistance		3	5	7	kΩ
TIMING CHARACTERISTICS					
TRANSMITTER					
Maximum Data Rate	R_L=3kΩ, C_L=150pF, one transmitter switching		2		Mbps
Transmitter Propagation Delay	t_{DPHL}, TxIN to TxOUT, R_L=3kΩ, C_L=150pF		100		ns
	t_{DPLH}, TxIN to TxOUT, R_L=3kΩ, C_L=150pF		100		
Transmitter Skew	| t_{DPHL} – t_{DPLH} |, R_L=3kΩ, C_L=150pF		20		ns
Transition-Region Slew Rate	R_L=3kΩ, C_{LT}=2200pF, One Transmitter Switching, transition from -3.0V to +3.0V or +3.0V to -3.0V (See Note 1)		12		V /μs
Receiver					
Receiver Propagation Delay	t_{RPHL}, RxIN to RxOUT, C_L=150pF		800		ns
	t_{RPLH}, RxIN to RxOUT, C_L=150pF		800		
Receiver Skew	| t_{RPHL} – t_{RPLH} |, C_L=150pF		20		ns
ESD PROTECTION					
Pin Name (Pin Number)	**Test Condition**				
RxIN(8,13) TxOUT(7,14)	IEC61000-4-2 Contact	-8		+8	kV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	IEC61000-4-2 Air	-15		+15	kV
All Other Pins	HBM	-2		+2	kV

Note 1:
C_{LT} includes C_{SR} & C_L.
C_{SR} is application circuit for slew-rate (Low-speed).
C_L includes probe and jig capacitance.



Application circuit for note 1

PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Description
1	C1+	Positive terminal of the first switch capacitor
2	V+	Positive voltage of charge pump output
3	C1-	Negative terminal of the first switch capacitor
4	C2+	Positive terminal of the second switch capacitor
5	C2-	Negative terminal of the second switch capacitor
6	V-	Negative voltage of charge pump output
7	T2OUT	Second transmitter output
8	R2IN	Second receiver input
9	R2OUT	Second receiver output
10	T2IN	Second transmitter input
11	T1IN	First transmitter input
12	R1OUT	First receiver output
13	R1IN	First receiver input
14	T1OUT	First transmitter output
15	GND	Ground of the device
16	Vcc	+3.0V to +5.5V supply voltage

Detail Description

AZRS1296P is a RS-232 transceiver that meets the EIA/TIA-232 and V.28/V.24 communication protocols. AZRS1296P is a 2-transmitter /2-receiver device with a high-efficient charge pump circuit embedded. The design of high-efficient charge pump circuit is Amazing's property that can generate RS-232 voltage levels from +3.0V to +5.5V power supply. This high-efficient charge pump circuit with 0.1μF capacitors provides the bipolar output to the transmitters, and makes the transmitters deliver the RS-232 output voltage levels. The design of transmitter is also the property of Amazing. Under normal operation and with loaded, AZRS1296P can operate for guaranteed data rate of 2Mbps with ultra low power consumption. Therefore, AZRS1296P is ideal for portable application such as notebook or PDA.

AZRS1296P is also a high reliable device with both latch-up free and high ESD immunity. The high robust ESD devices embedded in AZRS1296P are also the properties of Amazing. All the outputs of transmitters and the inputs of receivers can meet the specifications of IEC 61000-4-2 contact ±8kV, and air ±15kV.

Bipolar Charge Pump Circuit

High-efficient charge pump circuit in AZRS1296P is a four-capacitance structure with single power supply input. Bipolar voltage output of AZRS1296P can be pumped to above ±5.0V under the +3.0V to +5.5V supply power range. Because a negative feedback regulator is embedded, the output voltage is independent of supply power voltage. Moreover, the charge pump can select 2-phase or 4-phase operation for more flexible design. When AZRS1296P is powered on, the bipolar output will be pumped to the steady output with low ripple voltage in the 500μs.

Transmitter

The design of the transmitter is an inverted translator that converts TTL/CMOS-logic voltage level to EIA/TIA-232 voltage level. The transmitters of AZRS1296P guarantee a 2Mbps data rate under the loading of 3kΩ resistance in parallel with 150pF capacitance. When the transmitters are active, the input signals of transmitters will be transported to the outputs of transmitters in inverting level.

The inputs of transmitters have 400kΩ pull-up resistors design to ensure the output of transmitter to be a LOW state when the input of transmitter is unconnected.

Receiver

The receivers of AZRS1296P convert EIA/TIA-232 voltage levels to TTL/CMOS-logic voltage levels.

The receiver guarantees a 2Mbps data rate under the loading of a 150pF.

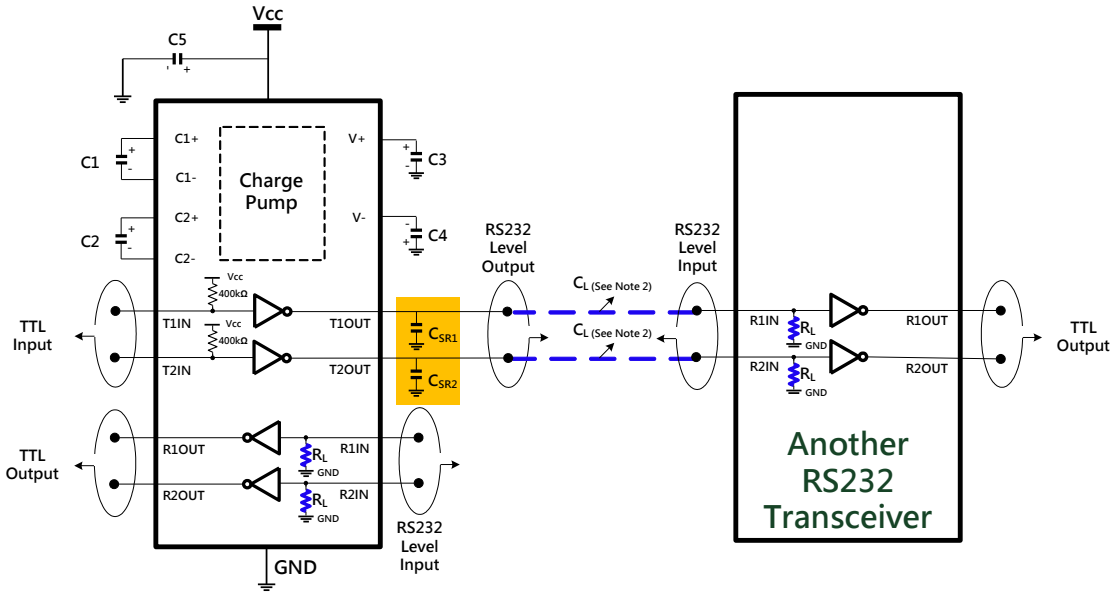
The inputs of receivers have 5kΩ pull-down resistors design to ensure the output of receiver to be a HIGH state when the input of receiver is unconnected.

Application Information

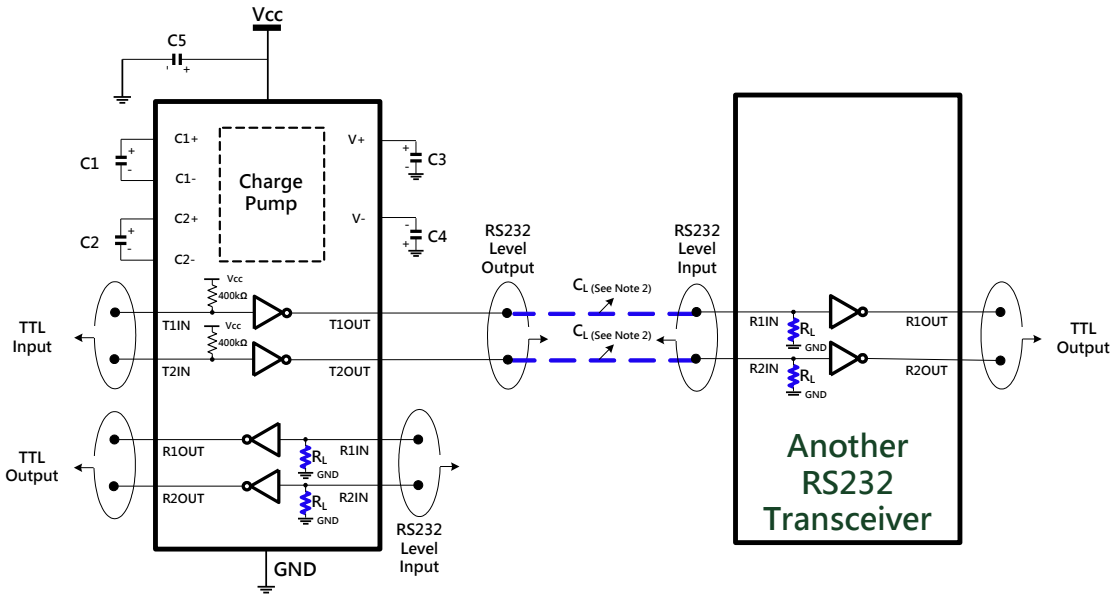
To generate the high-efficient bipolar charge pump, the four capacitors (C1 ~ C4) must be placed as closer to RS232 transceiver as possible. The trace of the PCB layout is suggested to be shorter than 1cm from the pinout of the charge pump to the dedicated capacitor. The other node of dedicated capacitor should be connected to ground shortly, too. Moreover, the capacitor of power supply (C5) should be placed as close to the transceiver as possible, and connect to ground nearby.

If Slew-rate (Low speed) is required, it can be connected to the application circuit: C_{SR1} & C_{SR2} are connected to T1OUT & T2OUT (Recommended value of C_{SR1} & C_{SR2} = 2200pF)

In other applications, C3 could be changed to connect to Vcc.

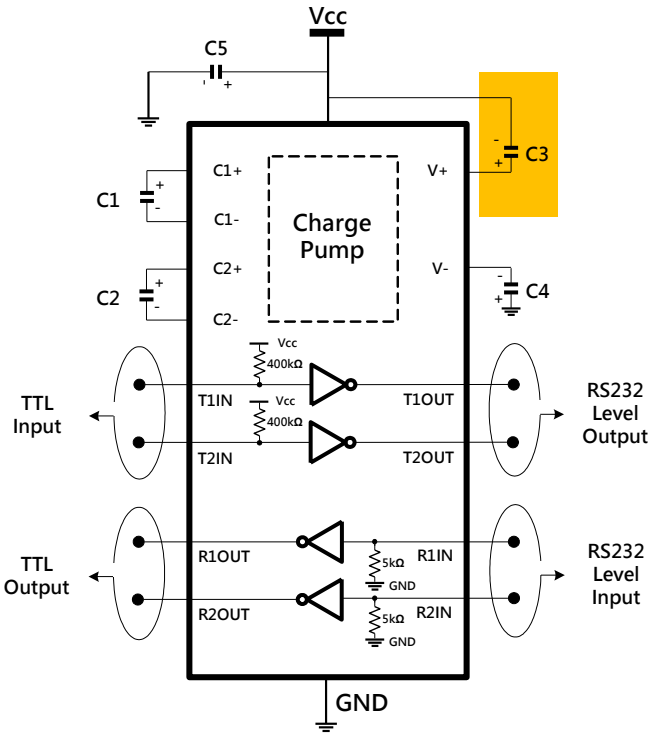


Operation of AZRS1296P for Slew-rate (Low-speed)



Operation of AZRS1296P (High-speed)

Note 2:
C_L includes probe and jig capacitance



Application circuit for note 3

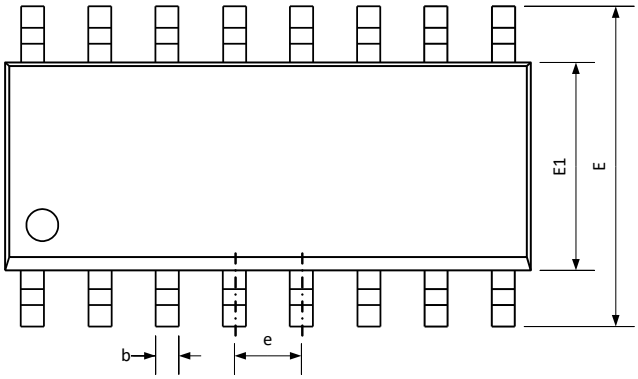
Note 3:
C3 could be changed to connect to Vcc

Mechanical Details

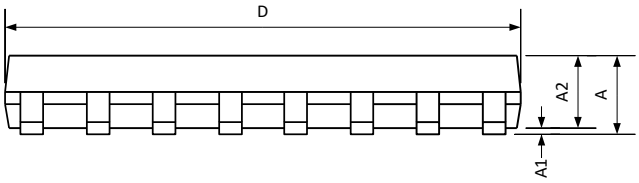
SOP-16L(150)

PACKAGE DIAGRAMS

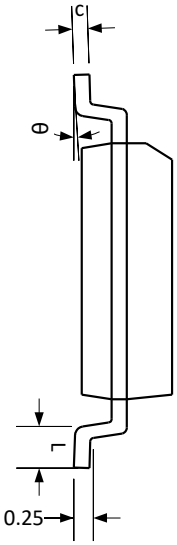
TOP VIEW



SIDE VIEW



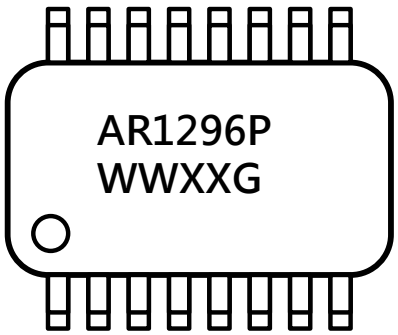
END VIEW



PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	-	1.75
A1	0.05	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.17	0.26
D	9.7	10.2
E	5.8	6.2
E1	3.7	4.1
e	1.27 BSC	
L	0.4	1.27
θ	0	8

Marking Code



AR1296P = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZRS1296P.RDG (Green part)	AR1296P WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZRS1296P.RDG	Green	T/R	13 inch	2,500/reel	1 reel =2,500/box	5 box = 12,500/carton

Revision History

Revision	Modification Description
Revision 2024/03/29	Formal Release
Revision 2024/09/23	Upgrade min. of Output Voltage Swing & Add Application information