Features

- Meets EIA/TIA-232-F standards from a +3.0V to +5.5V power supply
- Guaranteed data rate 2Mbps under loading
- Four Transmitters and Five Receivers design
- Latch-up free
- External Capacitor : 4 x 0.1μF
- Accepts 5V Logic Input under 3.3V supply
- Integrated ESD Transient Voltage Suppressor (TVS) in the Transceiver IC
- TVS protection Immunities for Bus Terminals:
  ± 8 kV IEC 61000-4-2 Contact Discharge
  ±15kV IEC 61000-4-2 Air Discharge

Applications

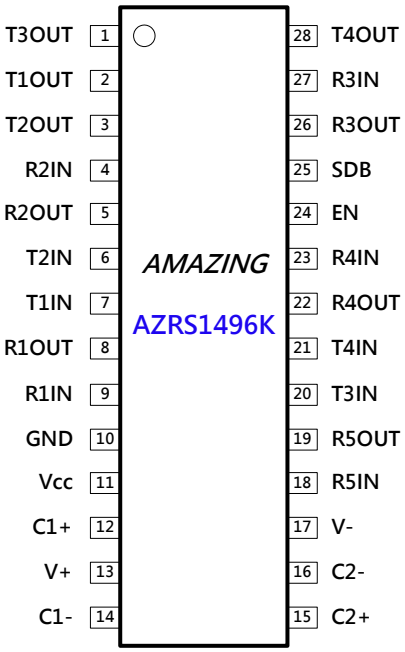
- Portable Computers
- Battery-Powered Systems
- Production Data Acquisition (PDA) and Point of Sale (POS) terminal
- Routers and HUBs
- Peripherals and Printers
- Industrial Controlled Machine

Description

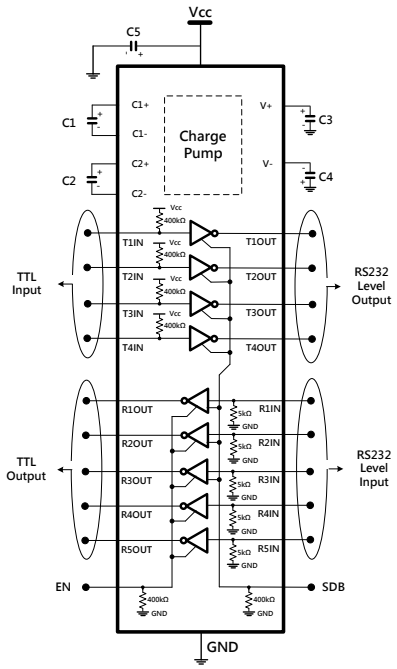
AZRS1496K is an RS-232 transceiver that meets the EIA/TIA-232-F standards under supply power +3.0V to +5.5V. AZRS1496K is a 4-transmitter and 5-receiver device with a high-efficient charge pump circuit embedded. This high-efficient charge pump circuit with 0.1μF external capacitors provides the bipolar output to the transmitters.

AZRS1496K operates with ultra low power consumption under guaranteed data rate of 2Mbps. Moreover, the bipolar output voltage of charge pump will be Vcc tied to V+ and GND tied to V-, respectively in shutdown mode. The output of transmitter will be high impedance under the shutdown mode. Therefore, AZRS1496K is an ideal transceiver IC for portable application such as notebook or PDA.

AZRS1496K is also a high reliable device with both latch-up free and enhanced ESD protection. All the outputs of transmitters and the inputs of receivers can meet the specifications of IEC 61000-4-2 contact ±8kV, and air ±15kV.



Pin Configuration for AZRS1496K



Functional Block of AZRS1496K

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Power Supply Vcc	Vcc	-0.3 to +6.0	V
Charge Pump Positive Output V+	V+	-0.3 to +9.5	V
Charge Pump Negative Output V-	V-	+0.3 to -9.5	V
V+, V- Supply voltage difference	|V+ - V-|	19	V
Transmitter Input and Enable Pin	TxIN , EN, SDB	-0.3 to (Vcc +0.3)	V
Receiver Input	RxIN	±25	V
Transmitter Output	TxOUT	±13.2	V
Receiver Output	RxOUT	-0.3 to (Vcc +0.3)	V
Operating Temperature	T_{OP}	-40 to +125	^{o}C
Storage Temperature	T_{STO}	-65 to +150	^{o}C

ELECTRICAL CHARACTERISTICS

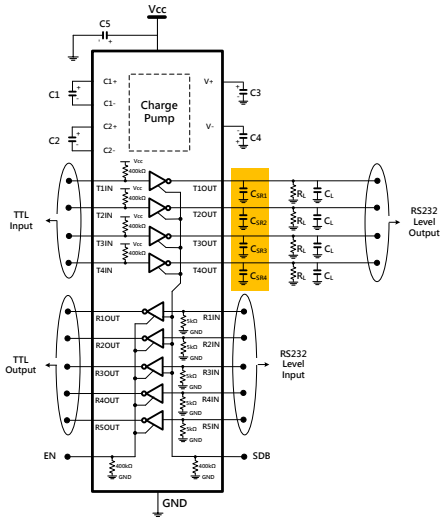
Unless otherwise noted, the following specifications apply for Vcc=+3.0V to +5.5V with T_{AMB}= -40 ^{o}C to +125 ^{o}C. C1 to C4=0.1μF. Typical values apply at Vcc=+5V and T_{AMB}=25 ^{o}C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Supply Current	SDB=Vcc, TxIN=Floating or Vcc or GND, No load		0.3	3	mA
Shutdown Supply Current	SDB=GND, EN=Floating or GND, TxIN=Floating or Vcc or GND, No load		10	100	μA
LOGIC INPUTS					
Logic Input Voltage Low	TxIN, EN, SDB, Vcc=3.3V			0.8	V
	TxIN, EN, SDB, Vcc=5V			0.8	V
Logic Input Voltage High	TxIN, EN, SDB, Vcc=3.3V	2.0			V
	TxIN, EN, SDB, Vcc=5V	2.4			V
Logic Input Pull-up Current	TxIN=GND		12	25	μA
Logic Input Pull-down Current	EN, SDB=Vcc		12	25	μA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER OUTPUTS					
Output Voltage Swing	3kΩ load to ground, Vcc=3.3V	±3.3	±5		V
	3kΩ load to ground, Vcc=5V	±5	±8		V
Output Resistance	Vcc=V+=V-=0V, V_{OUT}=±2V	300			Ω
Output Short-Circuit Current	V_{OUT}=0V		±25	±60	mA
Output Leakage Current	SDB=GND, V_{OUT}=±12V, Vcc=0V or 3.0V to 5.5V, Transmitters disabled.		±10		μA
RECEIVER INPUTS AND OUTPUTS					
Input Voltage Range		-25		25	V
Positive-going input threshold voltage	Vcc = 3.3V		1.7	2.4	V
	Vcc = 5.0V		2.0	2.4	
Negative-going input threshold voltage	Vcc = 3.3V	0.8	1.4		V
	Vcc = 5.0V	0.8	1.7		
Input Hysteresis			0.3		V
High-level output voltage	I_{OH} = -1mA	Vcc -0.6	Vcc – 0.1		V
Low-level output voltage	I_{OL}=+1.6mA			0.4	V
Output Leakage Current	Receivers disabled, EN=GND V_{OUT}=0V to Vcc		±0.1	±25	μA
Input Resistance		3	5	7	kΩ
TIMING CHARACTERISTICS					
TRANSMITTER					
Maximum Data Rate	R_L=3kΩ, C_L=150pF, one transmitter switching		2		Mbps
Transmitter Propagation Delay	t_{DPHL}, TxIN to TxOUT, R_L=3kΩ, C_L=150pF		100		ns
	t_{DPLH}, TxIN to TxOUT, R_L=3kΩ, C_L=150pF		100		
Transmitter Skew	$\lvert t_{DPHL} - t_{DPLH} \rvert$, R_L=3kΩ, C_L=150pF		20		ns
Transition-Region Slew Rate	R_L=3kΩ, C_{LT}=2200pF, One Transmitter Switching, transition		12		V /μs

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	from -3.0V to +3.0V or +3.0V to -3.0V (See Note 1)				
RECEIVER					
Receiver Propagation Delay	t_{RPHL}, RxIN to RxOUT, C_L=150pF		800		ns
	t_{RPLH}, RxIN to RxOUT, C_L=150pF		800		
Receiver Skew	$\lvert t_{RPHL} - t_{RPLH} \rvert$, C_L=150pF		20		ns
Receiver Output Enable Time	t_{PZL}, EN, SDB to RxOUT, C_L=150pF, R_L=3kΩ to Vcc, RxIN=Vcc		35		ns
	t_{PZH}, EN, SDB to RxOUT, C_L=150pF, R_L=3kΩ to GND, RxIN=GND				
Receiver Output Disable Time	t_{PLZ}, EN, SDB to RxOUT, C_L=150pF, R_L=3kΩ to Vcc, RxIN=Vcc		350		ns
	t_{PHZ}, EN, SDB to RxOUT, C_L=150pF, R_L=3kΩ to GND, RxIN=GND				
ESD PROTECTION					
Pin Name (Pin Number)	**Test Condition**				
RxIN(4,9,18,23,27)	IEC61000-4-2 Contact	-8		+8	kV
TxOUT(1,2,3,28)	IEC61000-4-2 Air	-15		+15	kV
All Other Pins	HBM	-2		+2	kV

Note 1:
C_{LT} includes C_{SR} & C_L.
C_{SR} is application circuit for slew-rate (Low-speed).
C_L includes probe and jig capacitance.



Application circuit for note 1

PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Description
1	T3OUT	Third transmitter output
2	T1OUT	First transmitter output
3	T2OUT	Second transmitter output
4	R2IN	Second receiver input
5	R2OUT	Second receiver output
6	T2IN	Second transmitter input
7	T1IN	First transmitter input
8	R1OUT	First receiver output
9	R1IN	First receiver input
10	GND	Ground of the device
11	Vcc	+3.0V to +5.5V supply voltage
12	C1+	Positive terminal of the first switch capacitor
13	V+	Positive voltage of charge pump output
14	C1-	Negative terminal of the first switch capacitor
15	C2+	Positive terminal of the second switch capacitor
16	C2-	Negative terminal of the second switch capacitor
17	V-	Negative voltage of charge pump output
18	R5IN	Fifth receiver input
19	R5OUT	Fifth receiver output
20	T3IN	Third transmitter input
21	T4IN	Fourth transmitter input
22	R4OUT	Fourth receiver output
23	R4IN	Fourth receiver input
24	EN	Receiver Enable. Logic High for normal operation. Logic Low for high impedance output.
25	SDB	Shutdown Input. Active low. With SDB= Low, the charge pump is disabled, the driver outputs are turned off and all receivers except R4 and R5 are placed in a high impedance state.
26	R3OUT	Third receiver output
27	R3IN	Third receiver input
28	T4OUT	Fourth transmitter output

Detail Description

AZRS1496K is a RS-232 transceiver that meets the EIA/TIA-232-F and V.28/V.24 communication protocols. AZRS1496K is a 4-transmitter/5-receiver device with a high-efficient charge pump circuit embedded. The design of high-efficient charge pump circuit is Amazing's property that can generate RS-232 voltage levels from +3.0V to +5.5V power supply. This high-efficient charge pump circuit with 0.1μF capacitors provides the bipolar output to the transmitters, and makes the transmitters deliver the RS-232 output voltage levels. The design of transmitter is also the property of Amazing. Under normal operation and with loaded, AZRS1496K can operate for guaranteed data rate of 2Mbps with ultra low power consumption.
AZRS1496K is also a high reliable device with both latch-up free and high ESD immunity. The high robust ESD devices embedded in AZRS1496K are also the properties of Amazing. All the outputs of transmitters and the inputs of receivers can meet the specifications of IEC 61000-4-2 contact ±8kV, and air ±15kV.

Bipolar Charge Pump Circuit

High-efficient charge pump circuit in AZRS1496K is a four-capacitance structure with single power supply input. Bipolar voltage output of AZRS1496K can be pumped to above ±5.0V under the +3.0V to +5.5V supply power range. Because a negative feedback regulator is embedded, the output voltage is independent of supply power voltage. Moreover, the charge pump can select 2-phase or 4-phase operation for more flexible design. When AZRS1496K is powered on, the bipolar output will be pumped to the steady output with low ripple voltage in the 500μs. Under the shutdown mode, charge pump can be waken up to reach the steady voltage within 100μs.

Transmitter

The design of the transmitter is an inverted translator that converts TTL/CMOS-logic voltage level to EIA/TIA-232-F voltage level. The transmitters of AZRS1496K guarantee a 2Mbps data rate under the loading of 3kΩ resistance in parallel with 150pF capacitance. When the transmitters are active (SDB=HIGH), the input signals of transmitters will be transported to the outputs of transmitters in inverting level.
The inputs of transmitters have 400kΩ pull-up resistors design to ensure the output of transmitter to be a LOW state when the input of transmitter is unconnected.

Receiver

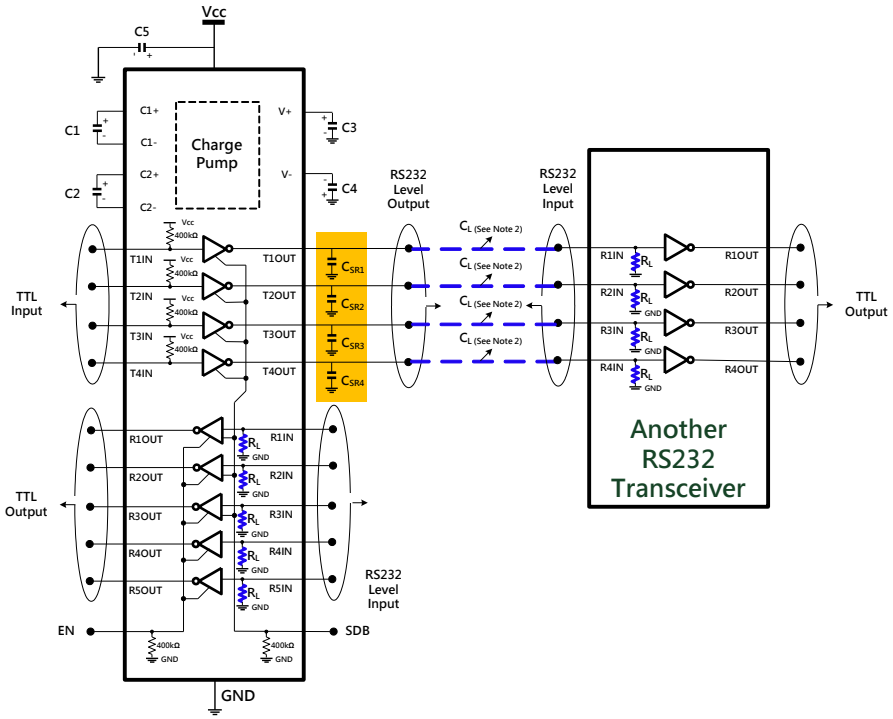
The receivers of AZRS1496K convert EIA/ TIA-232-F voltage levels to TTL/ CMOS-logic voltage levels. The receivers have an inverted tri-state output controlled by EN and SDB. Receivers R4 and R5 remain enabled during shutdown. When EN is LOW, the outputs of receivers R4 and R5 operate in tri-state. When EN is HIGH, the receivers R4 and R5 are active, but R1, R2 and R3 are disabled during shutdown, as listed in the Table1. The EN pin only controls the outputs of all receivers and has no any effect on the outputs of transmitters. Moreover, the SDB controls not only the transmitters but also the charge pump and receivers R1, R2 and R3.
The receiver guarantees a 2Mbps data rate under the loading of a 150pF.
The inputs of receivers have 5kΩ pull-down resistors design to ensure the output of receiver to be a HIGH state when the input of receiver is unconnected.

Application Information

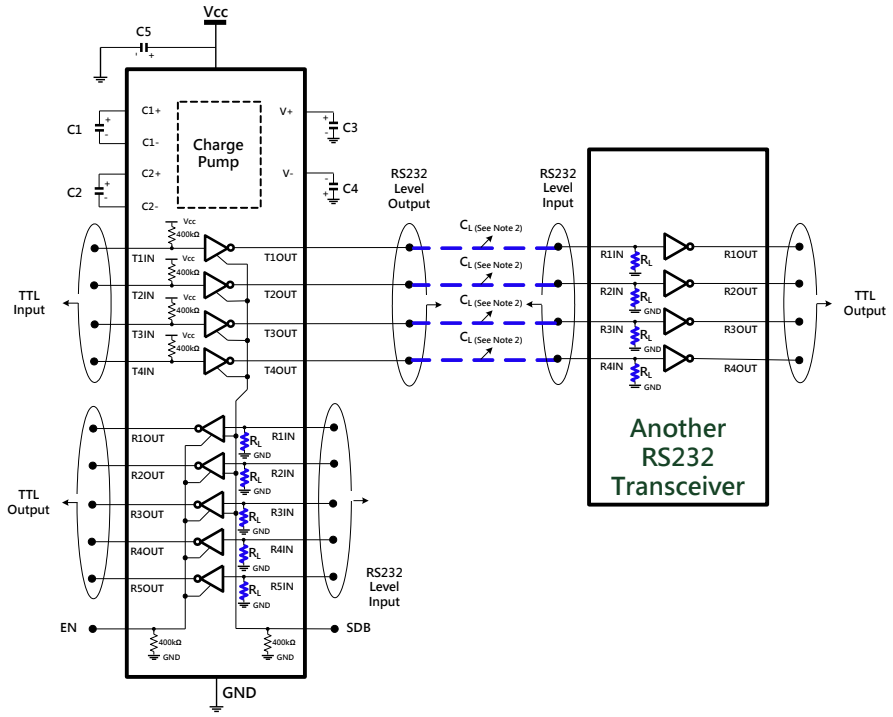
To generate the high-efficient bipolar charge pump, the four capacitors (C1 ~ C4) must be placed as closer to RS232 transceiver as possible. The trace of the PCB layout is suggested to be shorter than 1cm from the pinout of the charge pump to the dedicated capacitor. The other node of dedicated capacitor should be connected to ground shortly, too. Moreover, the capacitor of power supply (C5) should be placed as close to the transceiver as possible, and connect to ground nearby.

If Slew-rate (Low speed) is required, it can be connected to the application circuit: C_{SR1}, C_{SR2}, C_{SR3} & C_{SR4} are connected to T1OUT, T2OUT, T3OUT & T4OUT (Recommended value of C_{SR1}, C_{SR2}, C_{SR3} & C_{SR4} = 2200pF)

In other applications, C3 could be changed to connect to Vcc.

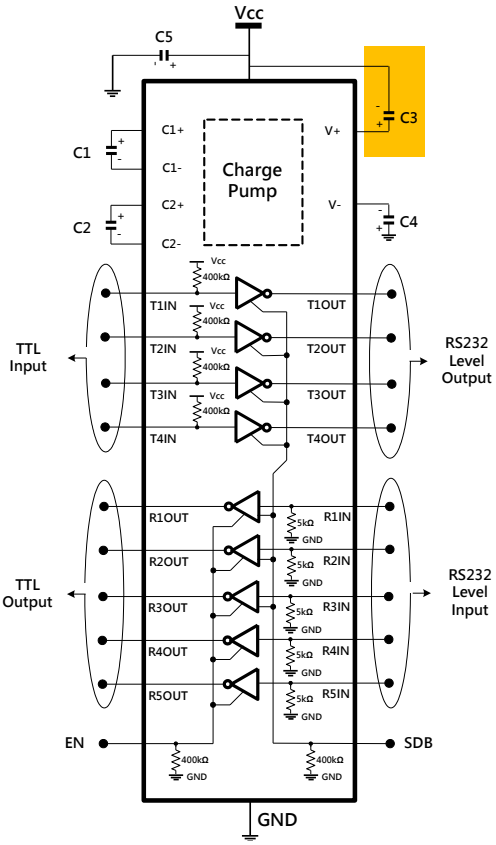


Operation of AZRS1496K for Slew-rate (Low-speed)



Operation of AZRS1496K (High-speed)

Note 2:
C_L includes probe and jig capacitance



Application circuit for note 3

Note 3:
C3 could be changed to connect to Vcc

Table 1 Function Table of SDB and EN Control

INPUTS		TRANSMITTER	RECEIVER		STATUS
SDB	EN	T1-T4	R1-R3	R4-R5	
L	L	Z	Z	Z	Shutdown
L	H	Z	Z	Active	Shutdown
H	L	Active	Z	Z	Active
H	H	Active	Active	Active	Active

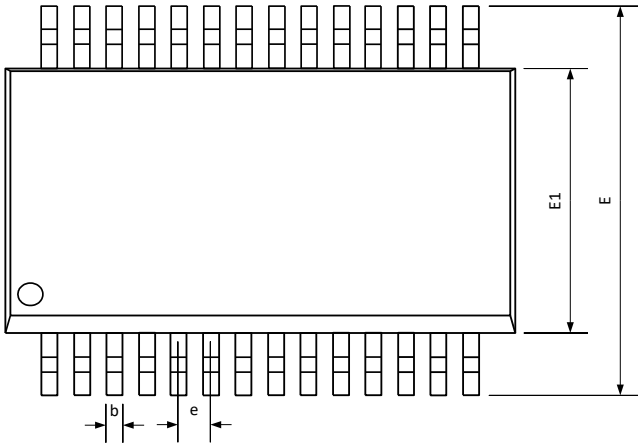
H = High level, L = Low level, X = Irrelevant, Z = High impedance.

Mechanical Details

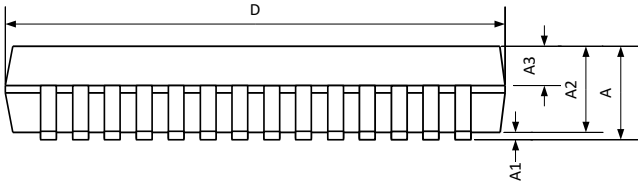
SSOP-28L(209)

PACKAGE DIAGRAMS

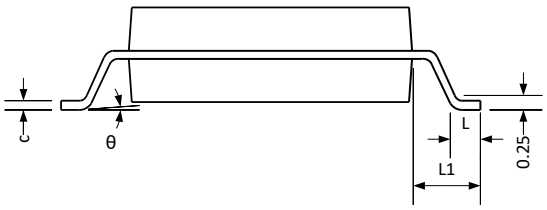
TOP VIEW



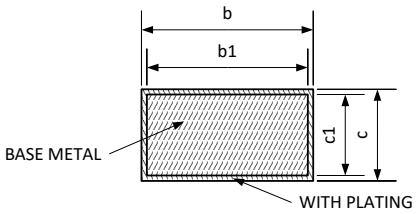
SIDE VIEW



END VIEW1



END VIEW2



PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.15	-	0.19
c1	0.14	0.15	0.16
D	10.10	10.20	10.30
E	7.60	7.80	8.00
E1	5.20	5.30	5.40
e	0.65BSC		
L	0.75	-	1.05
L1	1.25REF		
θ	0	-	8°

Marking Code

AR1496K = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZRS1496K.RDG (Green part)	AR1496K WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZRS1496K.RDG	Green	T/R	13 inch	2,000/reel	1 reel =2,000/box	5 boxes = 10,000/carton

Revision History

Revision	Modification Description
Revision 2024/04/01	Formal Release.
Revision 2024/09/23	Add Application information