Features

- ***Polarity Free for RS485 bus pins***
- Integrated TVS Protection for Bus Terminals :
  ±15 kV IEC 61000-4-2, Contact Discharge
  ±20 kV IEC 61000-4-2, Air-Gap Discharge
- HBM ±8kV ESD Protection for all pins
- MM ±800V ESD Protection for all pins
- Meet the Requirements of the EIA/TIA-485 Standards with 5V Power Supply
- True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility
- Data Rate up to 10Mbps
  Hot-Swap Glitch free Protection on Control Inputs
- High driving ability of VOD2 up to 2.3V
- Up to 256 Transceivers on the Bus

Applications

- Energy Meter Networks
- Industrial Control
- Telecommunications Equipment
- Security System
- Building Automation Networks

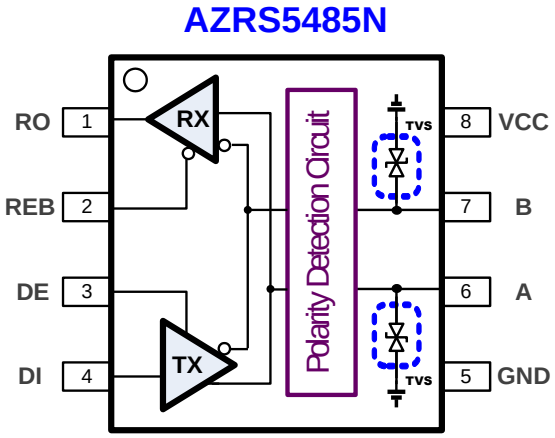
Description

The AZRS5485N is a **Polarity-Free** half-duplex RS485 transceiver IC with ±15kV IEC 61000-4-2 contact discharge protection. This device is fully compliant with the EIA/TIA-485 standard with 5V power supply. The Parity-Free AZRS5485N can automatically detect the polarity for A and B pins when pull-high for A and “pull-low” for B have been designed on the RS485 bus. The polarity detection function will be enabled when the AZRS5485N has been power up to 5V.

The detection function is real-time monitored the bus polarity without any data flow on the RS485 bus. AZRS5485N is slave-type RS485 to feature the Polarity Free function, which can not design the pull-up and pull-down resistor on the slave device.

AZRS5485N features an advanced fail-safe receiver, which combined the true fail-safe and Polarity Free function to guarantees the output of the receiver to be logic high when the differential inputs (bus pins, A and B) of the receiver are open, short, idle, and even inverting connection.

AZRS5485N features a hot-swap glitch-free function which guarantees outputs of both the transmitter and the receiver in a high impedance state so as to prevent short current event during the power up period. AZRS5485N has the thermal shutdown and the current limited function in the transmitter to protect the device from damage by system fault conditions during normal operating condition. AZRS5485N is designed 1/8 unit load with minimum 96kohm of input impedance, which can connect 256 devices on a bus at least.



Functional Block of AZRS5485N

Part Number	Duplex	Tx/Rx	Supply	Data Rate (Mbps)	HBM/MM	IEC 61000-4-2 Contact on A,B	Special Function	Package Type
AZRS5485N	Half	1/1	5V	10	±8kV/800V	± 15kV	Polarity Free	SO-8

ABSOLUTE MAXIMUM RATINGS

PARAMETER	PARAMETER	RATING	UNITS
Power Supply Vcc	Vcc	-0.3 to 8.0	V
Control Input Voltage	REB, DE	-0.3 to (Vcc+ 0.3)	V
Receiver Input Voltage	A, B	±13	V
Receiver Output Voltage	RO	-0.3 to (Vcc+ 0.3)	V
Transmitter Output Voltage	A, B	±13	V
Transmitter Input	DI	-0.3 to (Vcc+ 0.3)	V
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STO}	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

(Vcc=5V ±10% with T_{AMB}= T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at Vcc=5V and T_{AMB}= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transmitter							
Differential Transmitter Output	V_{OD1}	No load				Vcc	V
Differential Transmitter Output	V_{OD2}	Fig.1, R_L= 27Ω		1.5	2.3	5.0	V
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Fig.1, R_L= 27Ω				0.2	V
Transmitter Common- Mode Output Voltage	V_{OC}	Fig.1, R_L= 27Ω		1.0		3.0	V
Change in Magnitude of Common- Mode Voltage	ΔV_{OC}	Fig.1, R_L= 27Ω				0.2	V
Input High Voltage	V_{IH}	DE, DI, REB		2.0			V
Input Low Voltage	V_{IL}	DE, DI, REB				0.8	V
Input Current	I_{IN1}	DE, DI, REB				±2	μA
Input Current for A and B	I_{IN2}	DE=0V, Vcc=0V or 5.5V	V_{IN}=12V			125	μA
			V_{IN}=-7V	-100			
Transmitter Short-Circuit Output Current	I_{OSD}	A Pin Short to B Pin		-150		150	mA
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}			-100		+100	mV
Receiver Input Hysteresis	ΔV_{TH}				20		mV
Receiver Output High Voltage	V_{OH}	Io= -4mA, VID= 200mV		4.0			V
Receiver Output Low Voltage	V_{OL}	Io= 4mA, VID= -200mV				0.4	V
Three- State Output Current	I_{OZR}	0.4V ≤ V_{CM} ≤ 2.4V				±1	μA

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER							
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	Fig. 6, 0V ≤ V_{RO} ≤ Vcc		±7		±95	m A
SUPPLY CURRENT							
Supply Current	Icc	No load, REB= GND, DI= Vcc or GND.	DE= Vcc		500	800	μA
			DE= GND		400	800	μA

SWITCHING CHARACTERISTICS

(Vcc=5V ±10% with T_{AMB}= T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at Vcc=5V and T_{AMB}= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Input to Output	t_{DPLH}, t_{DPHL}	Fig.2 and 7, R_{DIFF}=54Ω, C_{L1}=C_{L2}= 100pF	5	8	15	ns
Transmitter Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	Fig.2, Fig.7, R_{DIFF}=54Ω, C_{L1}=C_{L2}= 100pF		5	10	ns
Transmitter Rise or Fall Time	t_{DF}, t_{DR}	Fig.2, Fig.7, R_{DIFF}=54Ω, C_{L1}=C_{L2}= 100pF		7		ns
Data Rate	f_{Data}				10	Mbps
Transmitter Enable to Output Low	t_{DZL}	Fig.4, Fig.8, C_{DL}= 100pF, S1 closed			70	ns
Transmitter Enable to Output High	t_{DZH}	Fig.4, Fig.8, C_{DL}= 100pF, S2 closed			70	ns
Transmitter Disable Time from Low	t_{DLZ}	Fig.4, Fig.8, C_{DL}= 15pF, S1 closed			70	ns
Transmitter Disable Time from High	t_{DHZ}	Fig.4, Fig.8, C_{DL}= 15pF, S2 closed			70	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Fig.5, Fig.9, $\lvert V_{ID} \rvert$ ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns	20	105	150	ns
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Different Receiver Skew	t_{RSKD}	Fig.5, Fig.9, $\lvert V_{ID} \rvert$ ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		6		ns
Receiver Enable to Output Low	t_{RZL}	Fig.3, Fig.10, C_{RL}= 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Fig.3, Fig.10, C_{RL}= 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Fig.3, Fig.10, C_{RL}= 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Fig.3, Fig.10, C_{RL}= 15pF, S2 closed		20	50	ns

PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	RO	Receiver Output: When REB is low and if (A - B) ≥ +100mV, RO is high; if (A - B) ≤ -100mV, RO is low.
2	REB	Receiver Output Enable: REB is low to enable the Receiver; REB is high to disable the Receiver.
3	DE	Transmitter Output Enable: DE is high to enable the transmitter; DE is low to disable the transceiver.
4	DI	Transmitter Input: When DE is high, a low on DI forces A output low and B output high. Similarly, a high on DI forces A output high and B output low.
5	GND	Ground pin. Must be connected to 0V.
6	A	Non-inverting Receiver Input and Non-inverting Transmitter Output **(Polarity Free design inside)**
7	B	Inverting Receiver Input and Inverting Transmitter Output **(Polarity Free design inside)**
8	VCC	Power Supply Input 5V.

FUNCTION TABLE

TRANSMITTING				
INPUTS			**OUTPUTS**	
REB	DE	DI	A	B
X	1	0	0	1
X	1	1	1	0
X	0	X	HIGH- Z	HIGH- Z

X= Don't care
HIGH- Z= High impedance

RECEIVING			
INPUTS			**OUTPUTS**
REB	DE	A - B	RO
0	0	≥ +0.1V	1
0	0	≤ –0.1V	0*[1]
0	0	Open/Shorted	1
1	0	X	HIGH- Z

X= Don't care
HIGH- Z= High impedance
***1 Within Polarity-Free Detection Time**

Detail Description

The AZRS5485N is a half-duplex RS-485 transceiver IC with IEC61000-4-2 contact ±15kV ESD protection for bus pins (A and B), which contains one transmitter and one receiver inside with 5V power supply. This device is fully compliant with the EIA/TIA-485 standard.

The AZRS5485N features the hot-swap glitch free design which guarantees the outputs of the transceiver in a high impedance state during the power-up period until the supply voltage has stabilized.

The AZRS5485N with whole chip ESD protected design for all of the I/O pins has robust ESD protection up to both HBM ±8kV and MM ±800V. Moreover, the latchup immunity of the AZRS5485N is up to ±400mA for all of the pins. For IC self discharge issue, the CDM protection level of the AZRS5485N is up to ±1kV.

Transmitter

The design of the transmitter is a non-inverted translator that converts the single-ended TTL input signal to differential EIA/TIA-485 signal level. The transmitter of the AZRS5485N guarantees 10Mbps data rate communication. When the transmitter is active (DE= HIGH), the single-end TTL input signals of transmitter will be transported to differential output RS485 signals of the transmitter. Under the disable state (DE= LOW), the outputs of transmitter keep at high impedance state.

The differential output voltage (VA-VB) of the AZRS5485N is 2.3V with 54 ohm load under T= 25^{o}C.

Receiver

The receiver of the AZRS5485N converts the differential EIA/TIA-485 signals to single-end output TTL signal when receiver is in active state (REB=LOW), which incorporates input filtering in addition to input hysteresis. The input filtering enhances the noise immunity under normal operating condition. When the receiver is disable (REB=HIGH), the output of the receiver keeps in high impedance state no matter what the input of the receiver is.

Advanced Fail-Safe

In traditional design, the fail-safe function is implemented by two resistors on the PCB. One resistor is terminated pin A to VCC; the other is terminated pin B to GND to keep RO at high state when bus is idle, which is only the open fail-safe.

The AZRS5485N guarantees a receiver output high when the receiver inputs are short, open or idle, that is true fail-safe. The threshold voltage of receiver input is between -100mV and +100mV. If the differential input voltage (A - B) of receiver is greater than or equal to +100mV, receiver output (RO) is logic-high. If (A - B) is less than or equal to -100mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage (A - B) is 0V, so the RO is logic-high at that time.

1/8 Unit Load

The RS-485 standard defines both receiver inputs impedance are 12kΩ (1 unit load) and the maximum 32-unit loads on the bus. The AZRS5485N transceiver has a 96kΩ input impedance (1/8 unit load) of the receiver, allowing up to 256 or fewer devices to be connected in parallel on the RS485 bus.

Transmitter Output Protection

The AZRS5485N has the current limitation function and the thermal shutdown protection in the transmitter. Firstly, the function of current limitation provides immediate protection against short circuits over the whole common-mode voltage range (-7V to +12V). Secondly, the function of thermal shutdown protection forces the transmitter outputs into a high impedance state if the die temperature becomes excessive.

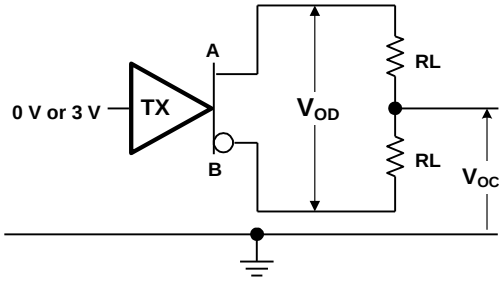


Fig.1 Transmitter DC test circuit

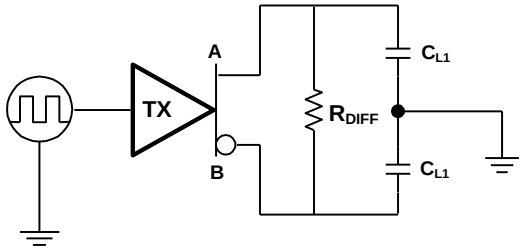


Fig.2 Transmitter timing test circuit

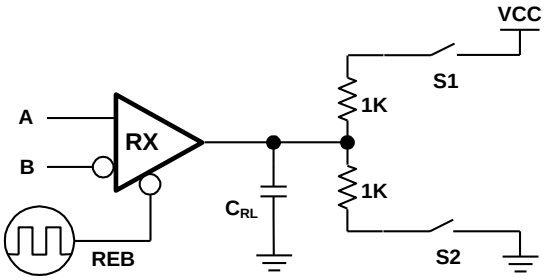


Fig.3 Receiver enable/disable timing test load

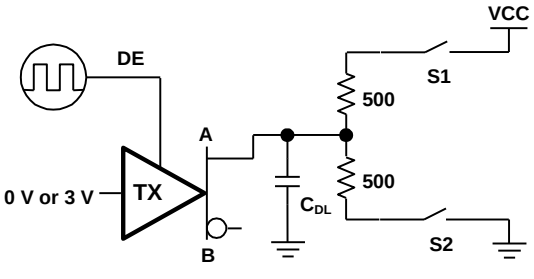


Fig.4 Transmitter enable/disable timing test load

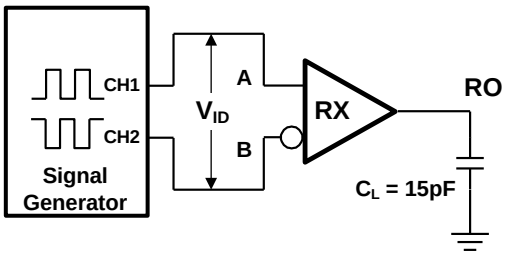


Fig.5 Receiver timing test circuit

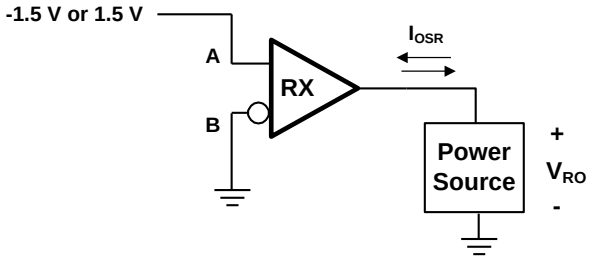


Fig.6 Receiver output short circuit

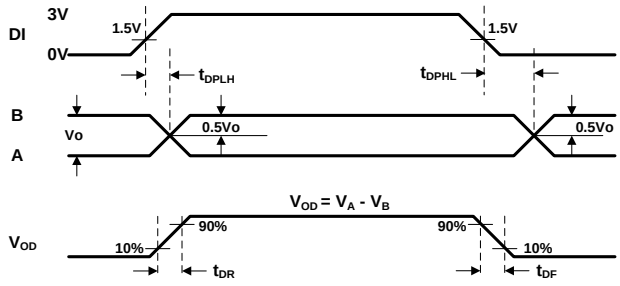


Fig.7 Transmitter Propagation Delays

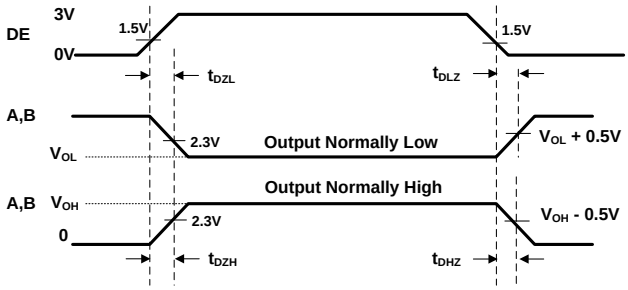


Fig.8 Transmitter Enable and Disable Times

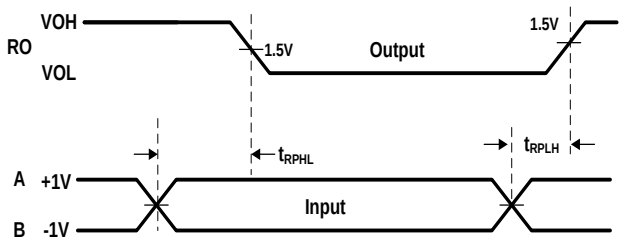


Fig.9 Receiver Propagation Delays

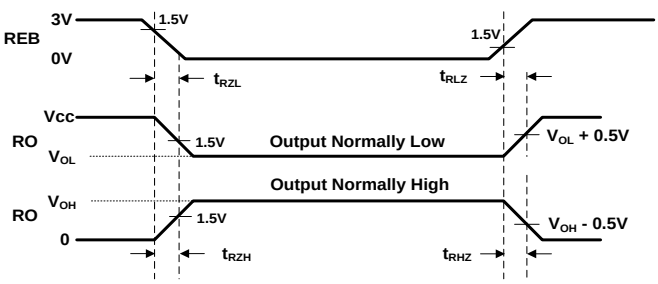


Fig.10 Receiver Enable and Disable Times

SWITCHING CHARACTERISTICS for POLARITY FREE

(Vcc=5V ±10% with T_{AMB}= T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at Vcc=5V and T_{AMB}= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Detection Time for Polarity Free	t_{DPF}	S1, S3 : ON ; S2, S4 : OFF S2, S4 : ON ; S1, S3 : OFF Fig. 11 and Fig. 12	10	60	150	ms

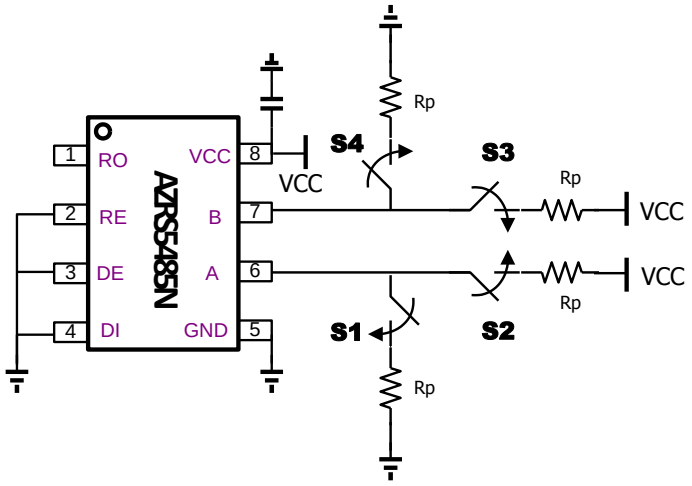


Fig. 11 Detection Time for Polarity Free testing circuit

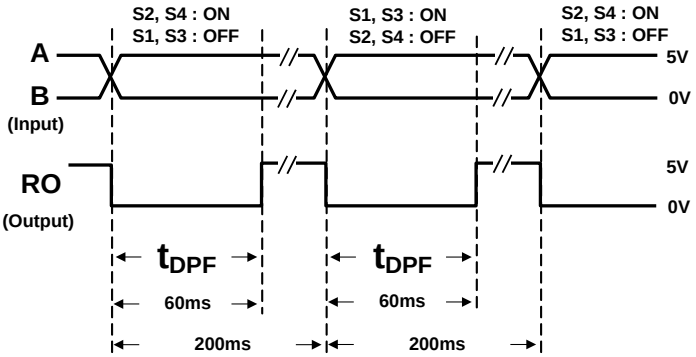


Fig. 12 Input and Output timing for detection time for polarity time

The detection time for polarity is about 60ms when no dataflow on the bus. AZRS5485N detects the polarity real-time after power-on.

Application Circuit for Slave-Side Device (Polarity Free)

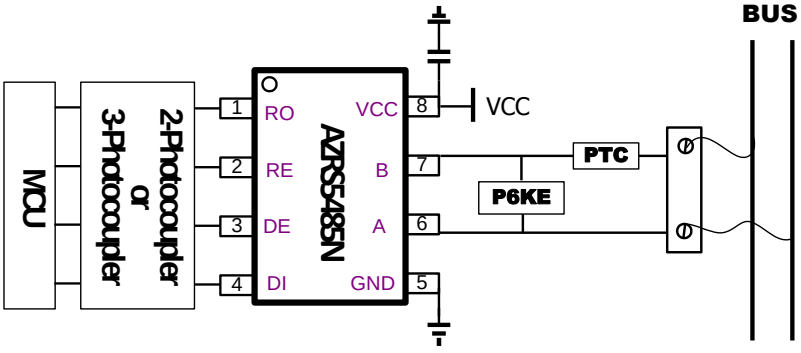


Fig. 13 AZRS5485N on the slave-side can not design the pull-up and pull-down resistor to form the polarity free function.

Application Circuit for Master-Side Device (Define Polarity)

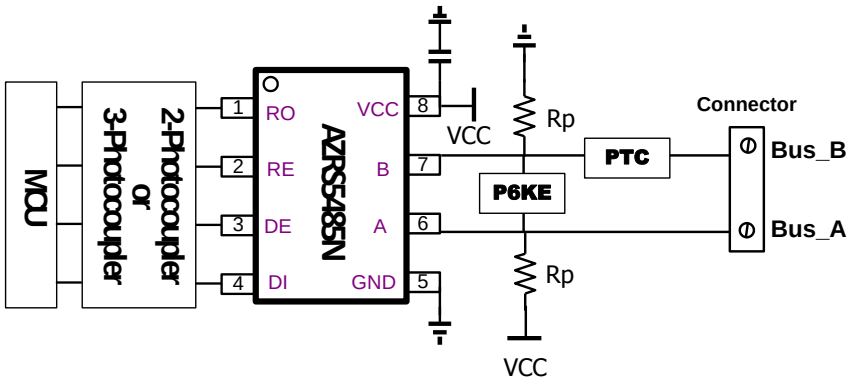


Fig. 14 AZRS5485N on the master-side to define which is Bus_A and Bus_B by pull-up and pull-down resistor, Rp.

The polarity free function of the AZRS5485N on the slave-side will be enable when the RS485 is under DE=REB=0V. Moreover, the pull-up and pull-down resistor, Rp, must not be designed on the device to define which is A or B, as show in Fig. 13. Once the polarity free conditions are ready, the operator can tie any pin to the bus. It is not necessary to know “which is A or B”.

On the master-side design, the pull-up and pull-down resistors are necessary to define A or B on the RS485 bus. The pull-up resistor defines pin A to tie to Vcc and the pull-down resistor defines pin B to tie to GND. The master device defines the polarity for bus, which is BUS_A and BUS_B, as shown in Fig.14.

AZRS5485N can communicate with MCU through either 2-photocoupler or 3-photocoupler base.

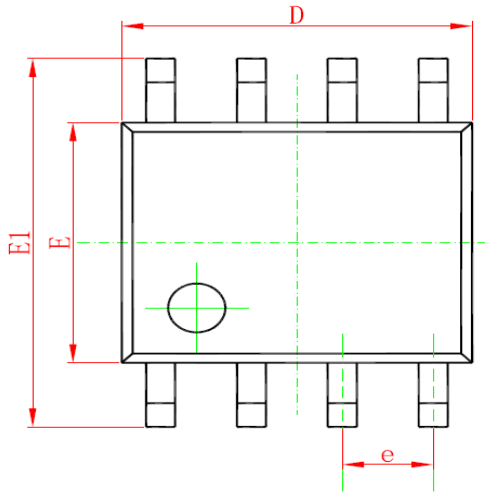
The best design for Rp on master device is 680 ohm for 2-photocoupler topology to connect below 50 slave devices. To connect more than 100 slave devices, the resistance of the Rp should be reduced to 200 ohm, for example, which depends on the parasitic effect for the bus condition.

Mechanical Details

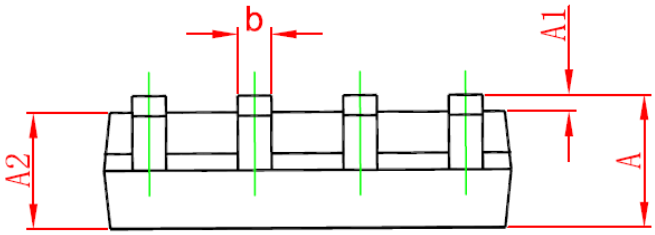
SO-8

PACKAGE DIAGRAMS

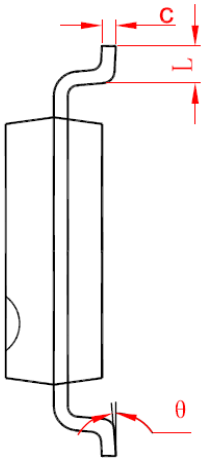
TOP VIEW



SIDE VIEW



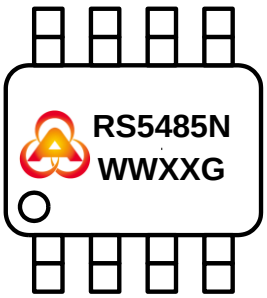
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.053	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

MARKING CODE



RS5485N = Device Code
WW = Date Code
XX = Control Code
G = Green Part Indication

Part Number	Marking Code
AZRS5485N.RDG	RS5485N WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZRS5485N.RDG	Green	T/R	13 inch	1 reel=2,500/box	5 box=12,500/carton

Revision History

Revision	Modification Description
Revision 2016/07/07	Formal Release.
Revision 2017/02/15	Adds logo and modifies Part Number at Marking Information