

# AZV99

## PECL/LVDS Oscillator Gain Stage & Buffer with Selectable Enable

### FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Packages Available
- Similar Operation as AZ100LVEL16VT except with **LVDS Outputs**
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a 2x2 or 3x3mm MLP Package
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website

### PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2x0.75) Green / RoHS Compliant / Lead (Pb) Free	AZV99NG	V1G <Date Code>	1,2
MLP 8 (2x2x0.75)	AZV99NA	V9 <Date Code>	1,2
MLP 8 (2x2x0.75) Green / RoHS Compliant / Lead (Pb) Free	AZV99NBG	V8G <Date Code>	1,2
MLP 8 (2x2x0.75) Green / RoHS Compliant / Lead (Pb) Free	AZV99NDG	V2G <Date Code>	1,2
MLP 16 (3x3) Green / RoHS Compliant / Lead (Pb) Free	AZV99LG	AZMG V99 <Date Code>	1,2
TSSOP 8 RoHS Compliant / Lead (Pb) Free	AZV99T+	AZ+ V99	1,2,3
DIE	AZV99XP	N/A	4

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.

2 Date code format: "Y" for year followed by "WW" for week.

3 Date Code "YWW" on underside of part.

4 Waffle Pack

### DESCRIPTION

The AZV99 is a specialized oscillator gain stage with LVDS output buffer including an enable. The enable input (EN) allows continuous oscillator operation by only controlling the  $Q_{HG}/\bar{Q}_{HG}$  outputs.

The AZV99 also provides a  $V_{BB}$  and 470 $\Omega$  internal bias resistors from D to  $V_{BB}$  and  $\bar{D}$  to  $V_{BB}$ . The  $V_{BB}$  pin can support 1.5 mA sink/source current. Bypassing  $V_{BB}$  to ground with a 0.01  $\mu$ F capacitor is recommended.

#### MLP 16, 3x3 mm Package (L) or DIE (X)

The MLP 16 and die versions of the AZV99 provide a selectable enable (EN). Enable polarity and threshold can be selected to accommodate either CMOS/TTL or PECL input levels. See the enable truth table for enable function. If enable pull-up is desired in the CMOS/TTL mode, an external  $\leq 20k\Omega$  resistor connecting EN to  $V_{CC}$  will override the on-chip pull-down resistor.

Outputs  $Q/\bar{Q}$  each have a selectable on-chip pull-down current source. See the current source truth table for current source functions. External resistors may also be used to increase pull-down current to a maximum of 25mA (includes internal on-chip current source).

# AZV99

## MLP 8, 2x2 mm Package, NA, NB & ND Options

The MLP 8 NA, NB and ND options of the AZV99 provide a PECL/ECL level enable input ( $\overline{EN}$ ). When the  $\overline{EN}$  input is LOW, the  $\overline{Q}$  and  $Q_{HG}/\overline{Q}_{HG}$  outputs pass data from the inputs. When  $\overline{EN}$  is HIGH, the  $\overline{Q}$  output continues to pass data while the  $Q_{HG}$  output is forced high and the  $\overline{Q}_{HG}$  output is forced low.

Only the  $\overline{Q}$  output operates with a current source (4 mA) to  $V_{EE}$ . This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

The AZV99NB and AZV99ND versions operates with a single ended data input (D). The  $\overline{D}$  input is internally bonded directly to the  $V_{BB}$  pin bypassing the 470 $\Omega$  bias resistor.

## TSSOP 8 Package (T), MLP 8 Package, (N)

The TSSOP 8 (T) and MLP 8 (N) versions of the AZV99 provide a CMOS/TTL level enable input (EN). When the EN input is HIGH, the  $\overline{Q}$  and  $Q_{HG}/\overline{Q}_{HG}$  outputs pass data from the inputs. When EN is LOW, the  $\overline{Q}$  output continues to pass data while the  $Q_{HG}$  output is forced high and the  $\overline{Q}_{HG}$  output is forced low.

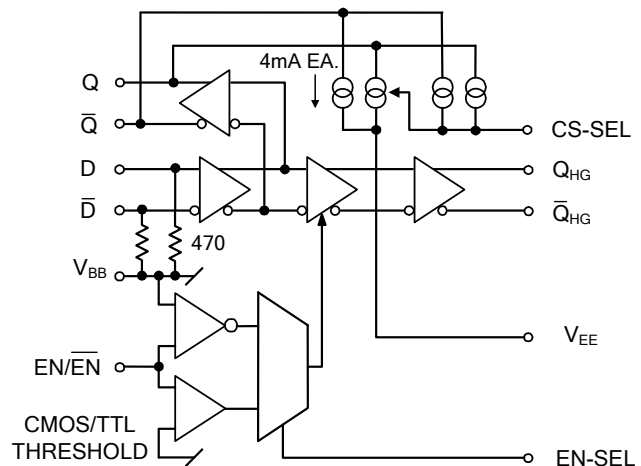
Only the  $\overline{Q}$  output operates with a current source (4 mA) to  $V_{EE}$ . This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

The TSSOP 8 (T) and MLP 8 (N) AZV99 operates with a single ended data input (D). The  $\overline{D}$  input is internally bonded directly to the  $V_{BB}$  pin bypassing the 470 $\Omega$  bias resistor.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

### PIN DESCRIPTION

PIN	FUNCTION
D/ $\overline{D}$	Data Inputs
Q/ $\overline{Q}$	PECL Data Outputs
$Q_{HG}/\overline{Q}_{HG}$	LVDS Data Outputs
$V_{BB}$	Reference Voltage Output
EN-SEL	Selects Enable Logic
EN/ $\overline{EN}$	Enable Input
CS-SEL	Selects Q and $\overline{Q}$ Current Source Magnitude
$V_{EE}$	Negative Supply
$V_{CC}$	Positive Supply



### ENABLE TRUTH TABLE

EN-SEL	EN/ $\overline{EN}$	Q/ $\overline{Q}$	$Q_{HG}$	$\overline{Q}_{HG}$
NC	PECL Low or NC	Data	Data	Data
NC	PECL High or $V_{CC}$	Data	High	Low
$V_{EE}$ <sup>1</sup>	CMOS/TTL Low, $V_{EE}$ or NC	Data	High	Low
$V_{EE}$ <sup>1</sup>	CMOS/TTL High or $V_{CC}$ <sup>2</sup>	Data	Data	Data

<sup>1</sup> EN-SEL connections must be less than 1 $\Omega$ .

<sup>2</sup> An external  $\leq 20k\Omega$  pull-up resistor between EN and  $V_{CC}$  ensures a High when the EN pin is not driven.

### CURRENT SOURCE TRUTH TABLE

CS-SEL	Q	$\overline{Q}$
NC	4mA typ.	4mA typ.
$V_{EE}$ <sup>1</sup>	8mA typ.	8mA typ.
$V_{CC}$ <sup>1</sup>	0	4mA typ.

<sup>1</sup> CS-SEL connections must be less than 1 $\Omega$ .

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
V <sub>CC</sub>	Power Supply	0 to +6.0	Vdc
V <sub>I</sub>	Input Voltage	0 to +6.0	Vdc
V <sub>D/D</sub>	D/ $\bar{D}$ Input Voltage	$\pm 0.75$ with respect to V <sub>BB</sub>	Vdc
I <sub>OUT</sub>	Output Current — Continuous Q/ $\bar{Q}$	25	mA
	— Surge Q/ $\bar{Q}$	50	
	— Continuous Q <sub>HG</sub> / $\bar{Q}$ <sub>HG</sub>	5	
	— Surge Q <sub>HG</sub> / $\bar{Q}$ <sub>HG</sub>	10	
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

**100K LVPECL DC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.3V)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1,2</sup> Q/ $\bar{Q}$	2255	2465	2275	2465	2275	2465	2275	2465	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1,2</sup> Q/ $\bar{Q}$	1375	1745	1400	1680	1400	1680	1400	1680	mV
V <sub>IH</sub>	Input HIGH Voltage									
	D/ $\bar{D}$ <sup>1</sup> , EN (EN-SEL open) <sup>1</sup> EN (EN-SEL tied to V <sub>EE</sub> )	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	2135 2000	2560 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage									
	D/ $\bar{D}$ <sup>1</sup> , EN (EN-SEL open) <sup>1</sup> EN (EN-SEL tied to V <sub>EE</sub> )	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	mV
V <sub>BB</sub>	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
I <sub>IL</sub>	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		μA
I <sub>IH</sub>	Input HIGH Current EN <sup>3</sup>		150		150		150		150	μA
I <sub>EE</sub>	Power Supply Current <sup>2</sup>		48		48		48		52	mA

1. Voltage levels vary 1:1 with V<sub>CC</sub>.
2. Specified with CS-SEL open.
3. Specified with EN-SEL open.

**100K PECL DC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +5.0V)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1,2</sup> Q/ $\bar{Q}$	3955	4165	3975	4165	3975	4165	3975	4165	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1,2</sup> Q/ $\bar{Q}$	3075	3445	3100	3380	3100	3380	3100	3380	mV
V <sub>IH</sub>	Input HIGH Voltage									
	D/ $\bar{D}$ <sup>1</sup> , EN (EN-SEL open) <sup>1</sup> EN (EN-SEL tied to V <sub>EE</sub> )	3835 2000	4260 V <sub>CC</sub>	3835 2000	4260 V <sub>CC</sub>	3835 2000	4260 V <sub>CC</sub>	3835 2000	4260 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage									
	D/ $\bar{D}$ <sup>1</sup> , EN (EN-SEL open) <sup>1</sup> EN (EN-SEL tied to V <sub>EE</sub> )	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	mV
V <sub>BB</sub>	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
I <sub>IL</sub>	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		μA
I <sub>IH</sub>	Input HIGH Current EN <sup>3</sup>		150		150		150		150	μA
I <sub>EE</sub>	Power Supply Current <sup>2</sup>		48		48		48		52	mA

1. Voltage levels vary 1:1 with V<sub>CC</sub>.
2. Specified with CS-SEL open.
3. Specified with EN-SEL open.

**LVDS DC Characteristics for Q<sub>HG</sub>/Q̄<sub>HG</sub> Outputs<sup>1</sup> (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.0V to +5.5V)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage		1600		1600		1600		1600	mV
V <sub>OL</sub>	Output LOW Voltage	900		900		900		900		mV
V <sub>OC</sub>	Output Common Mode Voltage <sup>2</sup>	1125	1375	1125	1375	1125	1375	1125	1375	mV
ΔV <sub>OC</sub>	Change in Common Mode Voltage <sup>3</sup>	-50	50	-50	50	-50	50	-50	50	mV
V <sub>OUT</sub>	Single-Ended Output Swing	250	450	250	450	250	450	250	450	mV
V <sub>DIFF_OUT</sub>	Differential Output Swing	500	900	500	900	500	900	500	900	mV

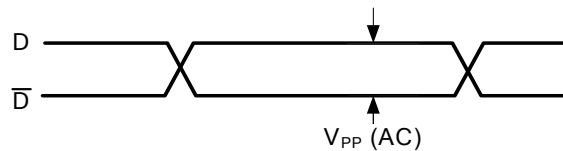
1. Specified with 100Ω resistor connecting Q<sub>HG</sub> and Q̄<sub>HG</sub> together.
2. Common mode voltage is the center voltage between Q<sub>HG</sub> and Q̄<sub>HG</sub> during a steady state.
3. Change in common mode voltage is the difference between common mode voltages at opposite binary states.

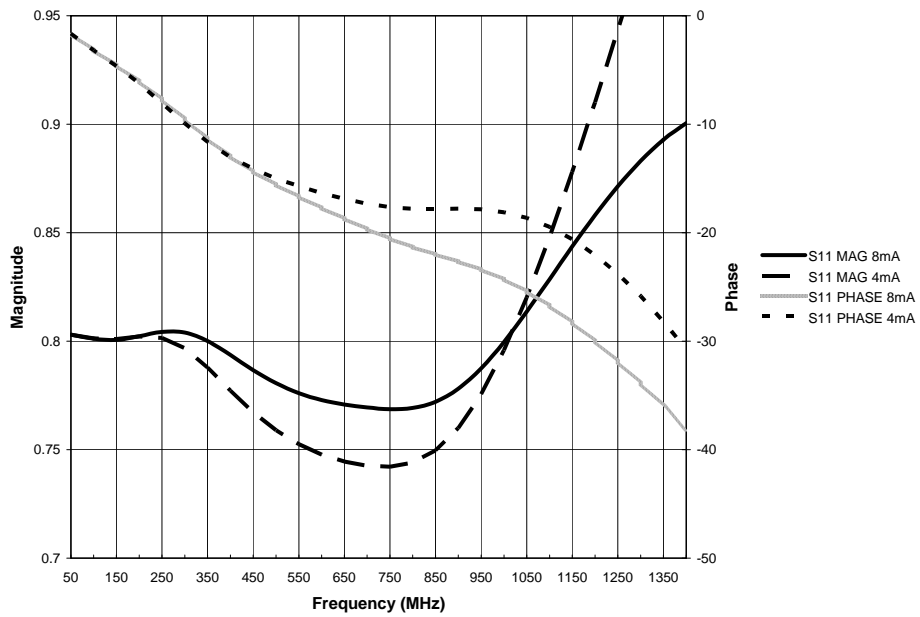
**AC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.0V to +5.5V)**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t <sub>PLH</sub> / t <sub>PHL</sub>	Propagation Delay D to Q/Q̄ Outputs <sup>1</sup> (SE)			400			400			400			430	ps
	D to Q <sub>HG</sub> /Q̄ <sub>HG</sub> Outputs <sup>2</sup> (SE)			550			550			550			630	
t <sub>SKEW</sub>	Duty Cycle Skew Q/Q̄ <sup>3</sup> (SE)		5	20		5	20		5	20		5	20	ps
V <sub>PP</sub> (AC)	Differential Input Swing <sup>4</sup>	80		1000	80		1000	80		1000	80		1000	mV
t <sub>r</sub> / t <sub>f</sub>	Output Rise/Fall Times (20% - 80%)			260			260			260			260	ps
	Q/Q̄ <sup>1</sup> Q <sub>HG</sub> /Q̄ <sub>HG</sub> <sup>2</sup>	100		180	100		180	100		180	100		180	

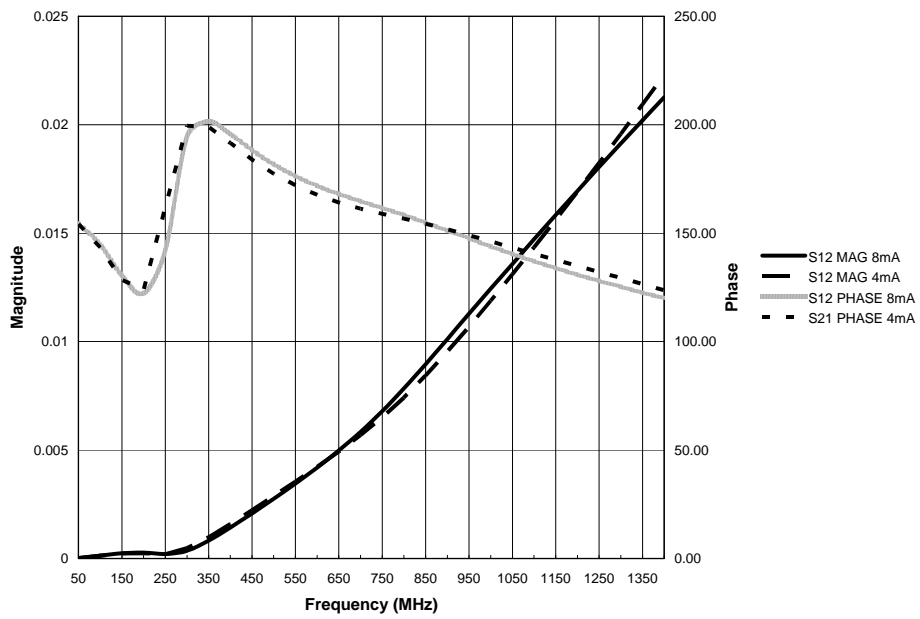
1. Specified with CS-SEL connected to V<sub>EE</sub> and Q/Q̄ with AC coupled 50Ω loads.
2. Specified with 100Ω resistor connecting Q<sub>HG</sub> and Q̄<sub>HG</sub> together.
3. Duty cycle skew is the difference between a t<sub>PLH</sub> and t<sub>PHL</sub> propagation delay through a device.
4. The peak-to-peak differential input swing is the range for which AC parameters guaranteed. V<sub>D</sub> and V<sub>D</sub> must remain within the range of ±750 mV with respect to V<sub>BB</sub>.

**AC PP INPUT**

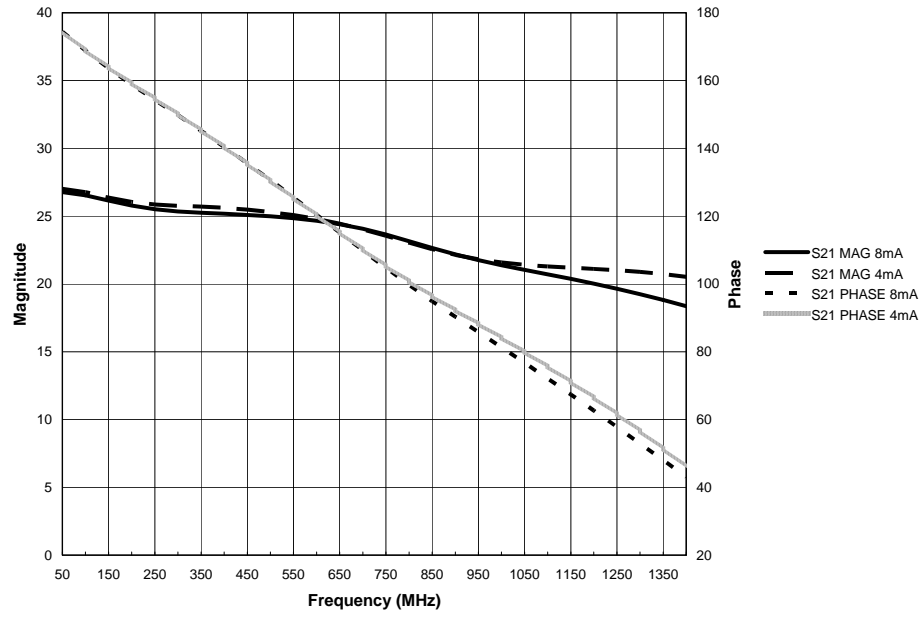




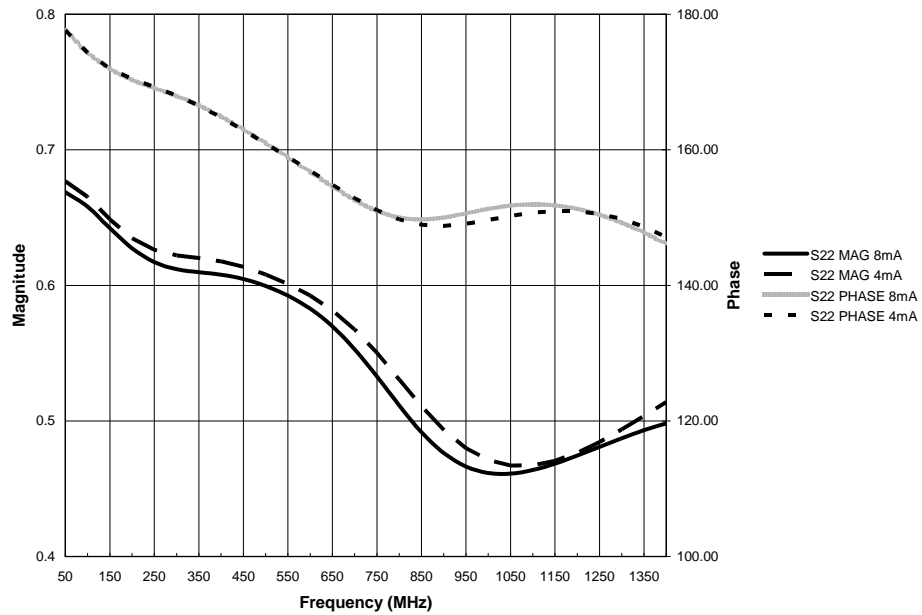
**S11, D to Q, 50 Ω AC load on Q**



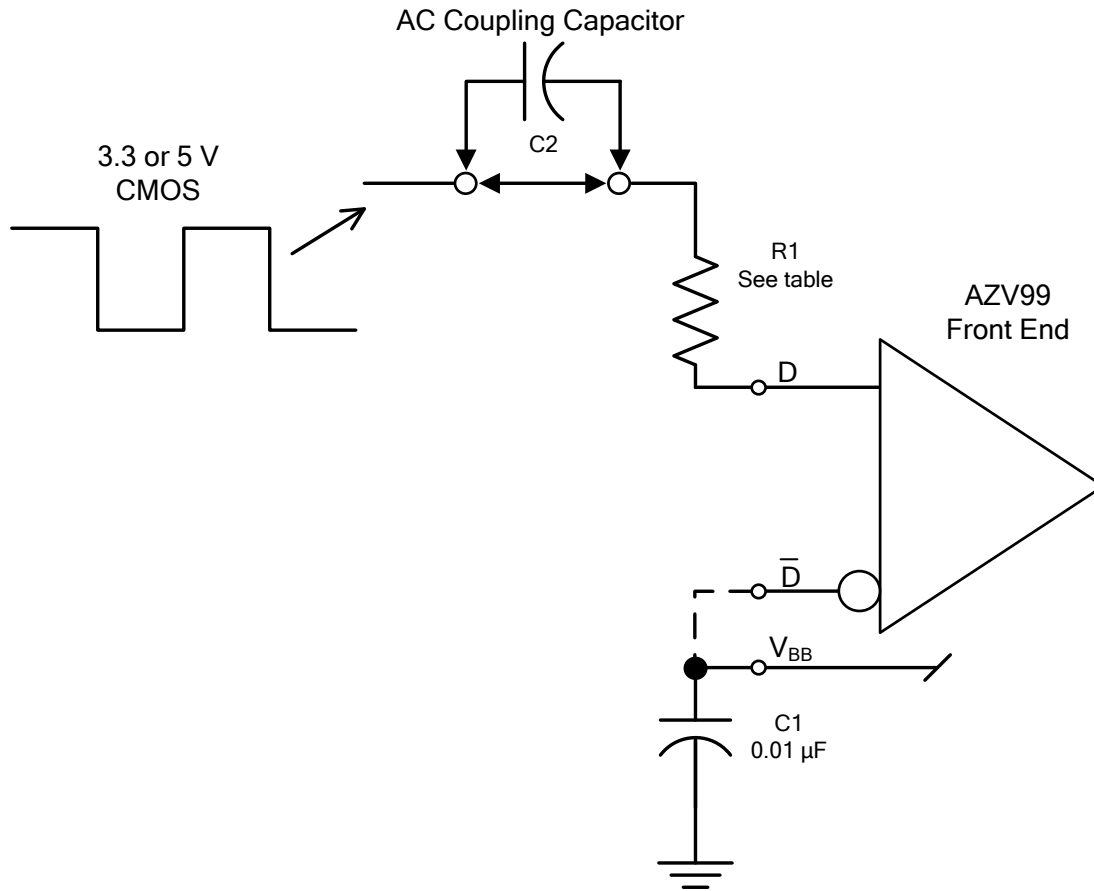
**S12, D to Q, 50 Ω AC load on Q**



**S21, D to Q, 50 Ω AC load on Q**



**S22, D to Q, 50 Ω AC load on Q**



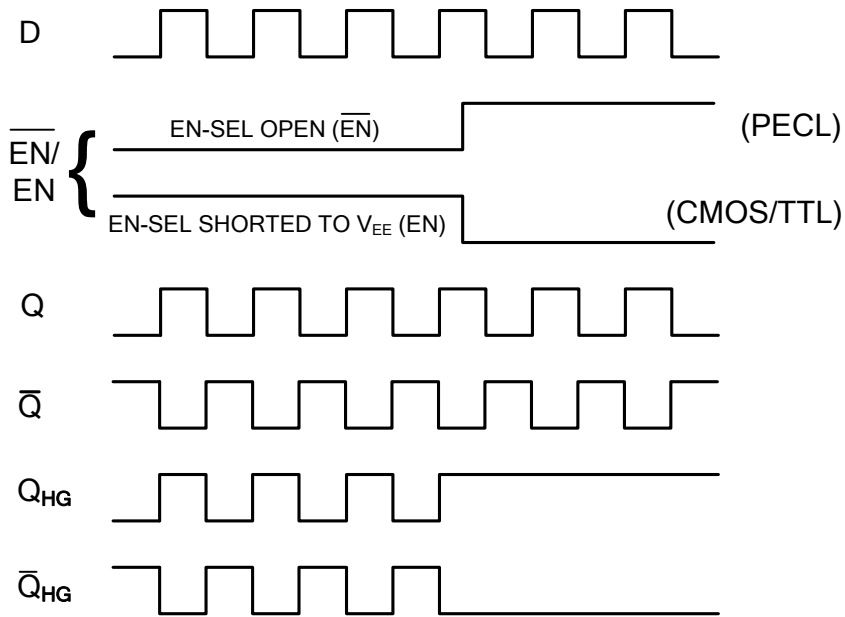
### Application Circuit for CMOS Inputs

Input Type	R1 <sup>1</sup>	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	1.1 kΩ	2.0 kΩ
5 V CMOS	1.6 kΩ	3.3 kΩ

<sup>1</sup> R1 should be chosen so that the input swing on the D input with respect to  $\bar{D}$  is in the range of  $\pm 80$  to  $\pm 1000$  mV, per the AC Characteristics table and the D input is  $< \pm 750$  mV with respect to V<sub>BB</sub>.

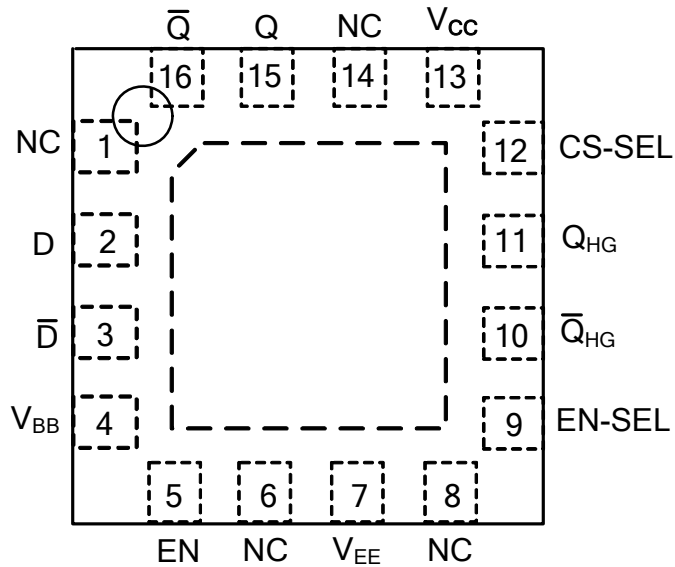
### Recommended Component Values for CMOS Single Ended Inputs

**TIMING DIAGRAM**



**PINOUT FOR AZV99L**

MLP 16, 3x3mm  
AZV99L

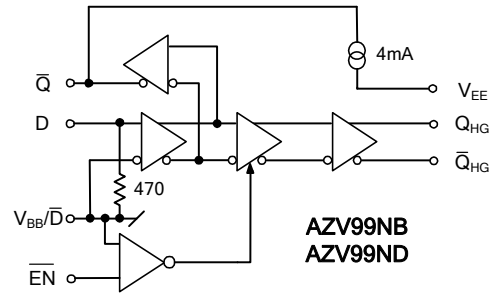
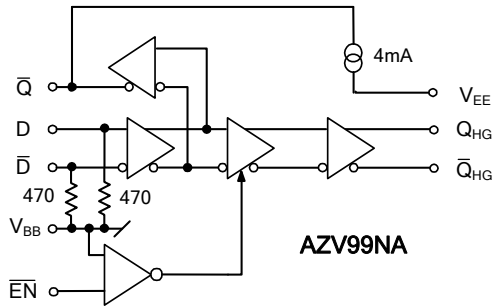


**TOP VIEW**

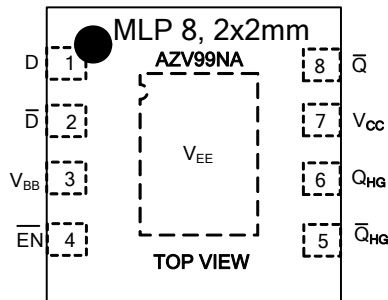
Bottom Center Pad may be left open or tied to V<sub>EE</sub>



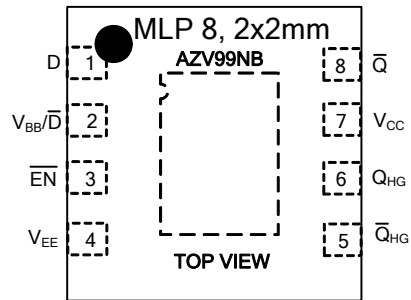
**LOGIC DIAGRAMS AND PINOUTS FOR  
AZV99NA, AZV99NB, AZV99ND**



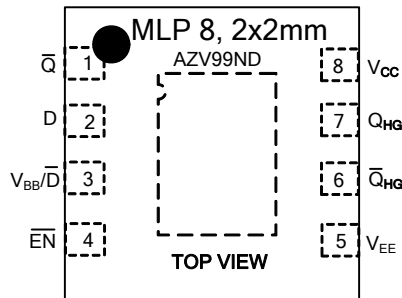
**EN operation follows PECL functionality. See the  
Timing Diagram.**



**Bottom Center Pad is the  $V_{EE}$   
return.**

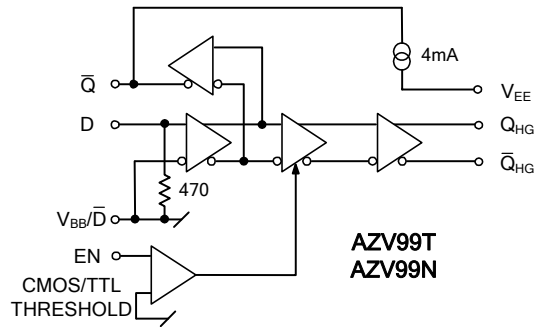


**Bottom Center Pad may be left open  
or tied to  $V_{EE}$ . Pin 4 is the  $V_{EE}$   
return.**

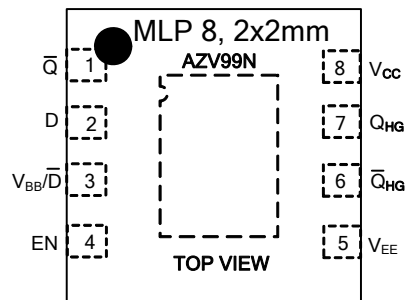
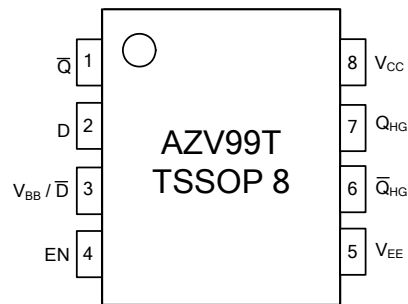


**Bottom Center Pad may be left open  
or tied to  $V_{EE}$ . Pin 5 is the  $V_{EE}$   
return.**

**LOGIC DIAGRAM AND PINOUTS FOR  
AZV99T, AZV99N**



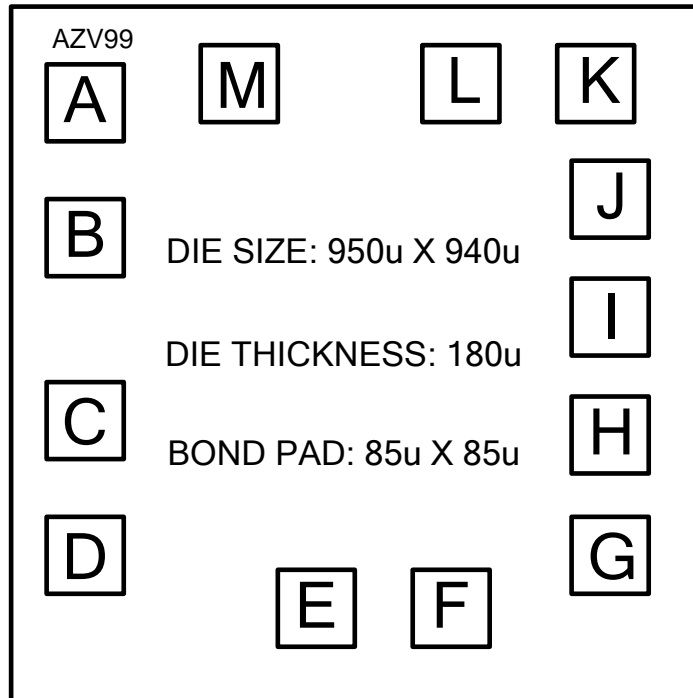
**EN follows CMOS/TTL functionality. See the Timing Diagram.**



**Bottom Center Pad may be left open or tied to V<sub>EE</sub>. Pin 5 is the V<sub>EE</sub> return.**

**DIE PAD COORDINATES**

AZV99 DIE:

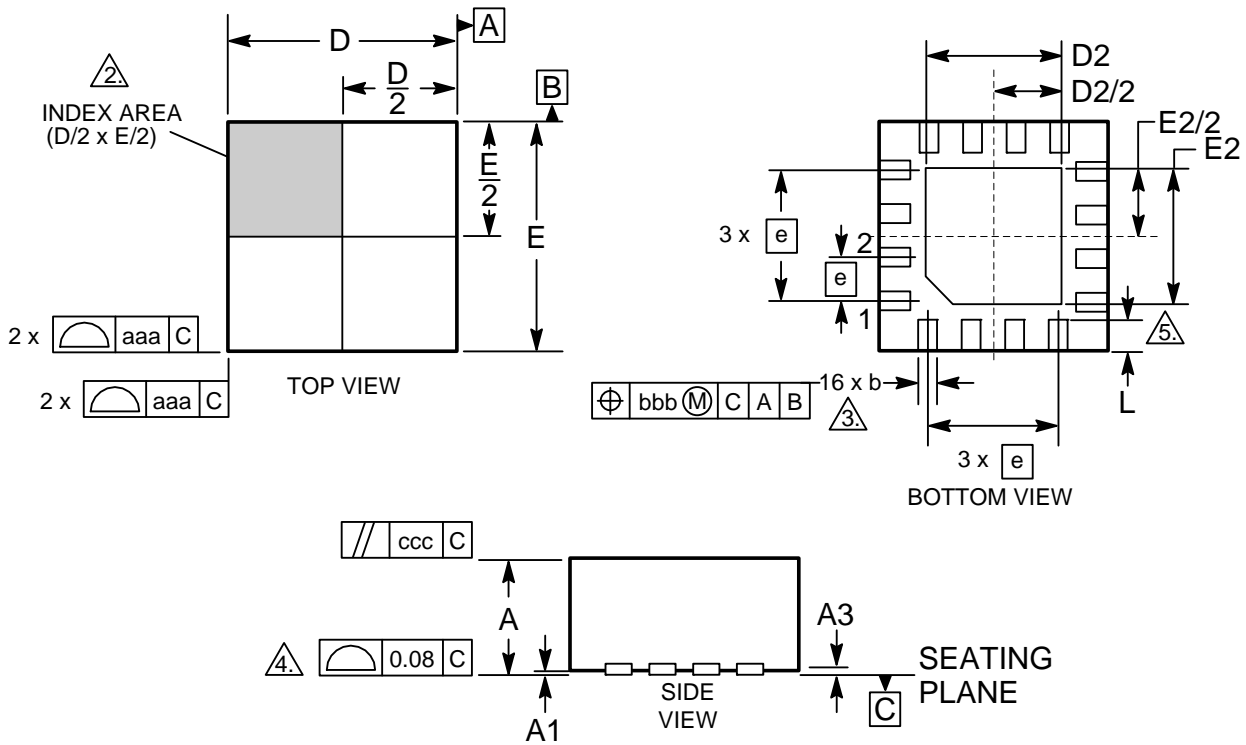


**PAD COORDINATES<sup>1</sup>**

NAME	PAD DESIGNATION	PAD CENTERS	
		X(Microns)	Y(Microns)
A	D	-342.5	312.5
B	$\bar{D}$	-342.5	144.5
C	$V_{BB}$	-342.5	-87.0
D	EN/ $\bar{EN}$	-342.5	-255.0
E	$V_{EE}$	-33.5	-312.5
F	NC	126.5	-312.5
G	EN-SEL	312.5	-248.5
H	$\bar{Q}_{HG}$	312.5	-98.5
I	$Q_{HG}$	312.5	51.5
J	CS-SEL	312.5	201.5
K	$V_{CC}$	302.5	342.5
L	Q	142.5	342.5
M	$\bar{Q}$	-140.5	342.5

1. 0, 0 is center of die.

**PACKAGE DIAGRAM  
MLP 16**

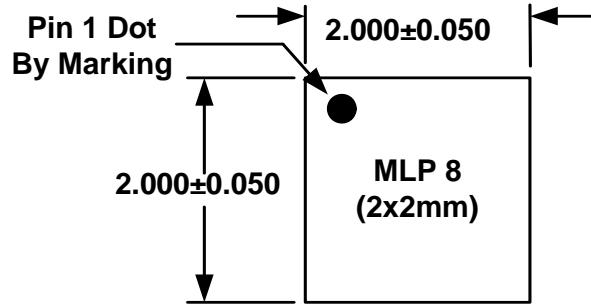


**NOTES:**

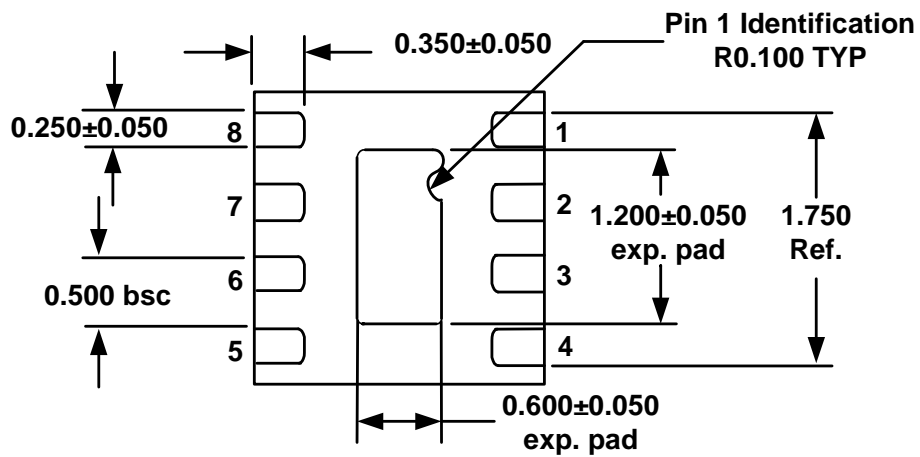
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
- $\triangle 2$ . THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
- $\triangle 3$ . DIMENSION  $b$  APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
- $\triangle 4$ . COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- $\triangle 5$ . INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

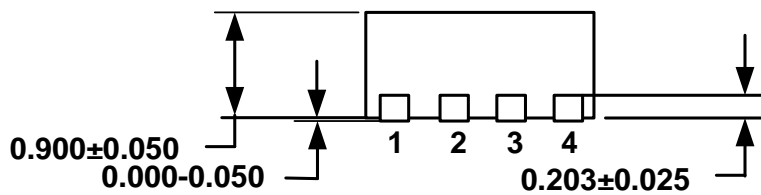
**PACKAGE DIAGRAM**  
**MLP 8 2x2mm**



TOP VIEW



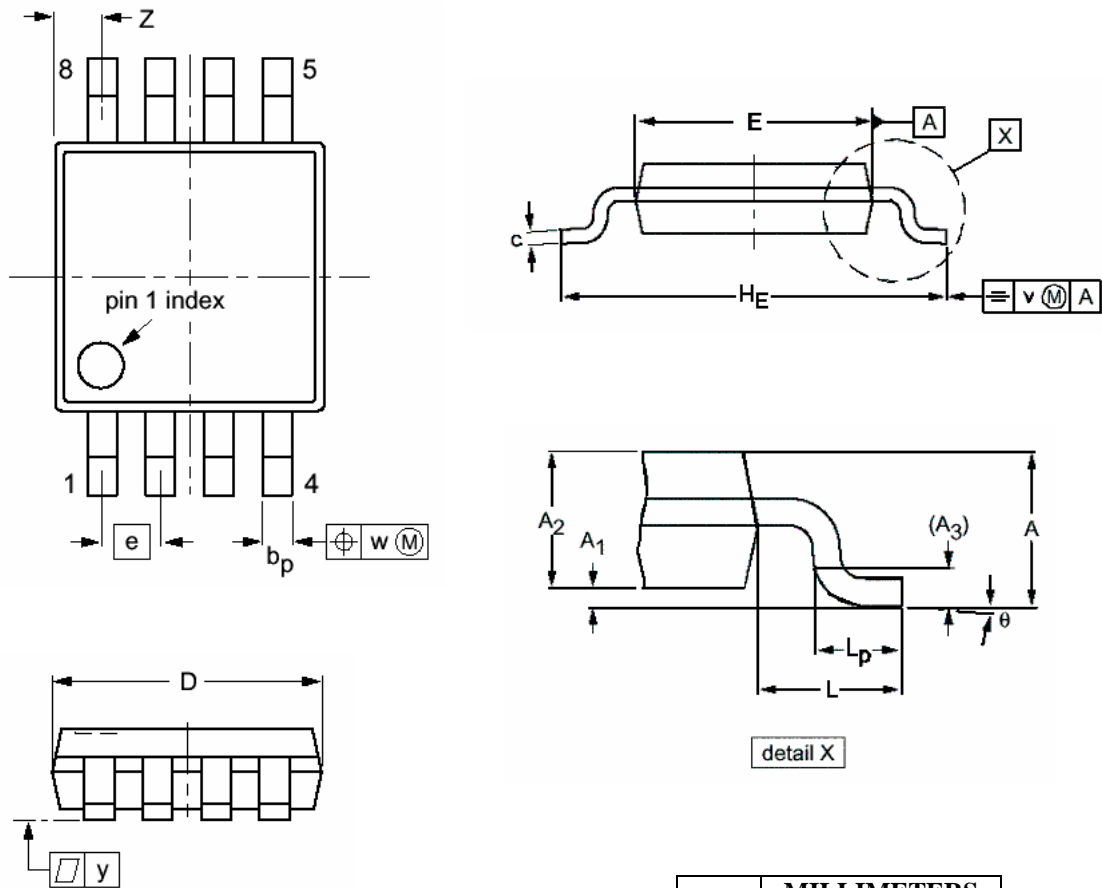
BOTTOM VIEW



SIDE VIEW

**Note: All dimensions are in mm**

**PACKAGE DIAGRAM  
TSSOP 8**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
  3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A <sub>1</sub>	0.05	0.15
A <sub>2</sub>	0.80	0.95
A <sub>3</sub>	0.25	
b <sub>p</sub>	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H <sub>E</sub>	4.70	5.10
L	0.94	
L <sub>p</sub>	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

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