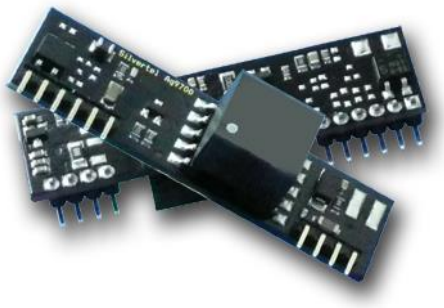
Silvertel

Ag9700

Power-Over-Ethernet Module



1. Features

- IEEE802.3af compliant
- Small SIL package
- Low cost, with minimal external components required
- Input voltage range 36V to 57V
- Short-circuit protection
- Adjustable output
- 1500V isolation (input to output)
- High performance option available with classification programming, industrial temperature range and thermal protection (Ag9700-FL)
- Silvertel “design-in” assistance

2. Description

The Ag9700 series of modules are designed to extract power from a conventional twisted pair Category 5 Ethernet cable, conforming to the IEEE 802.3af Power-over-Ethernet (PoE) standard.

The Ag9700 signature and control circuit provides the PoE compatibility signature required by the Power Sourcing Equipment (PSE) before applying up to 15W power to the port. By default all variants of the Ag9700 provides a Class 0 signature; but the Ag9700-FL has the additional feature of classification programming.

The DC/DC converter operates over a wide input voltage range and provides a regulated output. The DC/DC converter also has built-in short-circuit output protection.

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3. Ag9700 Product Selector

Part Number†	Nominal Output Voltage	Maximum Output Power *	Marking
Ag9712-S	12.0V	12 Watts	12S
Ag9705-S	5.0V	9 Watts	5S
Ag9703-S	3.3V	6 Watts	3S
Ag9712-2BR	12.0V	12 Watts	12B
Ag9705-2BR	5.0V	9 Watts	5B
Ag9703-2BR	3.3V	6 Watts	3B
Ag9724-FL	24.0V	12 Watts	24FL
Ag9712-FL	12.0V	12 Watts	12FL
Ag9705-FL	5.0V	9 Watts	5FL
Ag9703-FL	3.3V	6 Watts	3FL

*At 25°C with V_{IN} = 48V
† The Ag9700 fully meets the requirements of RoHS directive 2011/65/EC & EU RoHS 2, Moisture Sensitive Level 1 and HBM 1.

Table 1: Ordering Information

The Ag9700-2BR and Ag9700-FL are physically the same size as the Ag9700-S, but they have the two input bridge rectifiers on-board (see Figure 1).

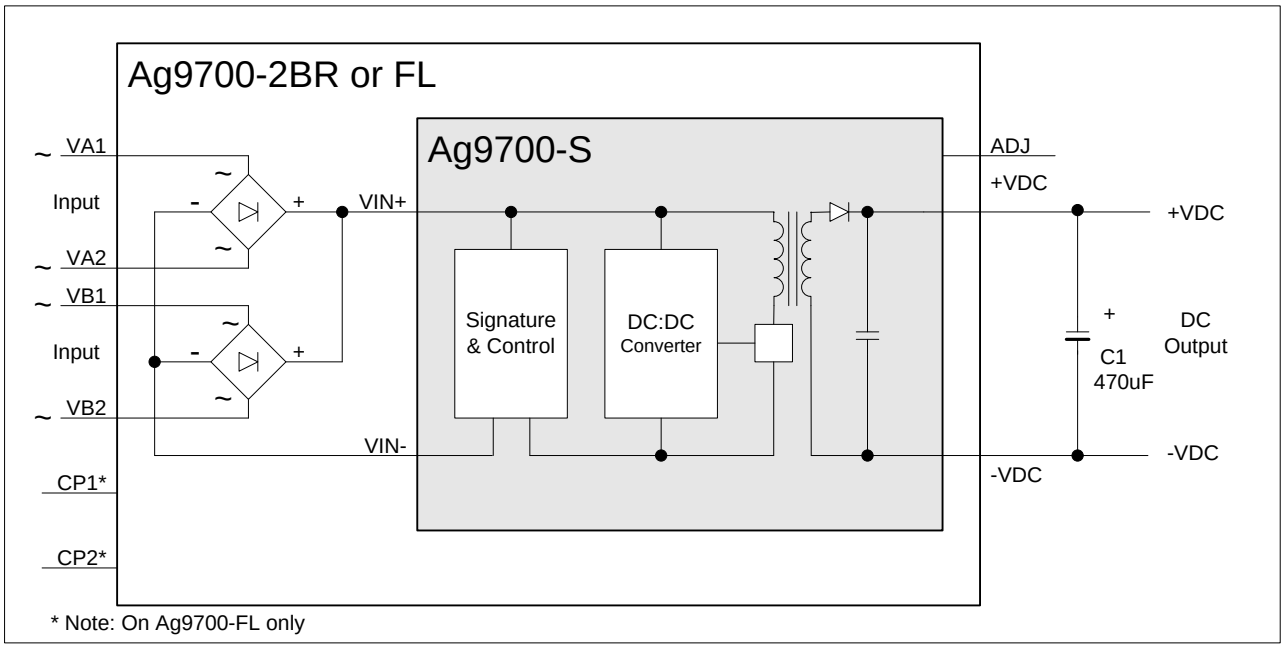


Figure 1: Block Diagram

4. Pin Description

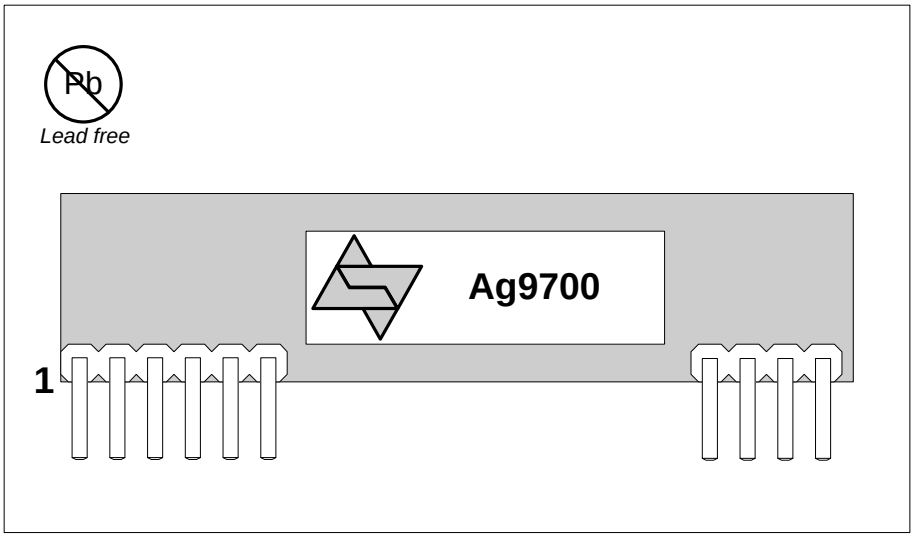


Figure 2: Ag9700 SIL Package Format

4.1 Ag9700-S

Pin #	Name	Description
1	VIN+	**Direct Input +**. This pin connects to the positive (+) output of the input bridge rectifiers (internally connected to pin 3).
2	VIN-	**Direct Input -**. This pin connects to the negative (-) output of the input bridge rectifiers (internally connected to pins 4).
3	VIN+	**Direct Input +**. Internally connected to pin 1.
4	VIN-	**Direct Input -**. Internally connected to pin 2.
5	IC	**Internal Connection.** Do not connect to this pin.
6	NC	**No Connection.**
7	-VDC	**DC Return.** This pin is the return path for the +VDC output.
8	+VDC	**DC Output.** This pin provides the regulated output from the DC/DC converter.
9	ADJ	**Output Adjust.** The output voltage can be adjusted from is nominal value, by connecting an external resistor from this pin to either the +VDC pin or the -VDC pin.
10	IC	**Internal Connection.** Do not connect to this pin.

Table 2: Pin Description

4.2 Ag9700-2BR

Pin #	Name	Description
1	VA1	**RX Input (1)**. This input pin is used in conjunction with VA2 and connects to the centre tap of the transformer connected to pins 1 & 2 of the RJ45 connector (RX) - it is not polarity sensitive.
2	VA2	**TX Input (2)**. This input pin is used in conjunction with VA1 and connects to the centre tap of the transformer connected to pins 3 & 6 of the RJ45 connector (TX) - it is not polarity sensitive.
3	VB1	**Direct Input (1)**. This input pin is used in conjunction with VB2 and connects to pin 4 & 5 of the RJ45 connector - it is not polarity sensitive.
4	VB2	**Direct Input (2)**. This input pin is used in conjunction with VB1 and connects to pin 7 & 8 of the RJ45 connector - it is not polarity sensitive.
5	IC	**Internal Connection.** Do not connect to this pin.
6	NC	**No Connection.**
7	-VDC	**DC Return.** This pin is the return path for the +VDC output.
8	+VDC	**DC Output.** This pin provides the regulated output from the DC/DC converter.
9	ADJ	**Output Adjust.** The output voltage can be adjusted from is nominal value, by connecting an external resistor from this pin to either the +VDC pin or the -VDC pin.
10	IC	**Internal Connection.** Do not connect to this pin.

Table 3: Pin Description

4.3 Ag9700-FL

Pin #	Name	Description
1	VA1	**RX Input (1)**. This input pin is used in conjunction with VA2 and connects to the centre tap of the transformer connected to pins 1 & 2 of the RJ45 connector (RX) - it is not polarity sensitive.
2	VA2	**TX Input (2)**. This input pin is used in conjunction with VA1 and connects to the centre tap of the transformer connected to pins 3 & 6 of the RJ45 connector (TX) - it is not polarity sensitive.
3	VB1	**Direct Input (1)**. This input pin is used in conjunction with VB2 and connects to pin 4 & 5 of the RJ45 connector - it is not polarity sensitive.
4	VB2	**Direct Input (2)**. This input pin is used in conjunction with VB1 and connects to pin 7 & 8 of the RJ45 connector - it is not polarity sensitive.
5	CP1	**Class Programming (1).** Connecting an external resistor between this pin and CP2 will change the current class of the module (see Section 5.4). With no resistor fitted the Ag9700-FL will default to Class 0.
6	CP2	**Class Programming (2).** Connecting an external resistor between this pin and CP1 will change the current class of the module (see Section 5.4). With no resistor fitted the Ag9700-FL will default to Class 0.
7	-VDC	**DC Return.** This pin is the return path for the +VDC output.
8	+VDC	**DC Output.** This pin provides the regulated output from the DC/DC converter.
9	ADJ	**Output Adjust.** The output voltage can be adjusted from is nominal value, by connecting an external resistor from this pin to either the +VDC pin or the -VDC pin.
10	IC	**Internal Connection.** Do not connect to this pin.

Table 4: Pin Description

5. Functional Description

5.1 Inputs

The Ag9700 is compatible with equipment that uses Alternative A or Alternative B options, see Figure 3. It is specified that the PSE does not apply power to both outputs at the same time (Refer to IEEE802.3af for more information).

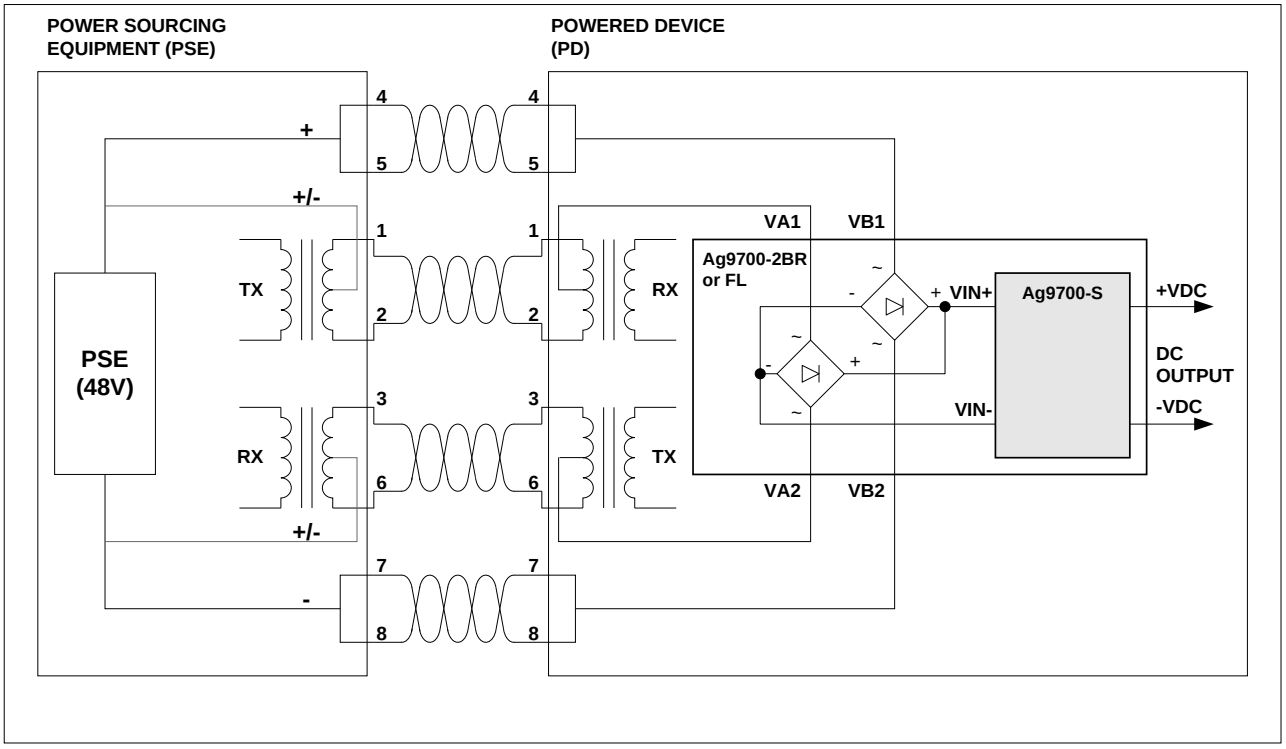


Figure 3: Typical System Diagram

5.2 PD Signature

When the Ag9700 is connected to the Cat 5e cable, it will automatically present a Powered Device (PD) signature to the Power Sourcing Equipment (PSE), when requested. The equipment will then recognise that a PD is connected to that line and supply power.

5.3 Isolation

To meet the safety isolation requirements of IEEE802.3af section 33.4.1 a PD must pass the electrical strength test of IEC 60950 sub clause 6.2. This calls for either a) 1500Vac test or b) 1500V impulse test.

The Ag9700 is specified to meet the 1500Vdc impulse test. It is also important that the tracks on either side of the isolation barrier have at least a 3mm clearance, see Figures 9 & 10 and Section 7 for more information.

5.4 Power Classification Programming (Ag9700-FL only)

This feature is optional from the PSE and is used for power management. The Ag9700-FL allows the Class to be externally programmed by connecting a resistor between the CP1 and CP2 pins, see Figure 4. If no resistor is fitted the Ag9700-FL will default to Class 0, a full list of programming resistor values are shown in Table 5.

CLASS	Programming Resistance (Ohms)	Min Power (W)	Max Power (W)
0	Do not fit	0.44	12.95
1	698 ±1%	0.44	3.84
2	383 ±1%	3.84	6.49
3	249 ±1%	6.49	12.95
4	TBD	Reserved	Reserved

Table 5: Class Programming

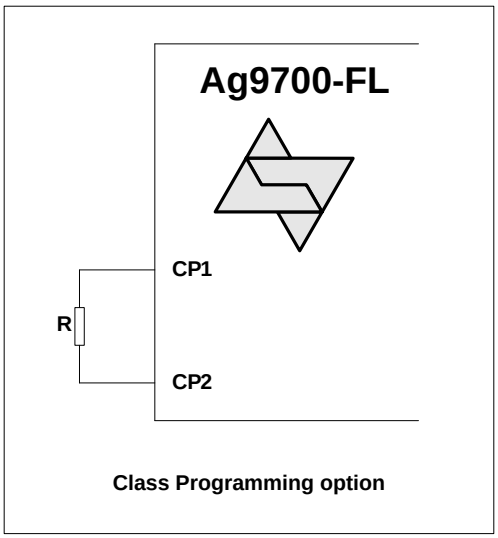


Figure 4: Class Programming Option

Note: The Ag9700-S and 2BR do not have classification programming and are fixed to Class 0 (0.44 Watts to 12.95 Watts).

5.5 DC/DC Converter

The Ag9700's DC/DC converter provides a regulated output that has built-in short-circuit output protection – refer to Table 1 for voltage and power ratings.

5.6 Output Adjustment

The Ag9700 has an ADJ pin, which allows the output voltage to be increased or decreased from its nominal value. Figure 5 shows how the ADJ pin is connected.

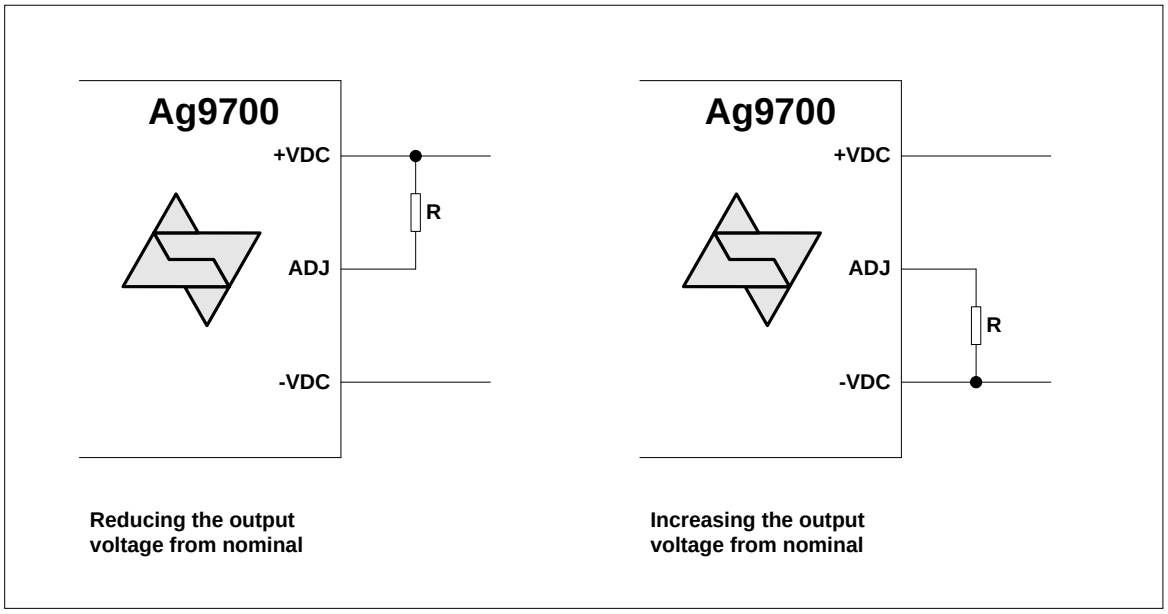


Figure 5: Output Adjustment

Reducing the output voltage, connect R between ADJ and +VDC							
Ag9703		Ag9705		Ag9712		Ag9724	
Value of R	Output	Value of R	Output	Value of R	Output	Value of R	Output
Open	3.30V	Open	5.00V	Open	12.00V	Open	24.00V
0 Ohms	3.20V	0 Ohms	4.45V	0 Ohms	10V	0 Ohms	19.5V
Increasing the output voltage, connect R between ADJ and -VDC							
Ag9703		Ag9705		Ag9712		Ag9724	
Value of R	Output	Value of R	Output	Value of R	Output	Value of R	Output
Open	3.3V	Open	5.00V	Open	12.00V	Open	24.00V
0 Ohms	3.75V	0 Ohms	5.65V	0 Ohms	12.65V	0 Ohms	24.65V

Table 6: Output Adjustment Resistor (R) Value

5.7 Typical Connections

The Ag9700 requires minimal external components for a basic configuration, as shown in Figure 6.

C1 must be fitted for output stability and should be a minimum of 470µF. This capacitor should be positioned as close to the output pins as possible. C1 is also required to handle load step changes and reduce the output ripple. For applications where the output needs to cope with high load step changes, the value of C1 may need to be increased to a minimum of 1000µF. This can be a standard low cost electrolytic, but by using a low ESR electrolytic this would reduce the ripple. A low ESR capacitor is recommended for operation below 0°C.

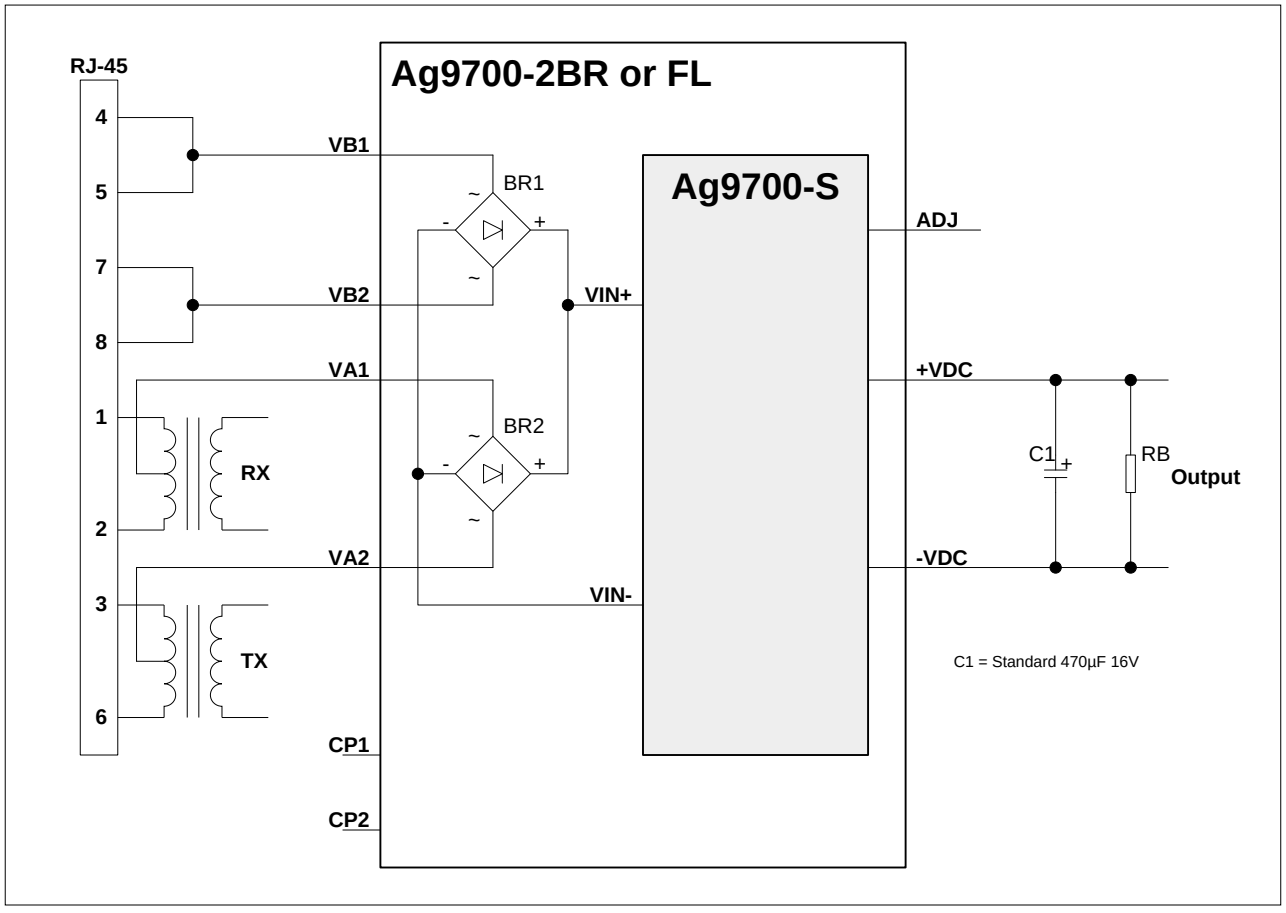


Figure 6: Basic Connection Diagram

The output adjust input (ADJ) is optional, it is provided to give greater flexibility to the Ag9700 product range. Further information on using these inputs can be found in Section 5.6.

The classification programming inputs (on the Ag9700-FL) are also optional. Further information can be found in Section 5.4.

The Ag9700 must always supply a minimum current, see Table 11.3. The Ag9700 will not be damaged if operated below this level, but it can emit a low level audible noise. If this audible noise is not an issue, then it is possible for the Ag9700 to work safely with no load at all. But to ensure that the PSE has a sufficient load to meet its Maintain Power Signature (MPS), it would be advisable not to operate the Ag9700 below the specified minimum load.

5.8 Additional Output Filtering

The Ag9700-FL has a built-in PI filter and should only require the external electrolytic capacitor as shown in Figure 6.

The Ag9700-S and 2BR output ripple and noise can be improved with additional output filtering. Figure 6 shows the basic output filtering for ripple and noise; which at maximum load this is typically 200mVp-p (for Ag9712-S or 2BR). Figure 7 shows two cost effective methods that can be used to reduce the ripple and noise, if required.

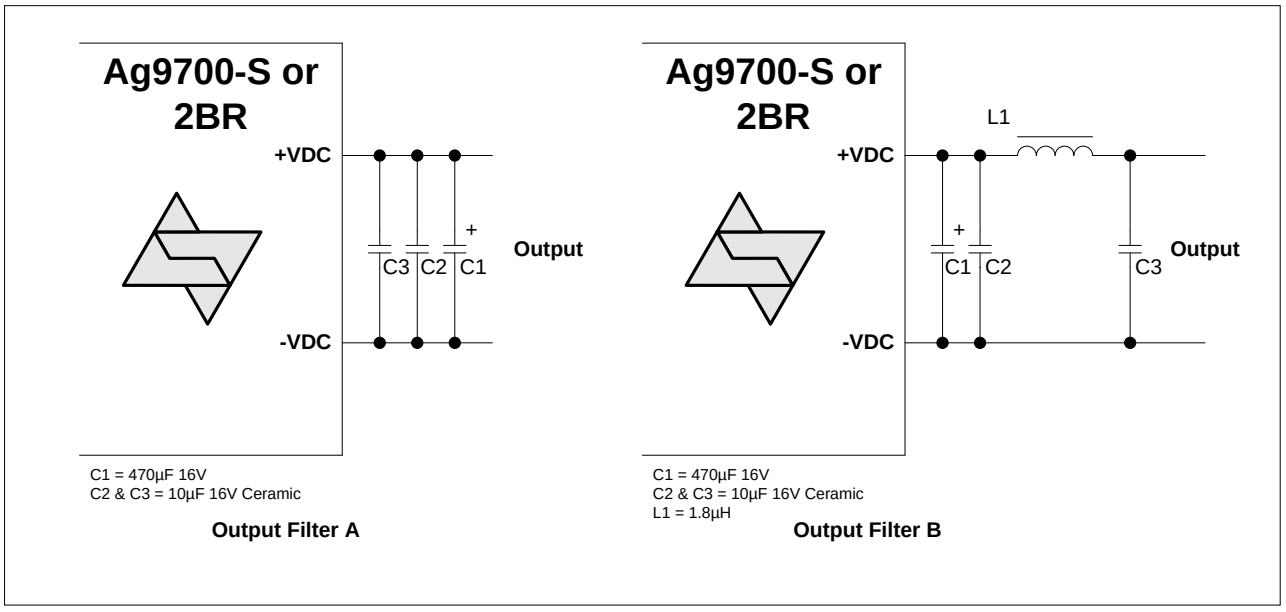


Figure 7: Output Filtering for the Ag9700-S or 2BR

The simplest and cheapest solution is shown in Figure 7 - Output Filter A. This will reduce the ripple and noise to typically 135mVp-p. Adding a PI filter, as shown in Figure 7 – Output Filter B, will take the ripple and noise level down to typically 14mVp-p. A low ESR electrolytic is recommended for operation below 0°C.

5.9 Start-up Power

It is important that during start-up the Ag9700 input voltage is ≥42V, this will ensure that the module powers up correctly. Once the dc/dc converter is up and running the module will work normally even if the input voltage is reduced to its minimum level of 36V.

When using an IEEE802.3af compliant PSE this will not be an issue, as the minimum output voltage of the PSE must be ≥44V.

6. Typical Application

The Ag9700 can be used in numerous applications. In the example shown in Figure 8, the data outputs from the switch are connected to the inputs of a midspan. The midspan will then add power (to the data) on each output that supports Power over Ethernet (PoE).

In this example port 1 is connected to an Ethernet camera and port 2 is connected to a wireless access point, both of these devices have a built-in Ag9700. When the midspan is switched on (or when the device is connected), the midspan will check each output for a PoE signature. On ports 1 and 2 the Ag9700 will identify themselves as PoE enabled devices and the midspan will supply both data and power to these peripherals.

The other ports (shown in this example) will not have a PoE signature and the midspan will only pass the data through to these peripherals. The midspan will continuously monitor each output to see if a PoE enabled device has been added or removed.

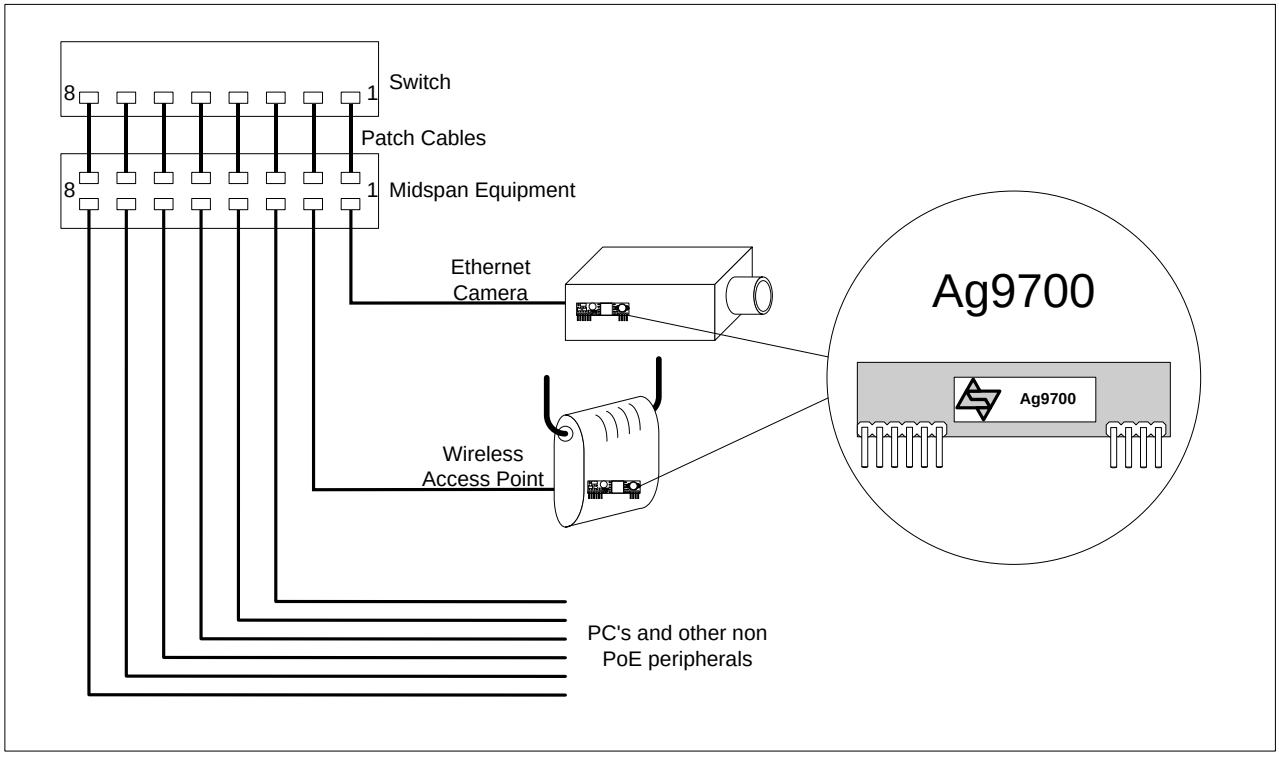


Figure 8: Typical Application

7. Layout Recommendations

Figure 9: gives an example of the tracking needed for the Ag9700 SIL Layout configured with Output Filter A (R1, R2, C2 and C3 are optional components, but C1 must be fitted). The thermal performance of the Ag9700 can be improved by increasing the surface area of the output tracks (+VDC and -VDC). This is not applicable if the Ag9700 is in a socket.

The Keep out area shows the position of the isolation barrier and must be kept clear of tracks.

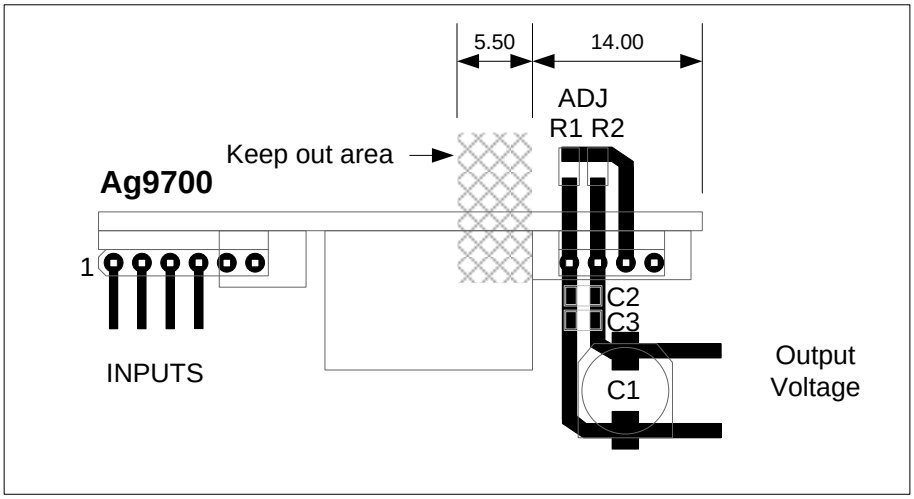


Figure 9: Typical SIL Layout

8. Operating Temperature Range

Because the Ag9700 is a power component, it will generate heat, so it is important that this be taken into consideration at the design stage.

The heart of the Ag9700 is a DC/DC converter, which like any other power supply will generate heat. The amount of heat generated by the module will depend on the load it is required to drive and the input voltage supplied by the PSE. The information shown within this section of datasheet is referenced to a nominal 48Vdc input voltage supplied by the PSE.

The Ag9700-S and 2BR has a maximum ambient* operating temperature of 70°C, see Figures 11 to 13. The Ag9700-FL has a maximum ambient operating temperature of 85°C, see Figures 14 to 17. These results were measured without any heatsink in an Associated Environmental System SD-302. The performance of the Ag9700 can be improved by forcing the airflow over the part or by using a heatsink (see the Ag9700 application note “ANX-POE-Thermal Considerations” for more information).

The Ag9700-FL has built-in thermal protection, so the module will protect itself. But the Ag9700-S and 2BR do not have built-in thermal protection, so it is very important that the maximum ambient temperature is not exceeded. To prevent the module from being damaged it is recommended that the module be powered by an IEEE 802.3af compliant PSE or Midspan equipment. However the Ag9700 may be powered by a user designed power supply which should include thermal and over current protection.

Because each application is different it is impossible to give fixed and absolute thermal recommendations. However it is important that any enclosure used has sufficient ventilation for the Ag9700 and a direct airflow if possible.

One simple method for drawing some of the heat away from the Ag9700 is shown in Figure 10. Power planes connected to the +VDC and -VDC pins of the Ag9700-S, 2BR and FL can be used to draw heat away from the DC/DC converter via the output pins.

These power planes must be on the outer layers of the PCB and the Ag9700 must not be fitted into a socket. The best results are achieved by having power plains on both sides of the main board with multiple through-hole connections (as shown in Figure 10).

*Note: The ambient operating temperature refers to the temperature directly around the Ag9700 and not the temperature outside of the case or enclosure. See application note “ANX-POE-Thermal Considerations” for more details and suggestions for thermal management.

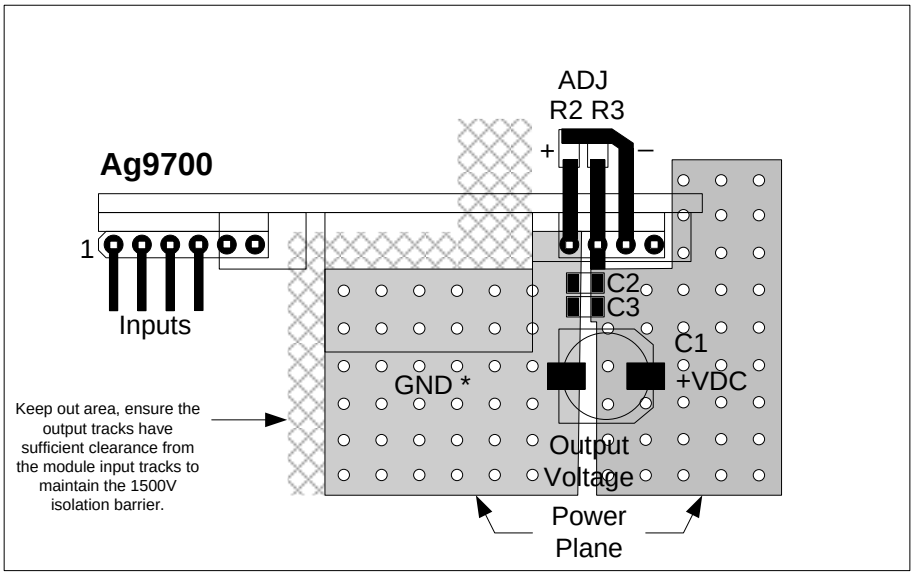


Figure 10: Power Plane Heatsink for Ag9700

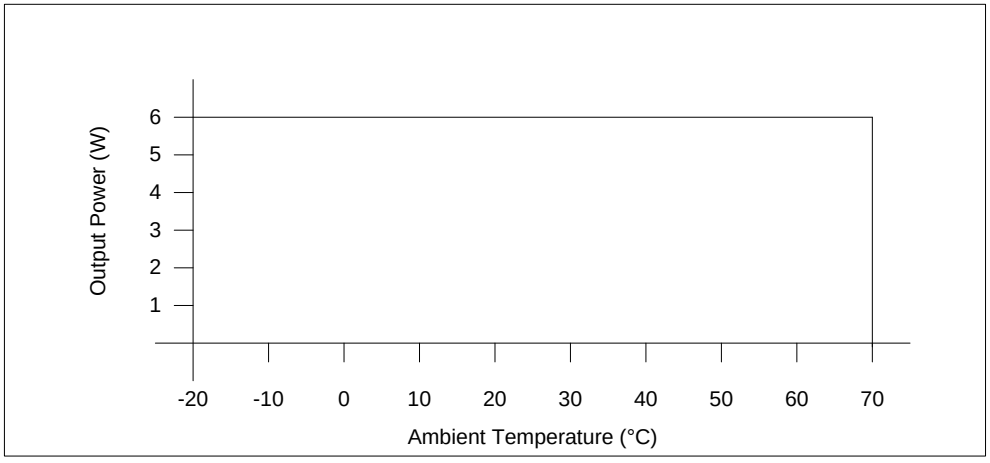


Figure 11: Ag9703-S and 2BR Operating Profile

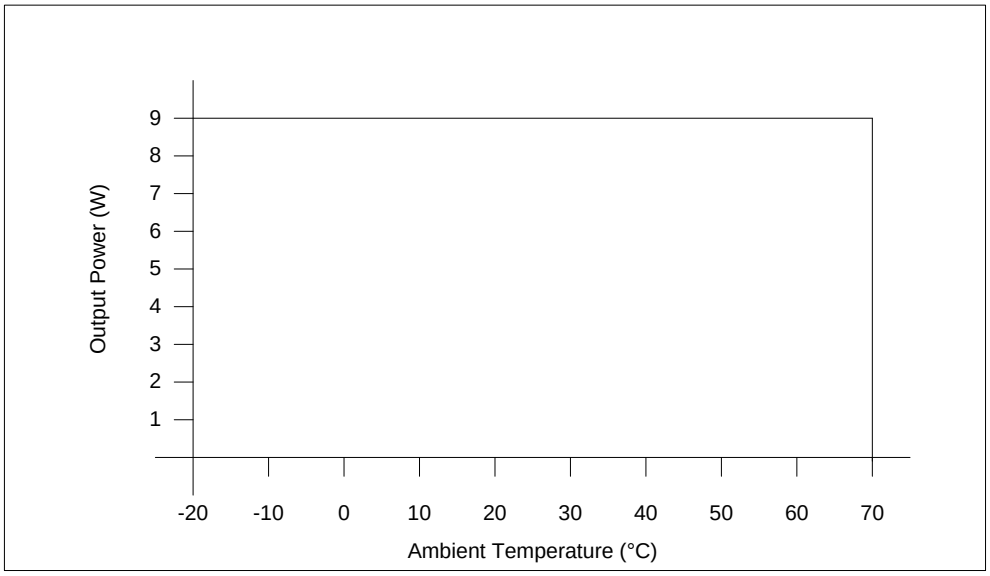


Figure 12: Ag9705-S and 2BR Operating Profile

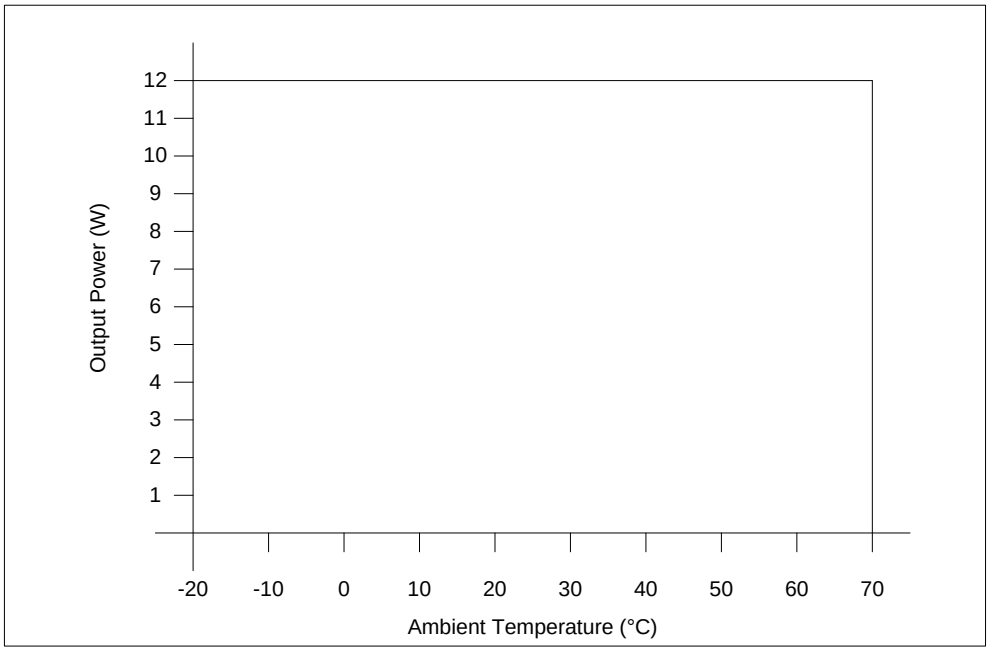


Figure 13: Ag9712-S and 2BR Operating Profile

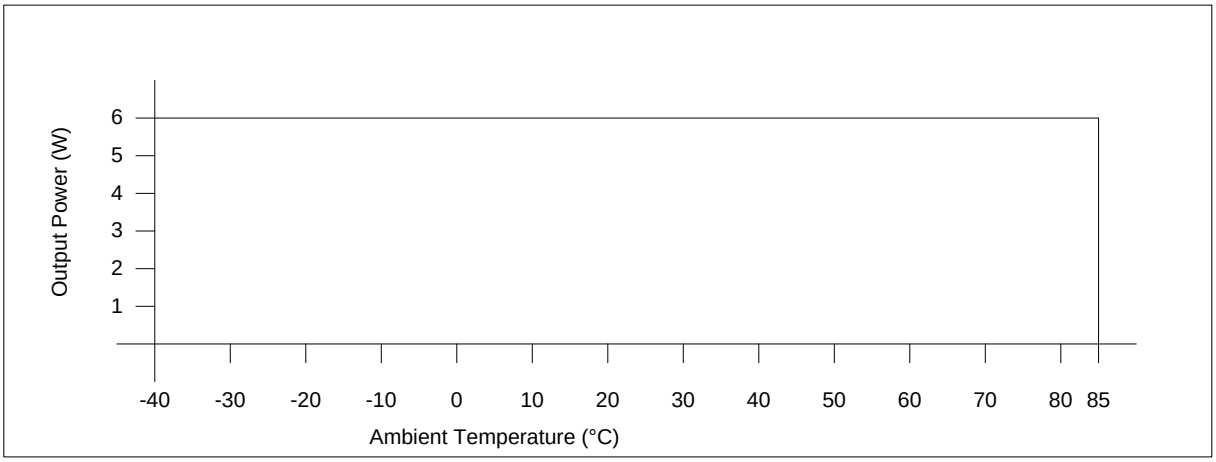


Figure 14: Ag9703-FL Operating Profile

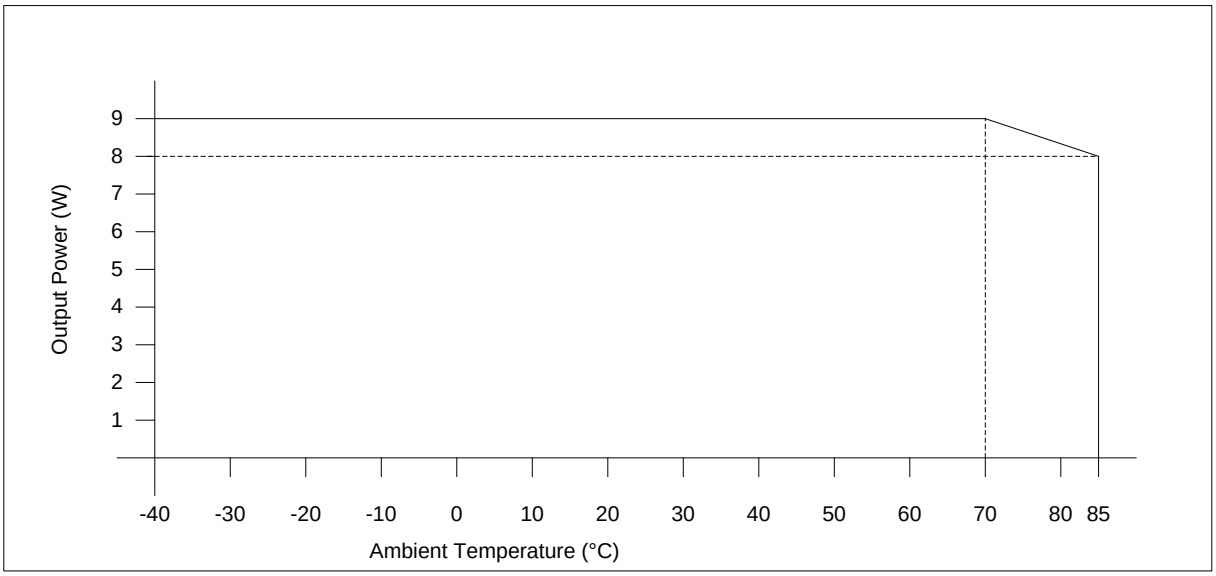


Figure 15: Ag9705-FL Operating Profile

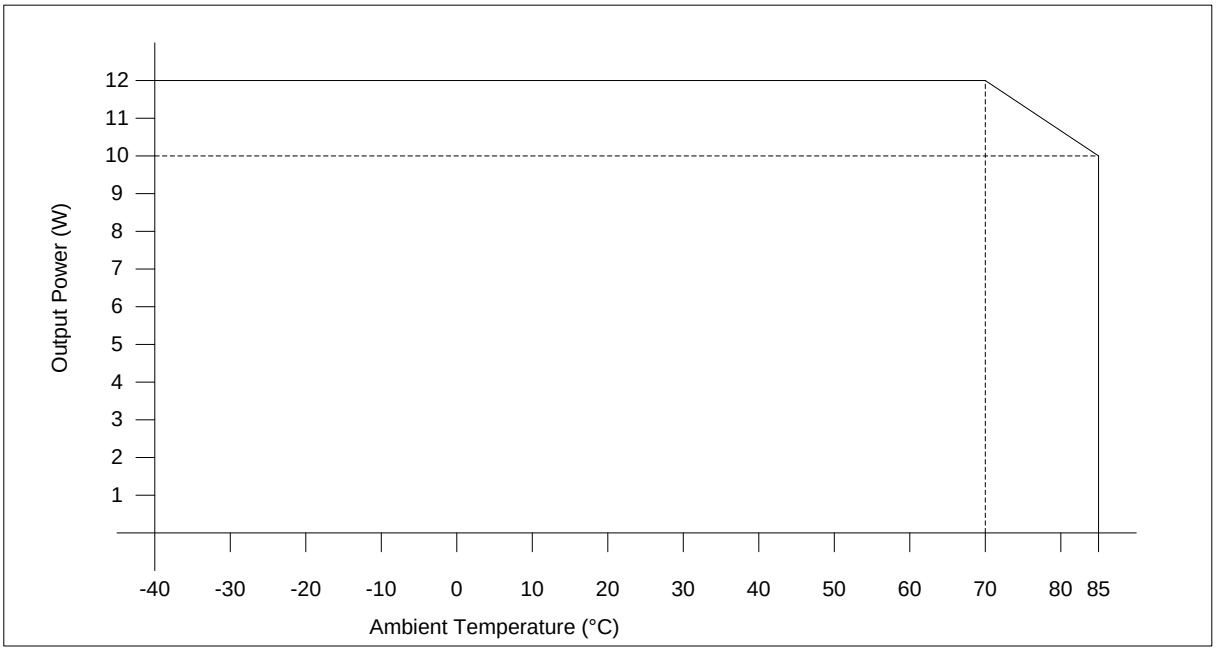


Figure 16: Ag9712-FL Operating Profile

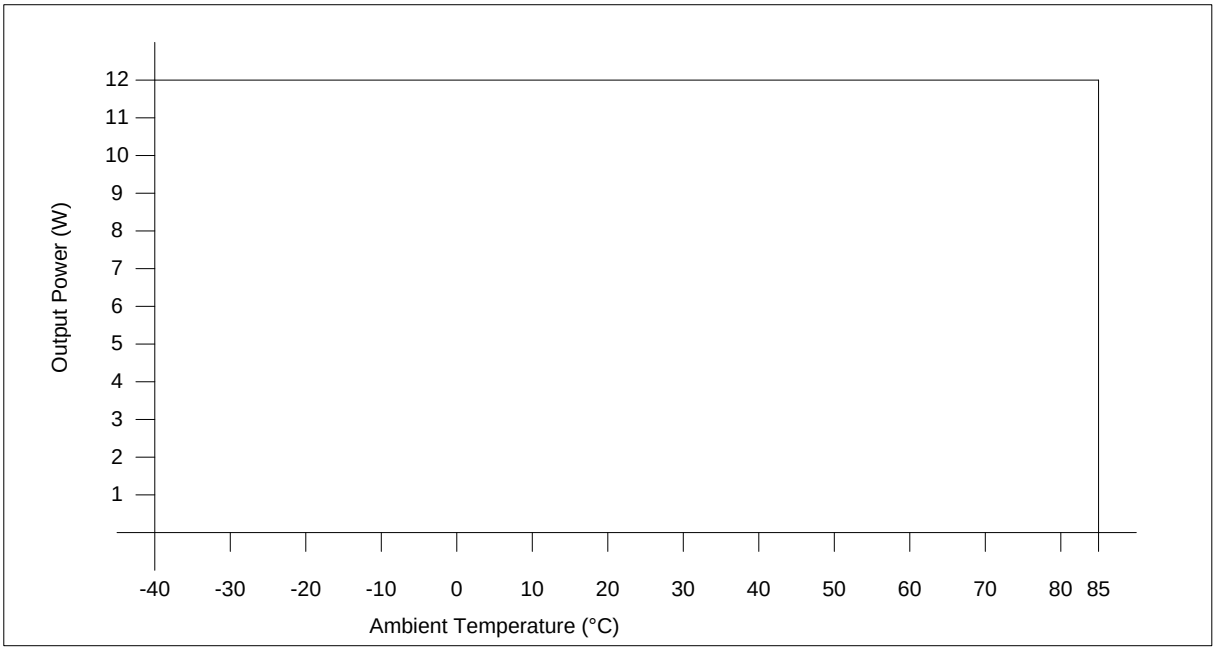


Figure 17: Ag9724-FL Operating Profile

It is important to remember that the ESR of the external electrolytic capacitors will increase considerably when the ambient temperature falls below 0°C. If the Ag9700 is going to be used in applications where the ambient temperature can fall below 0°C, selection of appropriate output filter components must be done at the design stage.

9. Protection

9.1 Input Protection

The Ag9700 must be protected from over-voltages exceeding the 80V maximum rated surge input voltage. An inexpensive but effective solution can be achieved by connecting Tranzorb diodes across each of the inputs; see Figure 18.

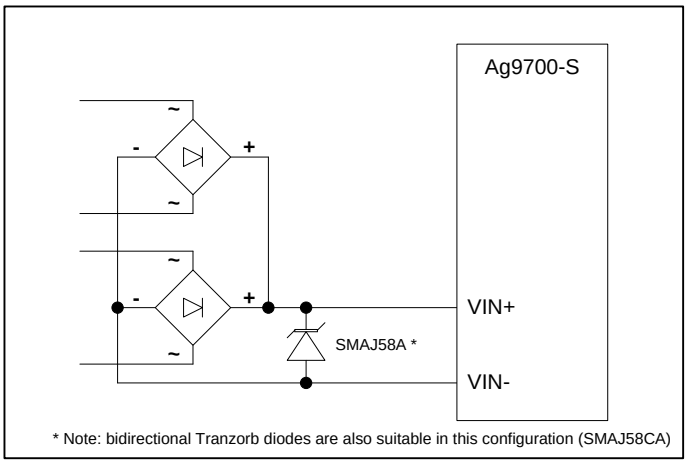


Figure 18: Input Protection

More information is available in Apps Note “ANX-POE-Protection”.

9.2 Thermal Protection

The Ag9700-FL (only) has built-in thermal protection that will protect the module by shutting down the dc/dc converter if exceeded.

10. EMC

The Ag9700 has been designed and tested to meet EN55022 Class B. However, because the Ag9700 will only be one component within a system; it is impossible to say whether the final product will pass EMC testing, without the need for additional filtering. The Ag9700 uses a DC:DC converter with pulse frequency modulation, so care does need to be taken to minimise emissions.

Figure 19 shows our recommended EMC Filter configuration for the Ag9700-S. For more information on the other product variants, refer to the application note “ANX-POE-EMI” on our website.

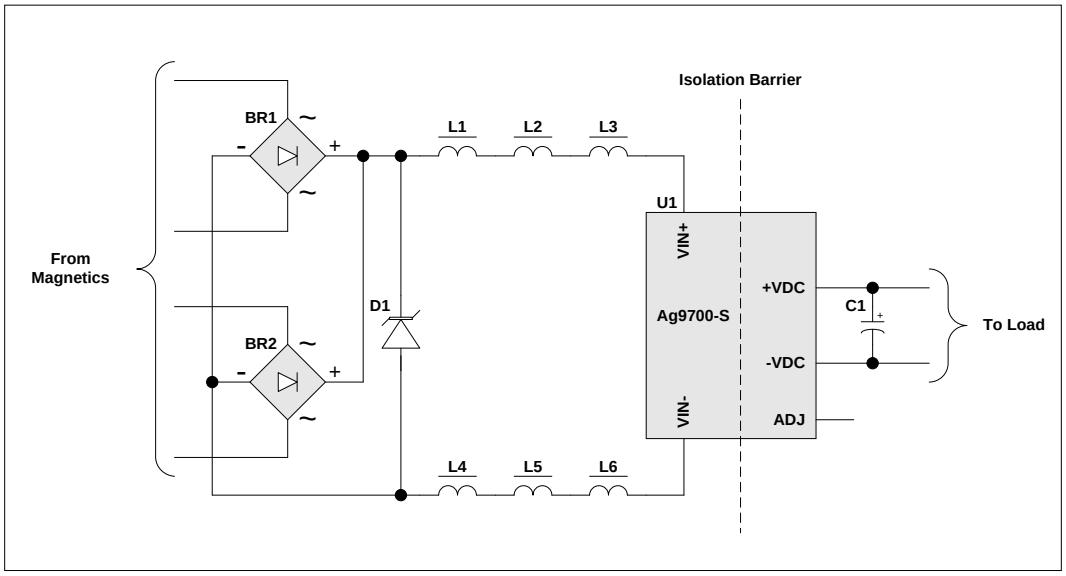


Figure 19: EMC Filtering

Components: -
BR1 & BR2 = MB4S, D1 = SMAJ58A, L1 – L6 = MMZ2012S102A, C1 = 470µF 16V.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings[1]

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{CC}	-0.3	60	V
2	DC Supply Voltage Surge for 1ms	V_{SURGE}	-0.6	80	V
3	Storage Temperature	T_S	-40	+100	^{O}C

Note 1: Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not implied. Maximum ratings assume free airflow.

11.2 Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Units
1	Input Supply Voltage[1]	V_{IN}	36	48	57	V
2	Under Voltage Lockout	V_{LOCK}	30		36	V
3	Operating Temperature[2] Ag9700-S and 2BR Ag9700-FL	T_{OP}	 -20 -40	 25 25	 70 85	Ta / ^{O}C

Note 1: With minimum load
2: See Section Operating Temperature Range

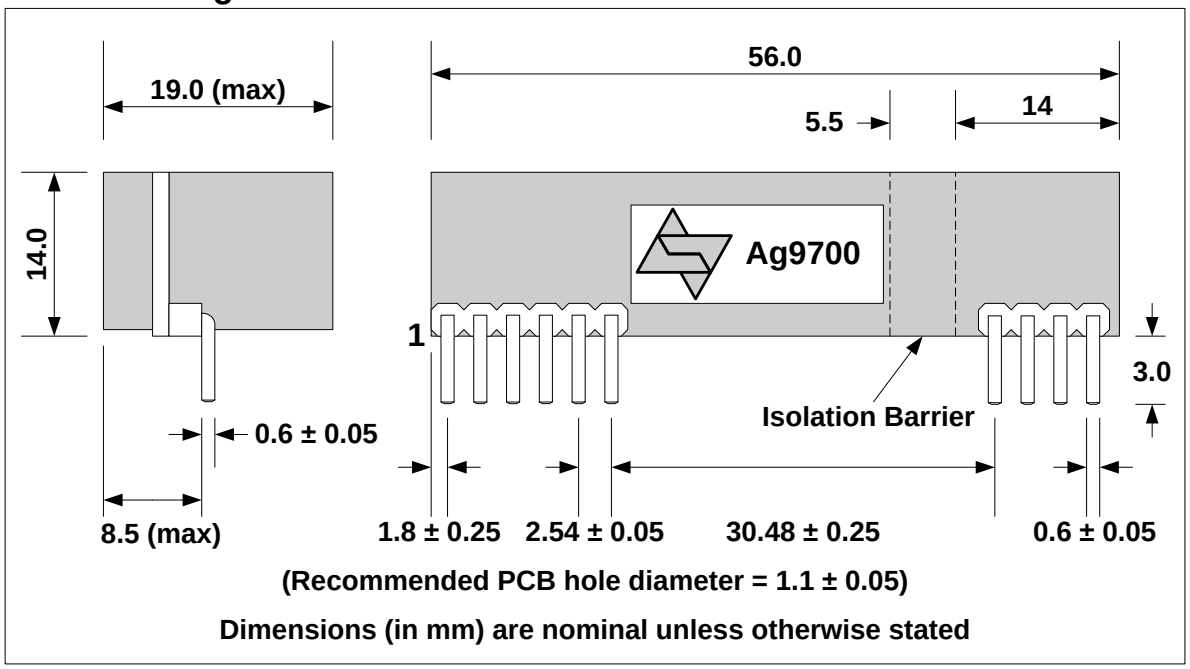
11.3 DC Electrical Characteristics

	DC Characteristic	Sym	Min	Typ[1]	Max	Units	Test Comments
1	Nominal Output Voltage	+VDC	3.1 4.75 11.5 23.5	3.3 5.0 12.0 24	3.5 5.25 12.5 24.5	V V V V	Ag9703 Ag9705 Ag9712 Ag9724-FL
2	Output Current (V_{IN} = 48V)	PWR			1.8 1.8 1.0 0.5	A A A A	Ag9703 Ag9705 Ag9712 Ag9724-FL
3	Line Regulation (V_{IN} = 36V to 57V)	V_{LINE}		0.1		%	@ Max load
4	Load Regulation - Min to Max (V_{IN} = 48V)	V_{LOAD}		1 0.6 0.2 0.2		% % % %	Ag9703 Ag9705 Ag9712 Ag9724-FL
5	Output Ripple and Noise Ag9700-S and 2BR[2] Ag9700-FL	V_{RN}		 200 30		 mVp-p mVp-p	 @ Max load
6	Minimum Load	I_{LOAD}	200 200 100 50			mA mA mA mA	Ag9703 Ag9705 Ag9712 Ag9724-FL
7	Short-Circuit Duration	T_{SC}			∞	sec	
8	Peak Efficiency Ag9703-S Ag9705-S Ag9712-S Ag9703-2BR and FL Ag9705-2BR and FL Ag9712-2BR and FL Ag9724-FL	EFF		 80 84 87 76 80 84 85		 % % % % % % %	
9	Isolation Voltage (I/O)	V_{ISO}			1500	V_{PK}	Impulse Test

Note 1: Typical figures are at 25°C with a nominal 48V supply and are for design aid only. Not Guaranteed
2: The output ripple and noise can be reduced with an external filter, see Section 5.8.

12. Package

12.1 SIL Package



12.2 SIL Plan View

The shaded section shows the external component keep-out area around the module.