AiP16C23
Ram Mapping 56 SEG/4 COM or 52 SEG/8 COM LCD Controllers with 2-line Serial Interface

Product Specification

Specification Revision History:

Version	Date	Description
2021-04-A1	2021-04	New

1、General Description

AiP16C23 is a standard I^2C interface communication LCD controller/driver. The device provides two display modes: 1/4 duty and 1/8 duty display modes. The display segments of the device are 224 patterns (56×4) or 416 patterns (52×8).

AiP16C23 has a built-in clock generator, LCD bias voltage generation module, LCD drive voltage follower and standard I^2C interface.

Features:

- Operating voltage: 2.4 to 5.5V
- I^2C interface
- Low power consumption
- Versatile blinking modes
- Read/Write address auto increment
- Internal 32kHz RC oscillator
- 16-step V_{LCD} voltage adjustable
- Display patterns:
  56×4 patterns: 56 SEGs and 4 COMs
  52×8 patterns: 52 SEGs and 8 COMs
- Bias: 1/3 or 1/4; duty: 1/4 or 1/8
- 52×8 bit display data register
- Internal LCD bias generator with voltage follower
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- LCD drive voltage can be adjusted by external resistor
- Packaging information: LQFP48/LQFP64

Ordering Information:

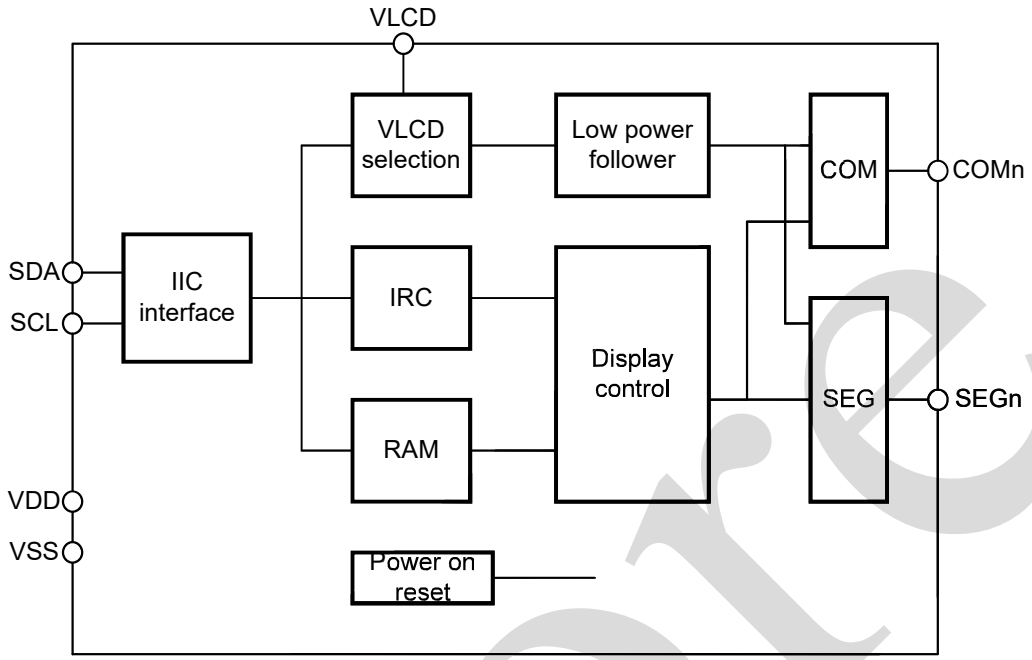
Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
AiP16C23LA.TB	LQFP48	AiP16C23	250 PCS/plate	10 plate/box	2500 PCS/box	6 box/pack	15000 PCS/pack	Dimensions of plastic enclosure: 7.0mm×7.0mm Pin spacing: 0.5mm
AiP16C23LB.TB	LQFP64	AiP16C23	250 PCS/plate	10 plate/box	2500 PCS/box	6 box/pack	15000 PCS/pack	Dimensions of plastic enclosure: 7mm×7mm Pin spacing: 0.4mm

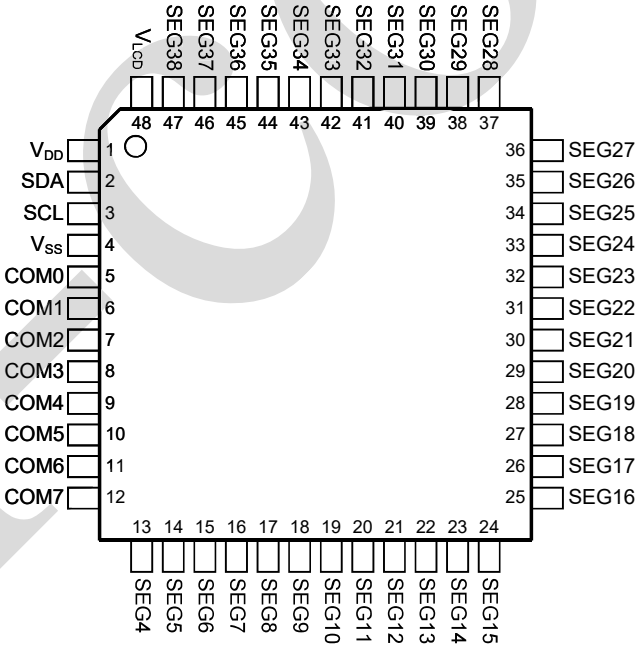
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

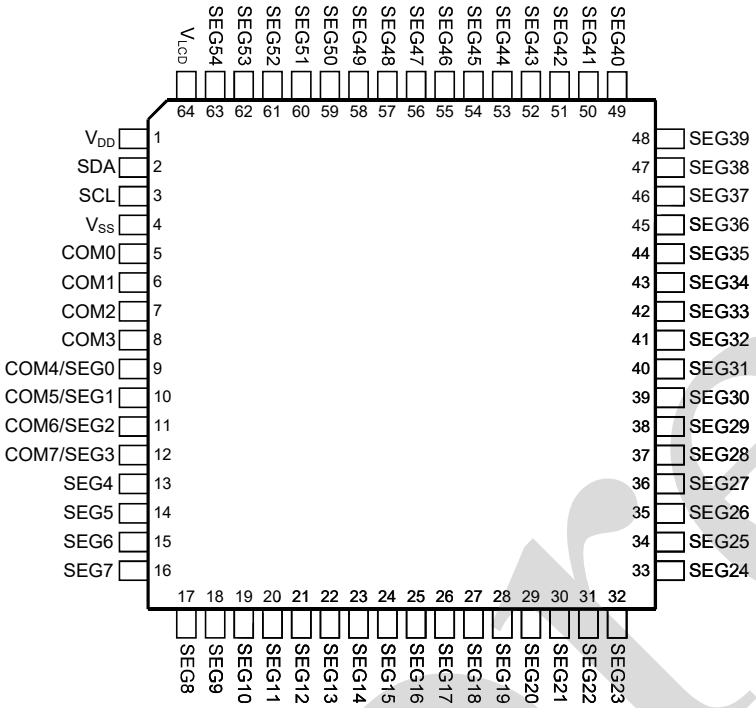
2.1、Block Diagram



2.2、Pin Configurations



LQFP48



LQFP64

Note:

1. Application at $V_{DD} \leq V_{LCD}$ or $V_{LCD} \leq V_{DD}$.
2. When the LQFP48 package is selected, this device does not support LCD 1/4 duty.

2.3、Pin Description

Pin No.		Pin Name	Type	Description
LQFP48	LQFP64			
2	2	SDA	I/O	Serial data input/output for I^2C interface
3	3	SCL	I	Serial clock input for I^2C interface
1	1	V_{DD}	-	Positive power supply
4	4	V_{SS}	-	Negative power supply, ground
48	64	V_{LCD}	-	LCD drive power
5~8	5~8	COM0~COM3	O	LCD COM outputs
9~12	-	COM4~COM7	O	LCD COM outputs
-	9~12	COM4/SEG0~COM7/SEG3	O	LCD COM/SEG multiplexed driver outputs
13~47	13~47	SEG4~SEG38	O	LCD SEG outputs
-	48~63	SEG39~SEG54	O	LCD SEG outputs

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
supply voltage	-	-	V_{SS}-0.3 to V_{SS}+6.5	V
input voltage	V_{IN}	-	V_{SS}-0.3 to V_{DD}+0.3	V
operating temperature	T_{amb}	-	-40 to +85	℃
storage temperature	T_{stg}	-	-55 to +150	℃

3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(T_{amb}=-40 to +85℃, V_{DD}=2.4 to 5.5V, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
operating voltage	V_{DD}	-	-	2.4	-	5.5	V
operating voltage	V_{LCD}	-	-	2.4	-	5.5	V
operating current	I_{DD}	3V	no load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to "0000"	-	25	40	uA
		5V		-	35	50	uA
operating current	I_{DD1}	3V	no load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display off, internal system oscillator on, DA0~DA3 are set to "0000"	-	2	5	uA
		5V		-	4	10	uA
standby curent	I_{STB}	3V	o load, V_{LCD}=V_{DD}, LCD display off, internal system oscillator off	-	-	1	uA
		5V		-	-	2	uA
HIGH level intput current	V_{IH}	-	SDA, SCL	0.7V_{DD}	-	V_{DD}	V
LOW level intput current	V_{IL}	-	SDA, SCL	0	-	0.3V_{DD}	V
input leakage curent	I_{IL}	-	V_{IN}=V_{SS} or V_{DD}	-1	-	1	uA
LOW level output current	I_{OL}	3V	V_{OL}=0.4V, SDA	3	-	-	mA
		5V		6	-	-	mA
LCD COM sink current	I_{OL1}	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	-	uA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	-	uA
LCD COM source current	I_{OH1}	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	-	uA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	-	uA
LCD SEG sink current	I_{OL2}	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	-	uA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	-	uA

LCD SEG source current	I_{OH2}	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	-	uA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	-	uA

3.2.2、AC Characteristics 1

(T_{amb}=-40 to +85℃, V_{DD}=2.4 to 5.5V, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
LCD frame frequency	f_{LCD1}	4V	1/4 duty, T_{amb}=+25℃	72	80	88	Hz
LCD frame frequency	f_{LCD2}	4V	1/4 duty, T_{amb}=+25℃	144	160	176	Hz
LCD frame frequency	f_{LCD3}	4V	1/4 duty, T_{amb}=-40 to +85℃	52	80	124	Hz
LCD frame frequency	f_{LCD4}	4V	1/4 duty, T_{amb}=-40 to +85℃	104	160	248	Hz
V_{DD} off time	t_{OFF}	-	V_{DD} drop down to 0V	20	-	-	ms
V_{DD} slew rate	t_{SR}	-	-	0.05	-	-	V/ms

Note:

1. During the power on/off period, if the conditions of the power-on reset sequence are not met, the internal power-on reset (POR) circuit cannot work normally.
2. During operating, if the V_{DD} voltage drops below the specified minimum operating voltage, the power-on reset sequence conditions must be satisfied. In other words, the V_{DD} voltage must drop to 0V and must maintain a 0V voltage of at least 20ms before rising to the normal operating voltage.

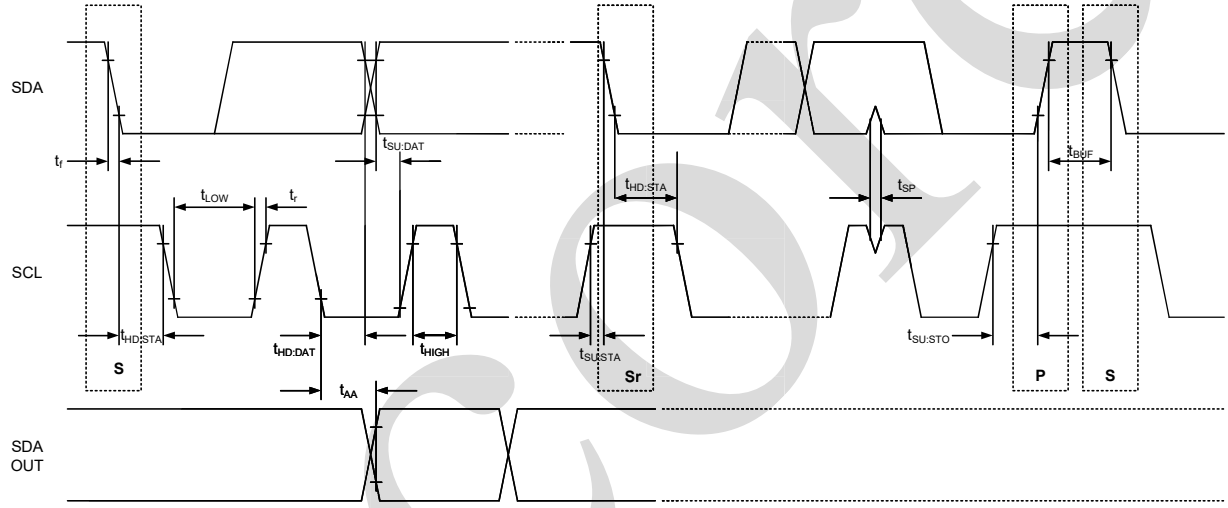
3.2.3、AC Characteristics 2 (I^2C Interface)

Parameter	Symbol	Conditions	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
clock frequency	f_{SCL}	-	-	100	-	400	kHz
bus free time	t_{BUF}	during this period the bus must be free until a new transmission starts	4.7	-	1.3	-	us
Start condition hold time	$t_{HD: STA}$	after this period, the first clock pulse is generated	4	-	0.6	-	us
SCL LOW time	t_{LOW}	-	4.7	-	1.3	-	us
SCL HIGH time	t_{HIGH}	-	4	-	0.6	-	us
Start condition setup time	$t_{SU: STA}$	only relevant for repeated START condition	4.7	-	0.6	-	us
data hold time	$t_{HD: DAT}$	-	0	-	0	-	ns
data setup time	$t_{SU: DAT}$	-	250	-	100	-	ns

SDA and SCL rise time	t_R	-	-	1	-	0.3	us
SDA and SCL fall time	t_F	-	-	0.3	-	0.3	us
Stop condition setup time	$t_{SU: STO}$	-	4	-	0.6	-	us
effective clock output time	t_{AA}	-	-	3.5	-	0.9	us
input filter time constant (SDA, SCL)	t_{SP}	noise suppression time	-	100	-	50	ns

4、Timing Diagrams

4.1、I²C Timing



4.2、Power-on Reset Timing

5、Function Description

5.1、Power-on Reset

After power-on, the device is initialized by the internal power-on reset circuit. The state of the internal circuit after initialization is as follows:

- The drive mode 1/4 duty output and 1/3 bias is selected for LQFP64 package.
- The drive mode 1/4 duty output and 1/3 bias is selected for LQFP48 package.
- Both the system oscillator and LCD bias generator are off state.
- The LCD display is off sate.
- The internal voltage adjustment function is enabled.
- The SEG/V_{LCD} shared pin is set to SEG pin.
- The detection switch function of the V_{LCD} pin is disabled.
- The frame frequency is set to 80Hz.
- The blinking function is switched off.

After power-on, Data transfers on the I^2C bus within 1ms should be avoided to complete the reset action.

5.2、Display Memory—RAM Structure

AiP16C23 has a 52×8-bit static RAM for storing LCD display data. Write "1" to it to turn on the corresponding LCD, and write "0" to turn off the corresponding LCD.

The contents of the RAM data are directly mapped to the LCD. The SEGs in the first column of RAM operate together with their corresponding COM0. In multiplexed LCD applications, SEGs in columns 2, 3, and 4 are time-multiplexed with their corresponding COM1, COM2, and COM3, respectively. The mapping relationship between RAM data and LCD pattern is as follows:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55					SEG54					1BH
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM mapping of 56×4 display mode

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	Address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55									33H
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM mapping of 52×8 display mode

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Display data transfer format for I^2C interface

5.3、Address Pointer

Display RAM addressing technology is realized by address pointer. This mechanism allows single or multiple display data bytes to be loaded at any location in the display RAM. The address pointer sequence is initialized by the address pointer command.

5.4、System Oscillator

The internal oscillator provides timing for the internal logic and LCD drive signals. The system clock frequency (f_{SYS}) determines LCD frame frequency. During the system power-on initialization, the system oscillator will be in the stop state.

5.5、Frame Frequency

The AiP16C21 provides two frame frequencies, which can be selected by the mode setting command to be 80Hz or 160Hz.

5.6、Blinker Function

The device contains versatile blinking modes. The whole display can be blinked at frequencies selected by blink command. The ratio between the system frequency and the blinking frequency depends on the blinking mode, as shown in the following table:

Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	闪烁关闭
1	f_{SYS}/16384Hz	2
2	f_{sys}/32768Hz	1
3	f_{sys}/65536Hz	0.5

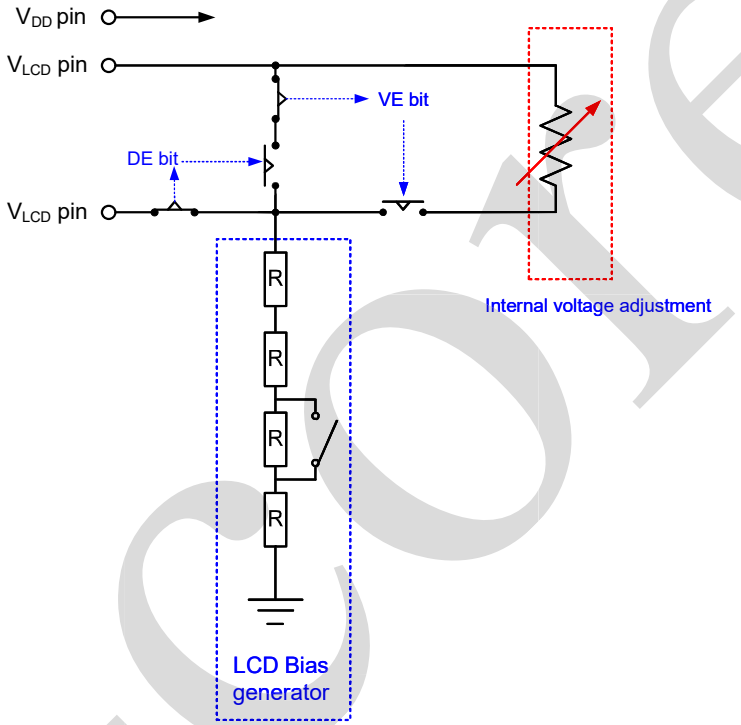
5.7、LCD Bias Generator

LCD full voltage (V_{OP}) comes from (V_{LCD}-V_{SS}). The LCD voltage can be externally compensated for temperature through the voltage provided by the V_{LCD} pin.

1/3 or 1/4 bias voltage can be obtained from an internal voltage divider of four series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of circuits to provide a 1/3 bias voltage.

5.8、Internal V_{LCD} Voltage Adjustment

- The internal V_{LCD} adjustment contains four series resistors and a 4-bit programmable analog switch which can provide 16-level voltage adjustment options using the V_{LCD} voltage adjustment command.
- The internal V_{LCD} adjustment as shown below:



When DE=1, VE=1:

Bias / DA3~DA0	1/3	1/4	Note
00H	1.000×V_{LCD}	1.000×V_{LCD}	default value
01H	0.944×V_{LCD}	0.957×V_{LCD}	
02H	0.894×V_{LCD}	0.918×V_{LCD}	
03H	0.849×V_{LCD}	0.882×V_{LCD}	
04H	0.808×V_{LCD}	0.849×V_{LCD}	
05H	0.771×V_{LCD}	0.818×V_{LCD}	
06H	0.738×V_{LCD}	0.789×V_{LCD}	
07H	0.707×V_{LCD}	0.763×V_{LCD}	
08H	0.678×V_{LCD}	0.738×V_{LCD}	
09H	0.652×V_{LCD}	0.714×V_{LCD}	
0AH	0.628×V_{LCD}	0.692×V_{LCD}	
0BH	0.605×V_{LCD}	0.672×V_{LCD}	
0CH	0.584×V_{LCD}	0.652×V_{LCD}	
0DH	0.565×V_{LCD}	0.634×V_{LCD}	
0EH	0.547×V_{DD}	0.616×V_{DD}	
0FH	0.529×V_{DD}	0.600×V_{DD}	

5.9、SEG Drive Output

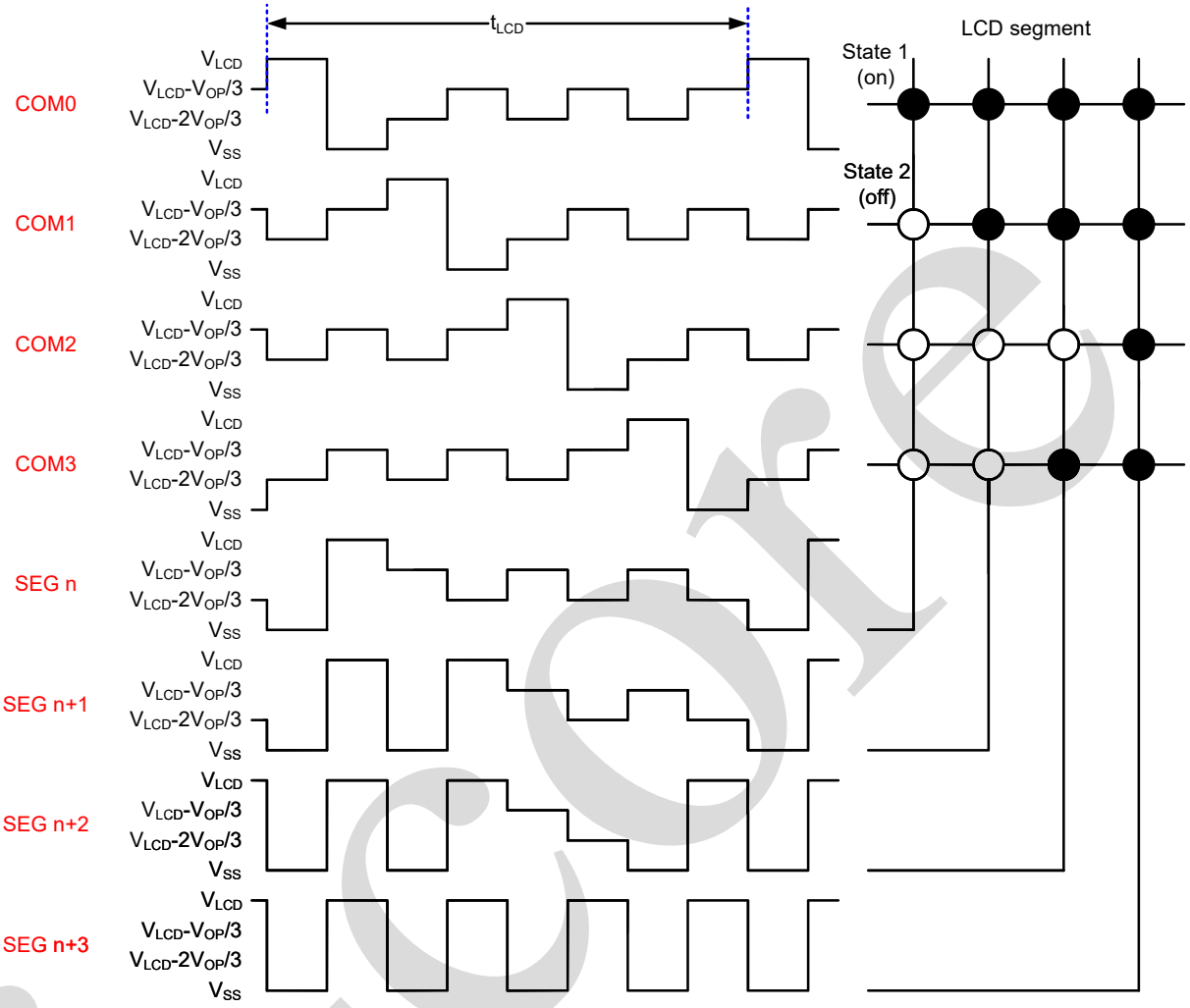
The LCD drive module contains 56 SEG outputs SEG0~SEG55 or 52 SEG outputs SEG4~SEG55, these SEGs should be directly connected to the LCD panel. The SEG output signals are generated according to the multiplexed COM signals and the data in the display latch. If the number of SEG used is less than 56 or 52, the unused SEG outputs should be left open-circuit.

5.10、COM Drive Output

The LCD drive section contains 4 COM outputs (COM0~COM3) or 8 COM outputs (COM0~COM7). These COMs should be directly connected to the LCD panel. The COM output signals are generated according to the selected LCD drive mode. If the number of COMs used is less than 4 or 8, the unused COM output should be left open-circuit.

5.11、LCD Drive Mode Waveforms

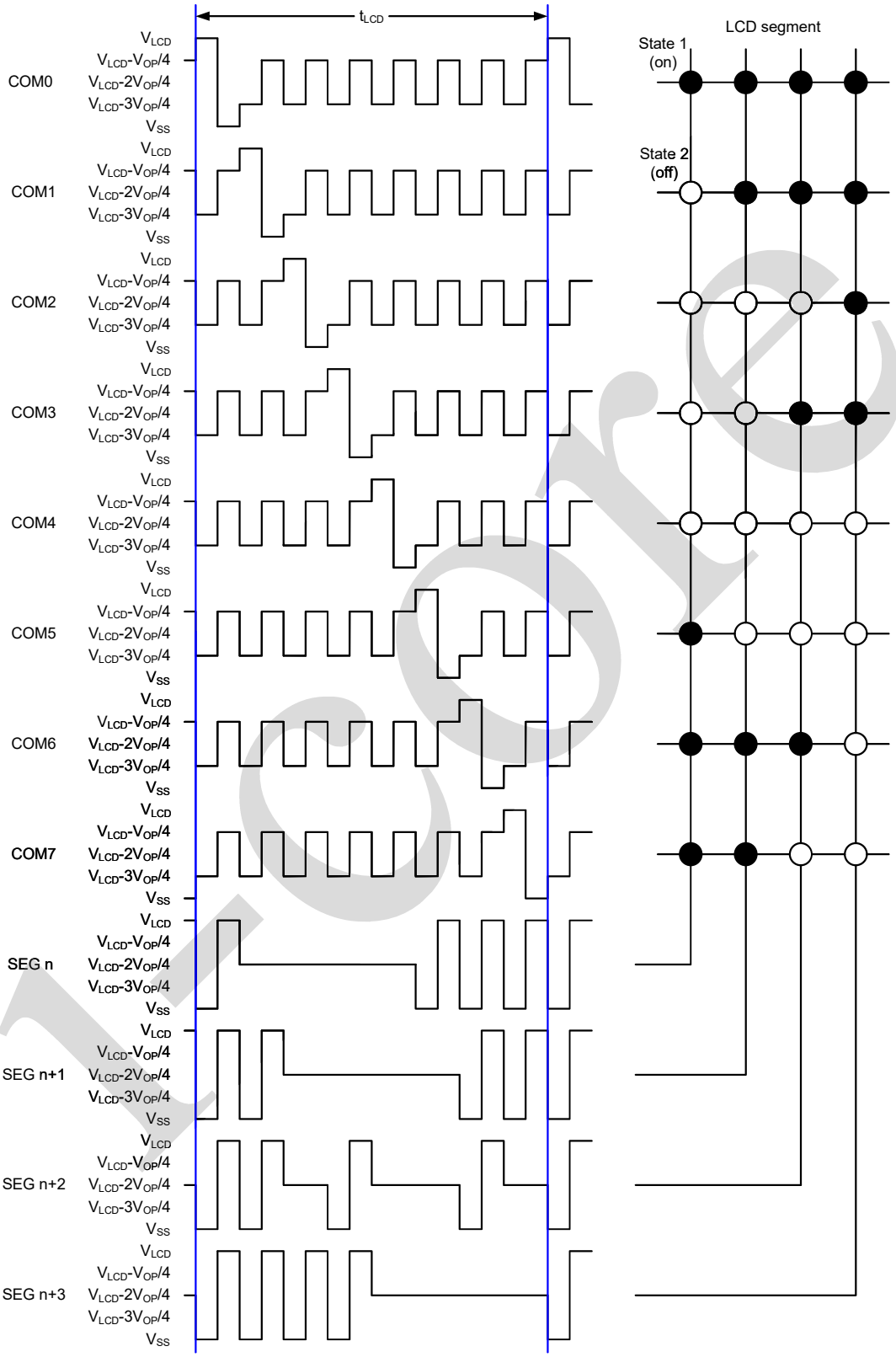
● When the LCD drive mode selects 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



1/4 duty and 1/3 bias drive mode waveform ($V_{OP}=V_{LCD}-V_{SS}$)

Note: $t_{LCD}=1/f_{LCD}$

● When the LCD drive mode selects 1/8 duty and 1/4 bias, the waveform and LCD display is shown as follows:



1/8 duty and 1/4 bias drive mode waveform (V_{OP}=V_{LCD}-V_{SS})

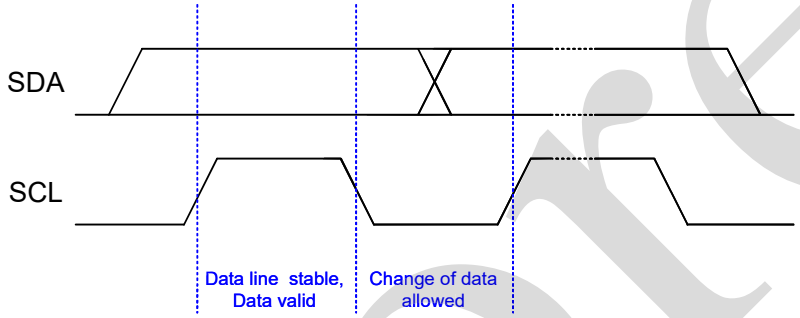
Note: t_{LCD}=1/f_{LCD}

5.12、I²C Serial Interface

The device provides I²C serial interface, and the device is only used as a slave for I²C communication. The I²C interface is for bidirectional, two-line communication between different ICs or modules, that is, a serial data line SDA and a serial clock line SCL. These two lines are respectively connected to the positive power supply through a pull-up resistor with a typical value of 4.7KΩ. When the I²C bus is free, both lines are HIGH. The microcontroller connected to the I²C interface must have an open-drain or open-collector output to realize the wired-or function. Data transmission starts only when the I²C interface is not busy.

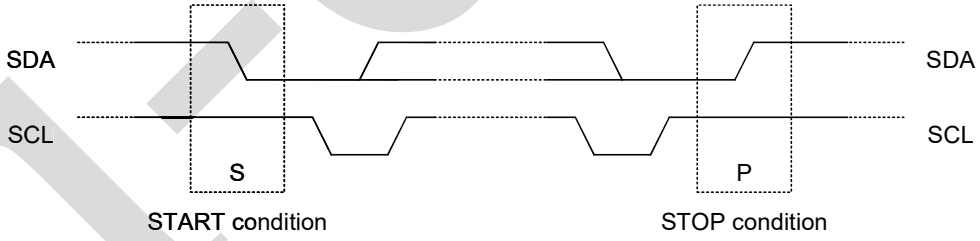
5.13、Data Validity

When SCL=1, the data on the SDA pin must be stable. Only when SCL=0, the level of the SDA pin will change, as shown in the diagram below:



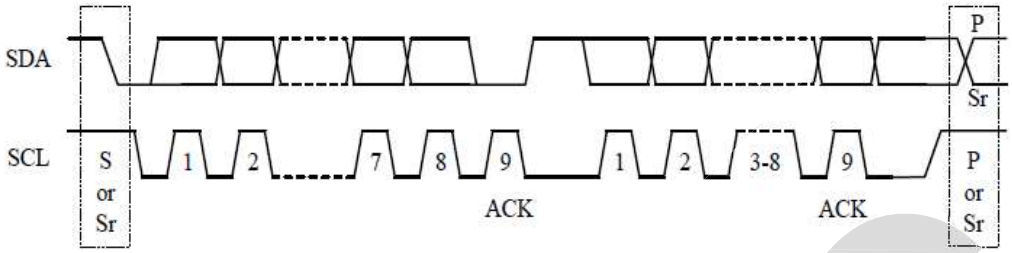
5.14、START And STOP Conditions

- When SCL=1, a high to low transition on the SDA line defines a START condition.
- When SCL=1, a low to high transition on the SDA line defines a STOP condition.
- START and STOP conditions are always generated by the master. The I²C interface is considered to be busy after the START condition. The I²C interface is considered to be free again a certain time after the STOP condition.
- The I²C interface stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START and repeated START (Sr) conditions are functionally identical.



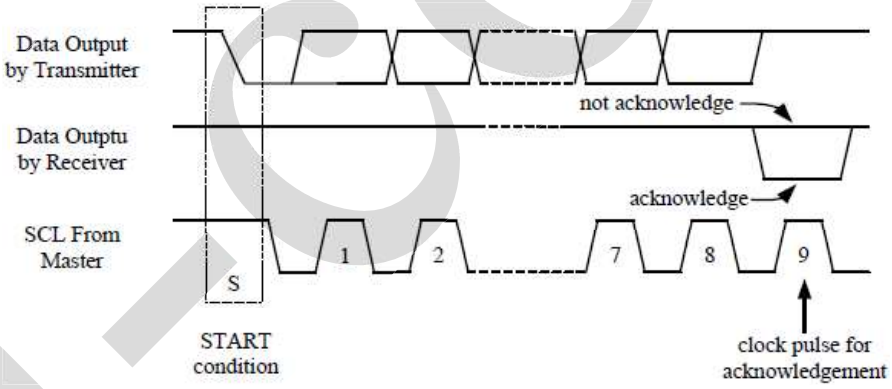
5.15、Byte Format

Every byte on the SDA line must be 8-bit long. The number of bytes that can be transmitted at a time is unlimited. Each byte has to be followed by an acknowledge bit. Data transmission starts from the highest bit.



5.16、Acknowledge (ACK)

- Each bytes of eight bits is followed by one acknowledge bit. This acknowledge bit is a LOW level placed on the I^2C interface by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the receiving each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.
- A master receiver generates a not-acknowledge (NACK) when the slave sends the last byte and has told the slave to end data transmission. In this case, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



5.17、Slave Addressing

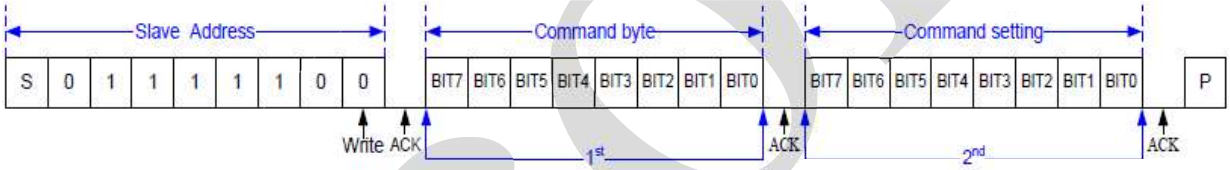
- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. When the R/$\overline{W}$ bit is "0", then a write operation is selected.
- AiP16C23 address bit is "0111110". When an address byte is sent, the device compares with its internal address. If they match, the device outputs an acknowledge on the SDA line.

5.18、Write Operation

5.18.1、Byte Writes Operation

- **Command Byte**

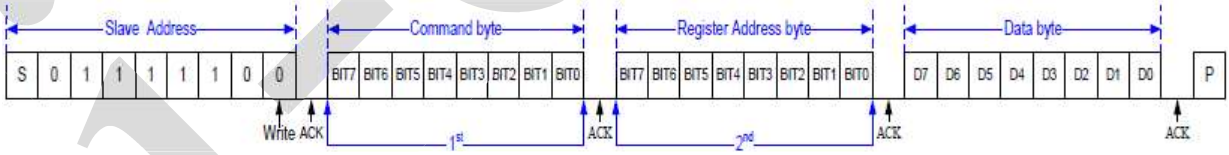
A Command Byte write operation consists of a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a command setting byte and a STOP condition.



Command Byte Write Operation

- **Display RAM Single Data Byte**

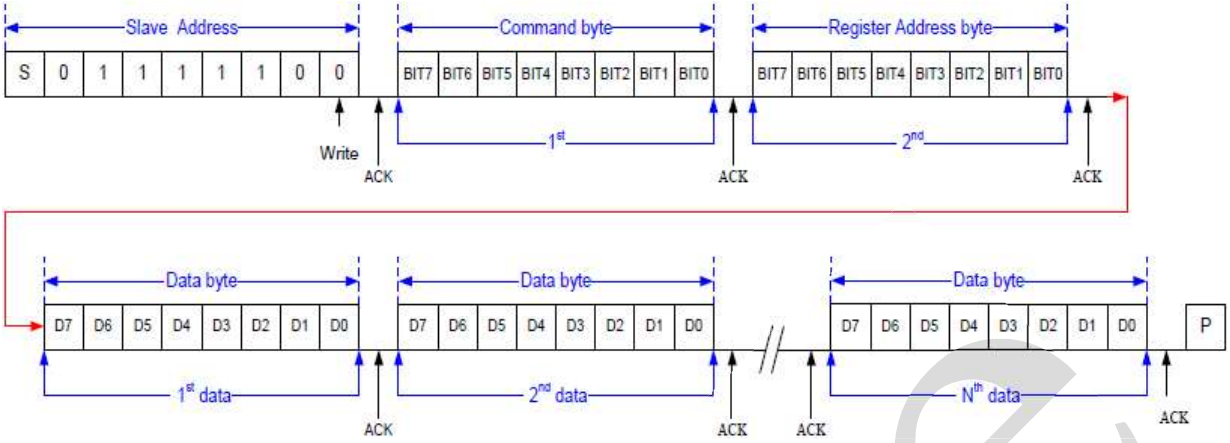
A display RAM data byte write operation consists of a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a valid Register Address byte, a Data byte and a STOP condition.



Display RAM Single Data Byte Write Operation

5.18.2、Display RAM Page Write Operation

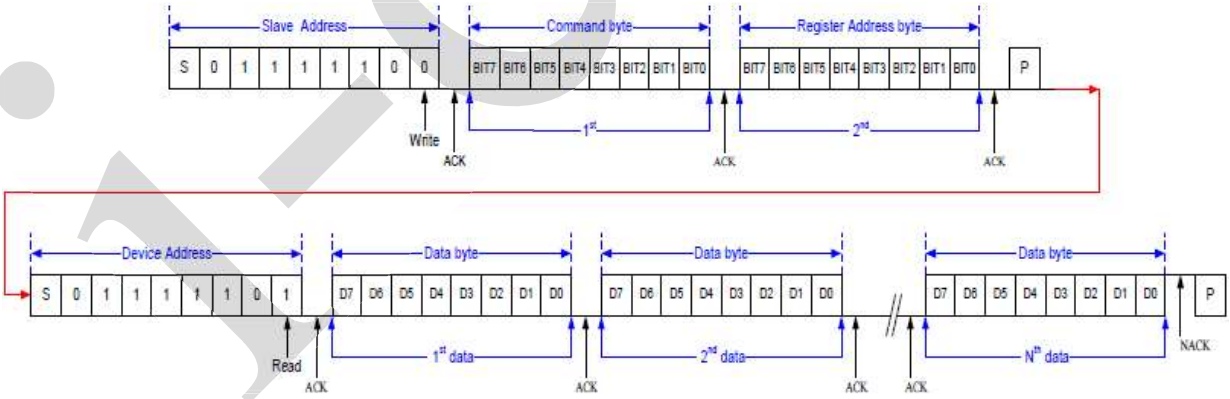
After a START condition the slave address with the R/$\overline{W}$ bit is sent to the I^2C interface followed with a command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the address pointer will be automatically incremented by 1, so it can write to the next address after receiving an acknowledge. After the internal address pointer reaches the maximum address, which is 1BH for 1/4 duty drive mode or 33H for 1/8 duty drive mode, the address pointer will be reset to 00H.



N Bytes Display RAM Data Write Operation

5.19、Display RAM Read Operation

- In this mode, the master reads the AiP16C23 data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After configuring the start address of the Read Operation, another START condition and the slave address are transferred on the I^2C interface followed by the R/$\overline{W}$ bit ("1"). Then the MSB of the data which was addressed is transmitted first on the I^2C interface. The address pointer is incremented by 1 after the receiving an acknowledge. That means that if the device sends the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum address, which is 1BH for 1/4 duty drive mode or 33H for 1/8 duty drive mode, the address pointer will be reset to 00H.
- The cycle of reading consecutive addresses will continue until the master sends a STOP condition.



5.20、Command Summary

- **Display Data Input Command**

This command is used to send data from MCU to memory map of the AiP16C23.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
display data input/ output command	1st	1	0	0	0	0	0	0	0	-	W	-
address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address of memory map	W	00H

Note:
- Power on status: The address is set to 00H.
- If the command is not defined, the function will not be affected.
- For 1/4 duty drive mode, if the address pointer reaches 1BH, the pointer will reset to 00H.
- For 1/8 duty drive mode, if the address pointer reaches 33H, the pointer will reset to 00H.

- **Drive Mode Command**

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
Drive mode setting command	1st	1	0	0	0	0	0	1	0	-	W	-
Duty and bias setting	2nd	X	X	X	X	X	X	Duty	Bias	No matter what "Duty" bit is set, 1/8 duty drive mode is only available for LQFP48.	W	00H

Note:

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

- Power on status: The drive mode 1/4 duty output and 1/3 bias is selected.
- If the command is not defined, the function will not be affected.

- **System Mode Command**

This command controls the internal system oscillator on/off and display on/off.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0	-	W	-
System oscillator and display on/off control	2nd	X	X	X	X	X	X	S	E	-	W	00H

Note:

Bit 1	Bit 0	Internal System Oscillator	LCD Display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

- Power on status: Display off and disable the internal system oscillator.
- If the command is not defined, the function will not be affected.

- **Frame Frequency Command**

This command selects the frame frequency.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
frame frequency command	1st	1	0	0	0	0	1	1	0	-	W	-
frame frequency setting	2nd	X	X	X	X	X	X	X	F	-	W	00H

Note:

Bit 0	Frame Frequency
F	
0	80Hz
1	160Hz

- Power on status: Frame frequency is 80Hz.
- If the command is not defined, the function will not be affected.

- **Blinking Frequency Command**

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
blinking frequency command	1st	1	0	0	0	1	0	0	0	-	W	-
blinking frequency setting	2nd	X	X	X	X	X	X	BK1	BK0	-	W	00H

Note:

Bit 1	Bit 0	Blinking Frequency
BK1	BK0	
0	0	Blinking off
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power on status: Blinking function is switched off.
- If the command is not defined, the function will not be affected.

- **Internal Voltage Adjustment (IVA) Setting Command**

The internal voltage (V_{LCD}) can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
IVA setting	1st	1	0	0	0	1	0	1	0	-	W	-
IVA control	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	● SEG/V_{LCD} shared pin can be set via the "DE" bit. ● The "VE" bit is used to enable or disable the internal voltage adjustment. ● The DA3~DA0 bits can be used to adjust the V_{LCD} output voltage.	W	30H

Note:

Bit 5	Bit 4	SEG/V_{LCD} Shared Pin Select	Internal Voltage Adjustment	Note
DE	VE			
0	0	Analog power supply LCD drive bias	off	● The LCD drive voltage is input from the external to the V_{LCD} pin. ● Disable the internal voltage adjustment function ● DA3~DA0 bit must be set as "0000". ● The V_{LCD} pin and the V_{DD} pin connect to use. ● It can be use, but it is not recommended to use the scheme of connecting a resistor between the V_{LCD} pin and the V_{DD} pin.
0	1	Analog power supply LCD drive bias	on	
1	0	Analog power supply LCD	off	● The LCD drive voltage is input from the external to the V_{LCD} pin. ● Disable the internal voltage adjustment function.

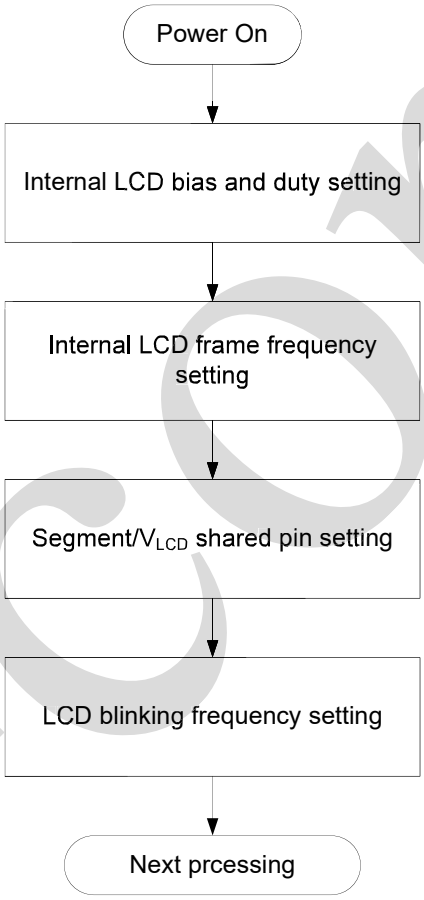
		drive bias		● DA3~DA0 can be any value.
1	1	Analog power supply LCD drive bias	on	● The LCD drive voltage is input from the external to the V_{LCD} pin. ● Enable the internal voltage adjustment function. ● DA3~DA0 can be any value.

● Power on status: Disable the internal voltage adjustment and the SEG/V_{LCD} pin is set as the SEG pin.
● When the DA0~DA3 bits are set to "0000", the internal voltage-follower (OP4) is disabled. When the DA0~DA3 bits are set to other values except "0000", the internal voltage follower (OP4) is enabled.
● If the command is not defined, the function will not be affected.

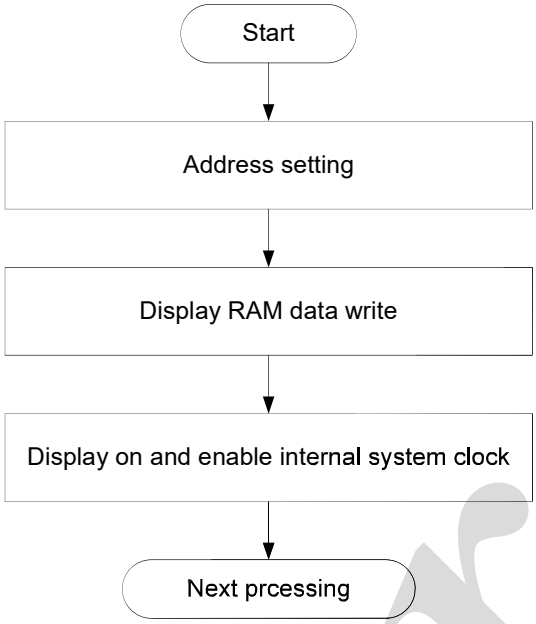
5.21、Operation Flow Chart

The flow charts of the access procedures are shown below.

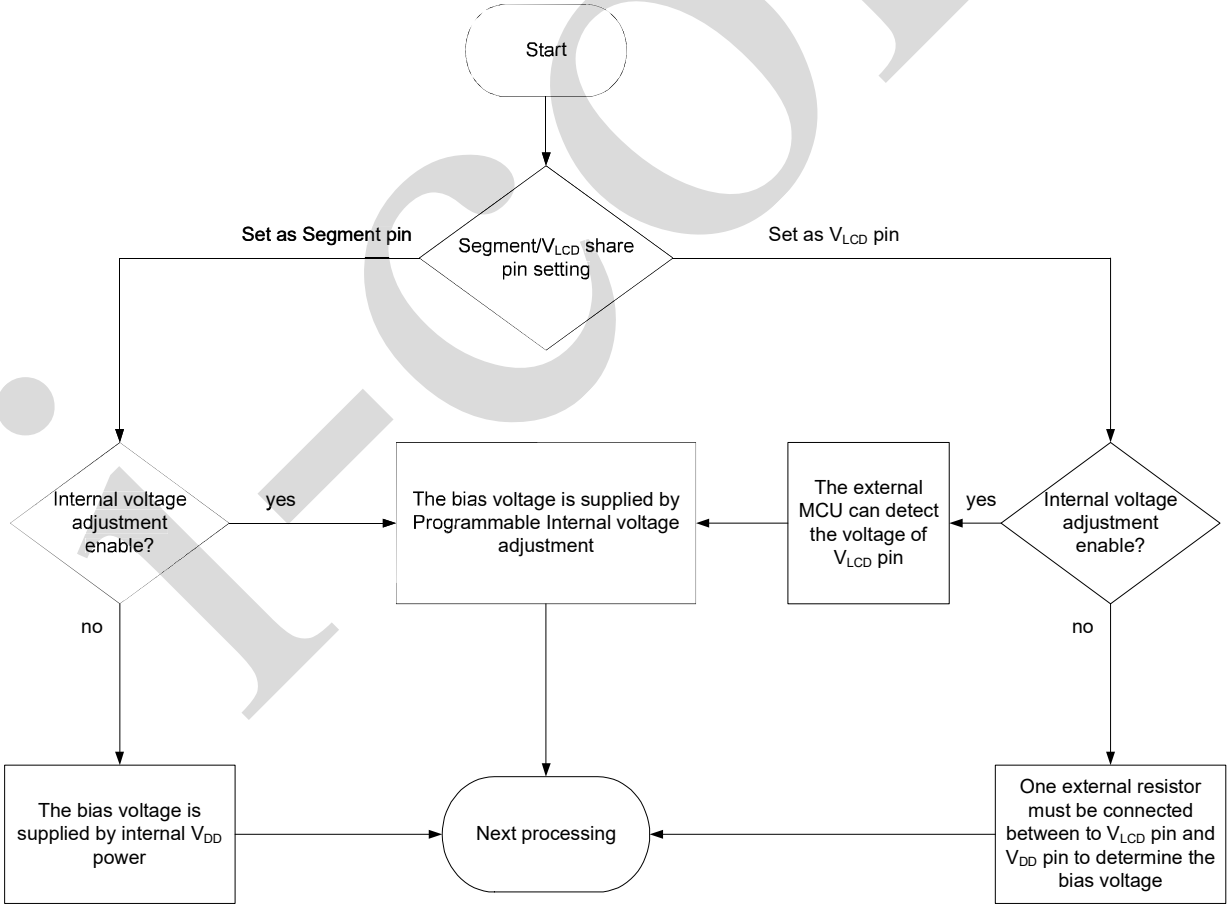
- **Initialization**



- **Display Data Read/Write (Address Setting)**



- **SEG/V_{LCD} Shared Pin And Internal Voltage Adjustment Setting**



5.21、Power Supply Sequence

● If the LCD and V_{DD} pin are powered separately, it is strongly recommended to follow the power supply sequence requirements.

● Failure to follow the requirements of the power supply sequence may cause malfunctions.

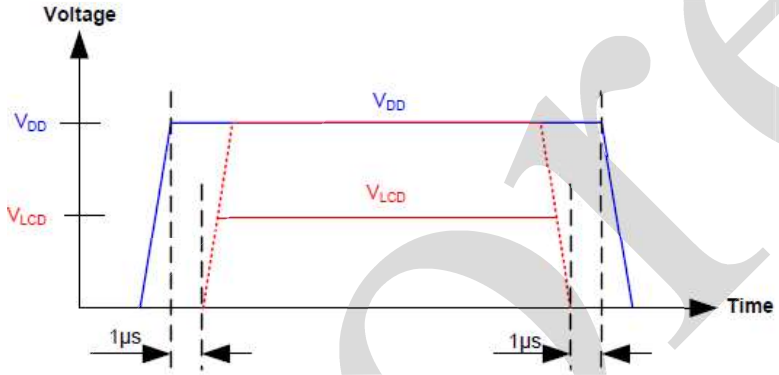
Power supply sequence requirements:

1. Power-on sequence: First turn on the logic power supply voltage V_{DD}, then turn on the LCD drive voltage V_{LCD}.

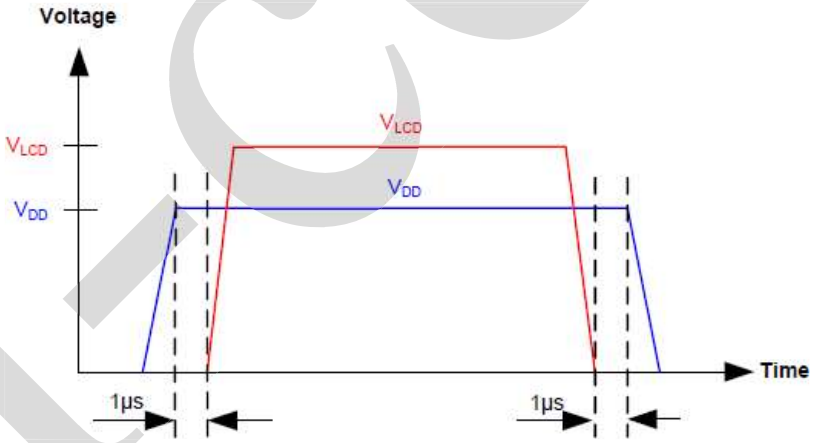
2. Power-off sequence: First turn off the LCD drive voltage V_{LCD}, then turn off the logic power supply voltage V_{DD}.

3. Regardless of whether the V_{LCD} voltage is higher than the V_{DD} voltage, the power supply sequence must be followed.

● $V_{LCD} \leq V_{DD}$:



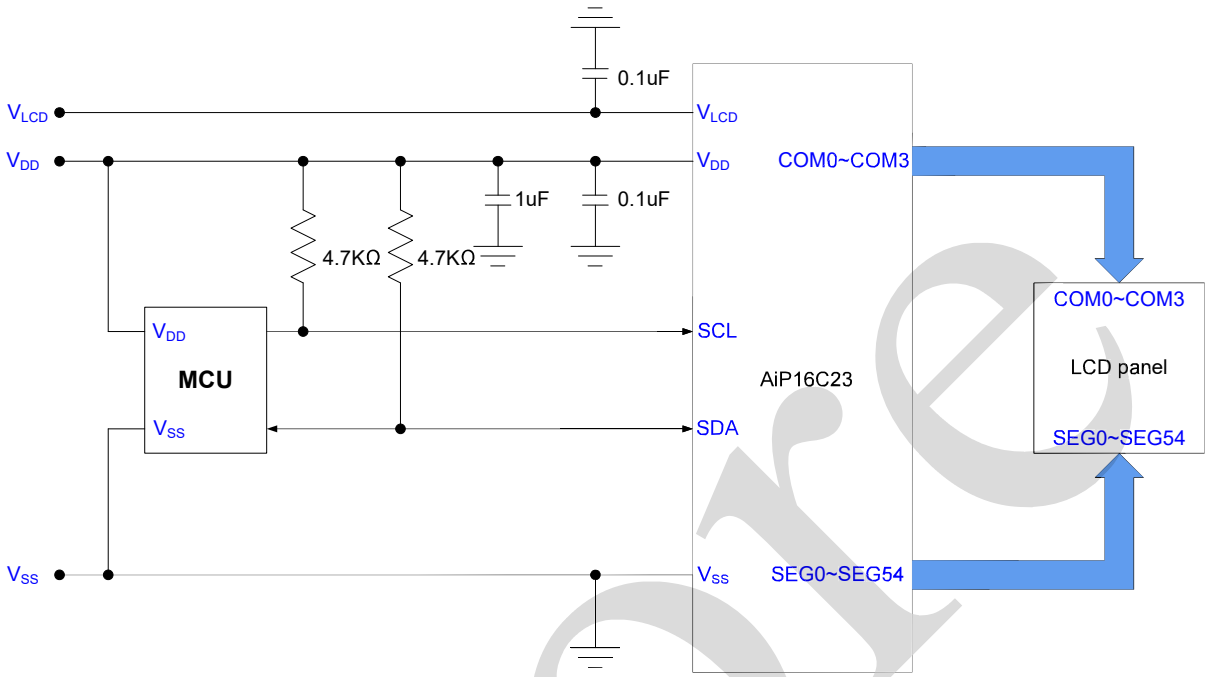
● $V_{LCD} > V_{DD}$:



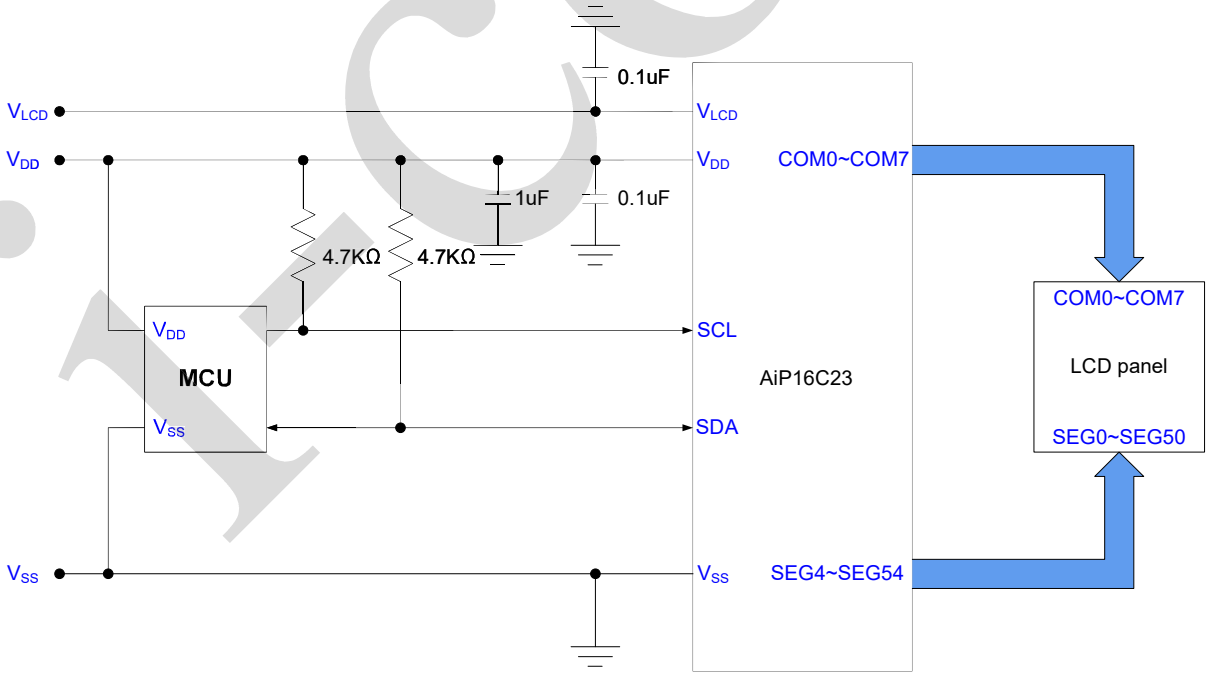
6、Typical Application Circuit And Application Note

6.1、64-pin package

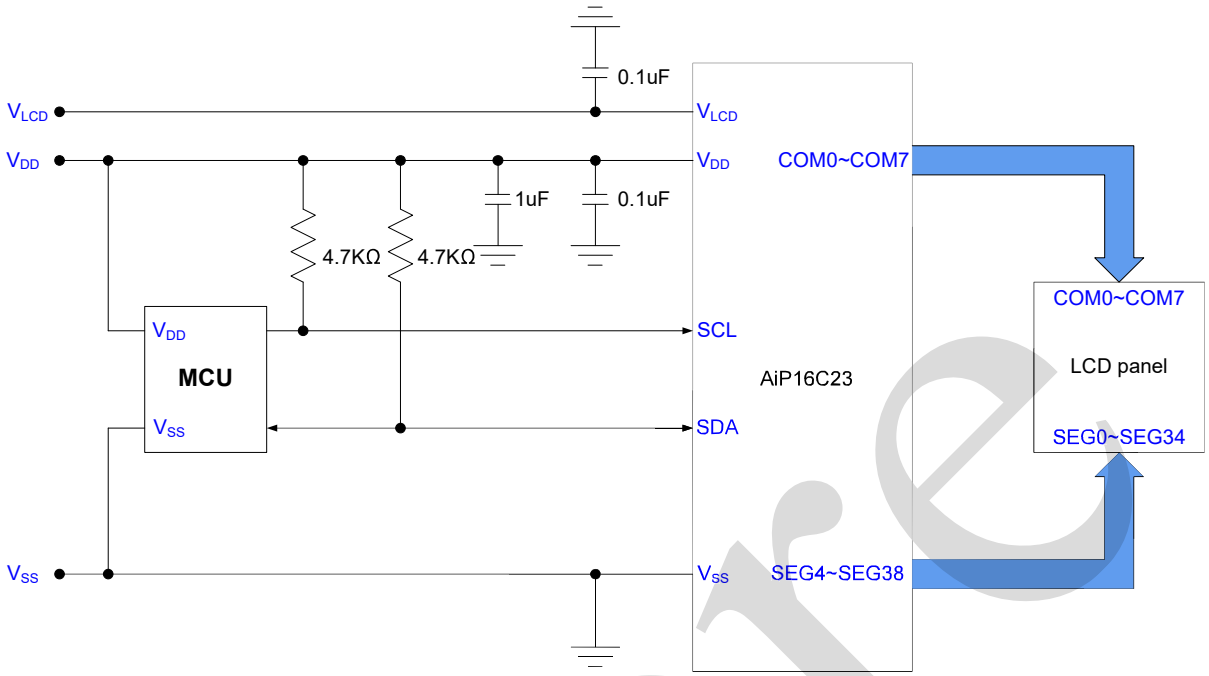
- **1/4 Duty**



- **1/8 Duty**

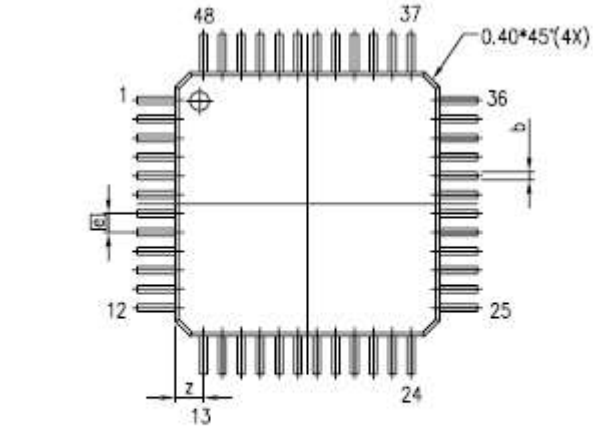


6.2、48-pin package (the 48 pin package supports LCD 1/8 duty only)

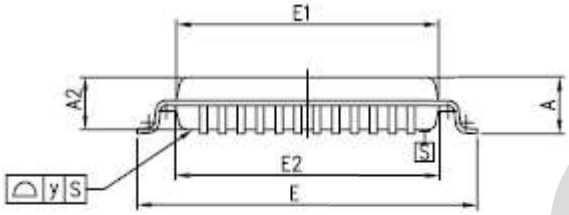


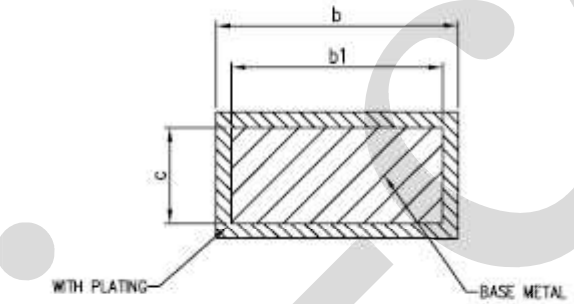
7、Package Information

7.1、LQFP48

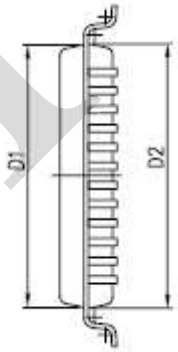


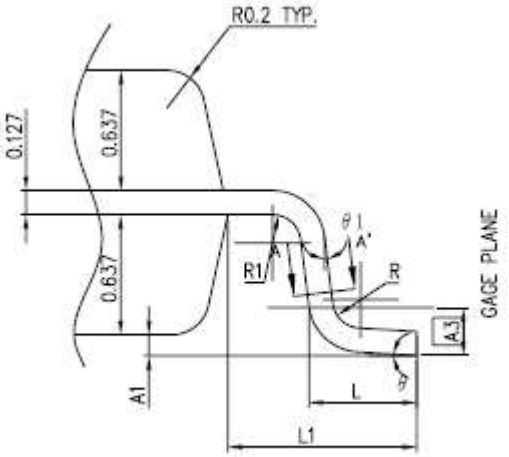
Symbol	Min	Nom	Max
A	----	----	1.63
A1	0.01	----	0.21
A2	1.30	1.40	1.50
A3	----	0.254	----
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
c	----	0.127	----
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	----	0.50	----
L	0.43	----	0.71
L1	0.90	1.00	1.10
R	0.1	----	0.25
R1	0.1	----	----
θ	0	----	10°
θ1	0	----	----
y	----	----	0.1
Z	----	0.75	----





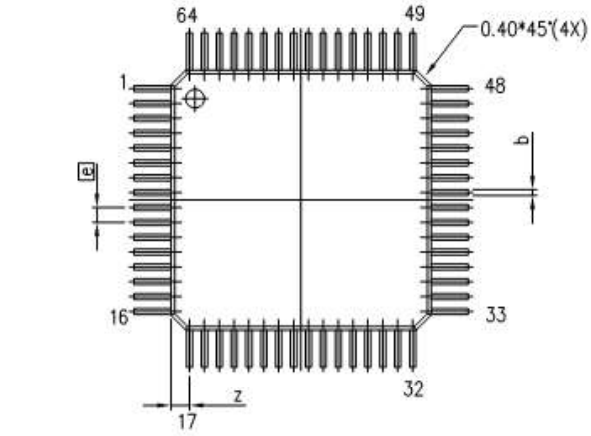
SECTION A–A'

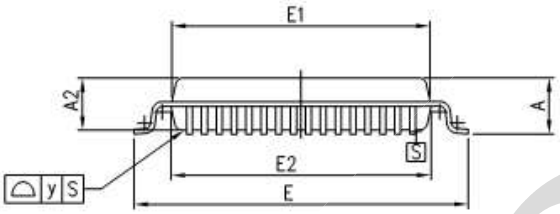


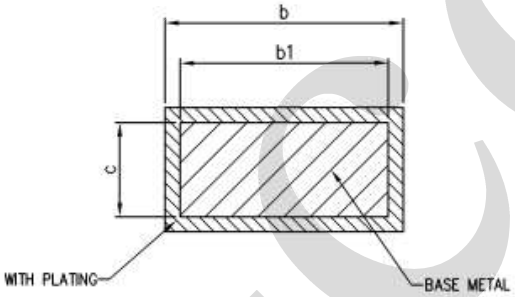


DETAIL A

7.2、LQFP64







Symbol	Min	Nom	Max
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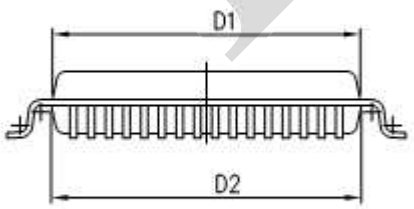
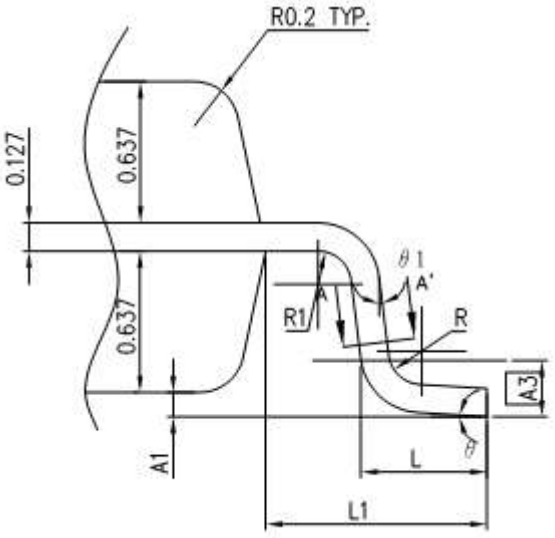
A1	0.01	----	0.21
A2	1.30	1.40	1.50
A3	----	0.254	----
b	0.14	0.19	0.24
b1	0.11	0.16	0.21
c	----	0.127	----
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	----	0.40	----
L	0.43	----	0.71
L1	0.90	1.00	1.10
R	0.1	----	0.25
R1	0.1	----	----
θ	0	----	10°
θ1	0	----	----
y	----	----	0.1
Z	----	0.5	----





8、Statements And Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.