



# AiP74HC/HCT595

## 8-bit Serial-in, Serial or Parallel-out Shift Register with Output Latches; 3-state

### Product Specification

#### Specification Revision History:

Version	Date	Description
2012-06-A1	2012-06	New
2021-09-A2	2021-09	Modify Ordering Information
2021-12-A3	2021-12	Modify Ordering Information
2022-01-A4	2022-01	Modify ambient temperature to $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ and add electrical characteristics of $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$
2022-08-A5	2022-08	Modify the tube packing specifications of SOP16/TSSOP16; Modify package information; Modify ambient temperature to $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
2022-09-A6	2022-09	Modify the value range of $V_{IL}$ ; delete notes; modify the value range of $f_{max}$ and the typical value of propagation delay when $V_{CC}=2\text{V}$ in the AC Characteristics 1; remove $C_{PD}$ ; remove the typical value of $f_{max}$



## 1、 General Description

The AiP74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset  $\overline{MR}$  input. A LOW on  $\overline{MR}$  will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ( $\overline{OE}$ ) is LOW. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### Features:

- Input levels:
  - For AiP74HC595: CMOS level
  - For AiP74HCT595: TTL level
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC595 DA16.TB	DIP16	74HC595	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT595 DA16.TB	DIP16	74HCT595	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC595 SA16.TB	SOP16	74HC595	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HCT595 SA16.TB	SOP16	74HCT595	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC595 TA16.TB	TSSOP16	74HC595	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT595 TA16.TB	TSSOP16	74HCT595	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

**Reel packing specifications:**

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC595SA16.TR	SOP16	74HC595	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HCT595SA16.TR	SOP16	74HCT595	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HC595TA16.TR	TSSOP16	74HC595	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
AiP74HCT595TA16.TR	TSSOP16	74HCT595	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

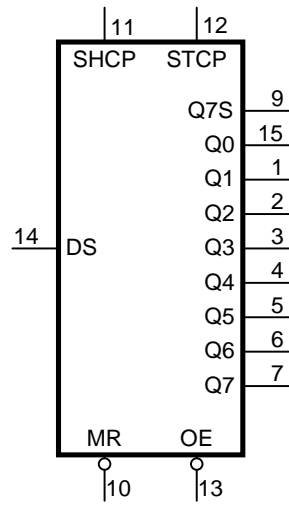


Figure 1. Logic symbol

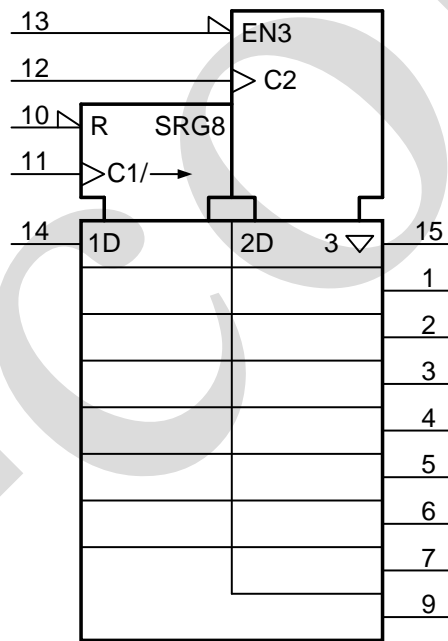


Figure 2. IEC logic symbol

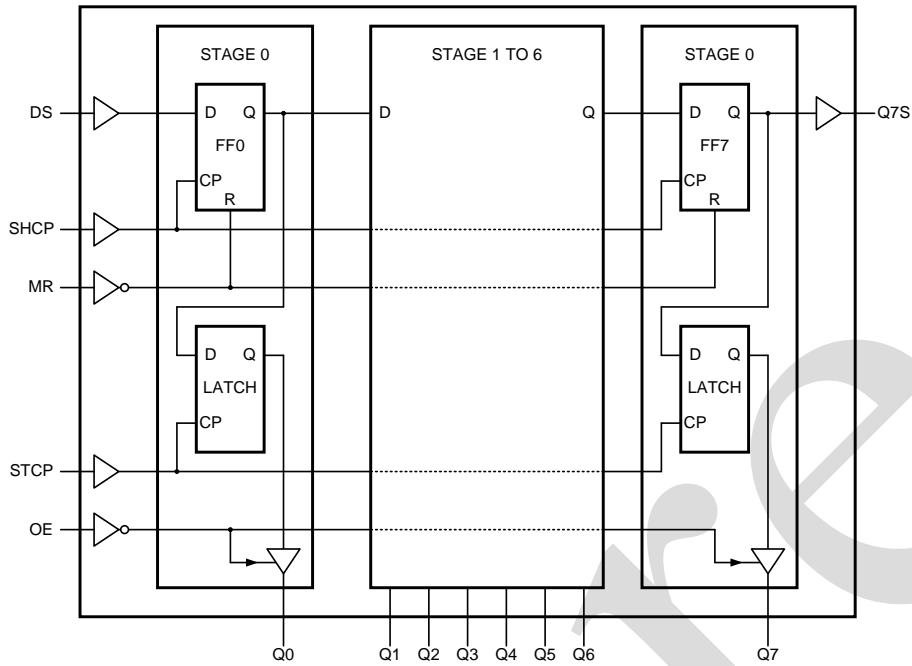


Figure 3. Logic diagram

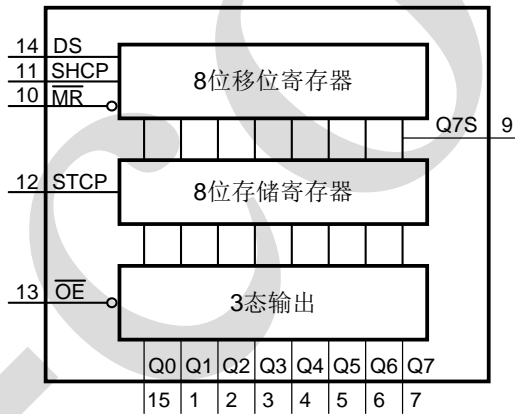
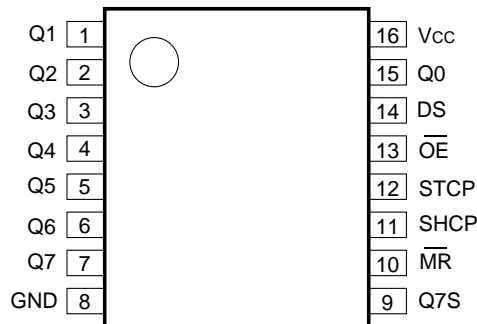


Figure 4. Functional diagram

## 2.2、Pin Configurations





## 2.3、Pin Description

Pin No.	Pin Name	Description
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0V)
9	Q7S	serial data output
10	$\overline{\text{MR}}$	master reset (active LOW)
11	SHCP	shift register clock input
12	STCP	storage register clock input
13	$\overline{\text{OE}}$	output enable input (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V <sub>CC</sub>	supply voltage

## 2.4、Function Table

Control				Input	Output		Function
SHCP	STCP	$\overline{\text{OE}}$	$\overline{\text{MR}}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{\text{MR}}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;

↑=LOW-to-HIGH transition; X=don't care; NC=no change.



## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit	
supply voltage	$V_{CC}$	-	-0.5	+7.0	V	
input clamping current	$I_{IK}$	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	$\pm 20$	mA	
output clamping current	$I_{OK}$	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	$\pm 20$	mA	
output current	$I_O$	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	pin Q7S	-	$\pm 25$	mA
			pins Qn	-	$\pm 35$	mA
supply current	$I_{CC}$	-	-	70	mA	
ground current	$I_{GND}$	-	-70	-	mA	
storage temperature	$T_{stg}$	-	-65	+150	°C	
total power dissipation	$P_{tot}$	-	-	500	mW	
soldering temperature	$T_L$	10s	DIP	245	°C	
			SOP	250	°C	

### 3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>AiP74HC595</b>						
supply voltage	$V_{CC}$	-	2.0	5.0	6.0	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
ambient temperature	$T_{amb}$	-	-40	-	+125	°C
<b>AiP74HCT595</b>						
supply voltage	$V_{CC}$	-	4.5	5.0	5.5	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
ambient temperature	$T_{amb}$	-	-40	-	+125	°C



## 3.3、Electrical Characteristics

### 3.3.1、DC Characteristics 1

( $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>AiP74HC595</b>							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0\text{V}$	1.5	1.2	-	V	
		$V_{CC}=4.5\text{V}$	3.15	2.4	-	V	
		$V_{CC}=6.0\text{V}$	4.2	3.2	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0\text{V}$	-	0.8	0.5	V	
		$V_{CC}=4.5\text{V}$	-	1.35	1.0	V	
		$V_{CC}=6.0\text{V}$	-	1.8	1.5	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	all outputs; $I_O = -20\mu\text{A}$ ; $V_{CC} = 2.0\text{V}$	1.9	2.0	-	V
			all outputs; $I_O = -20\mu\text{A}$ ; $V_{CC} = 4.5\text{V}$	4.4	4.5	-	V
			all outputs; $I_O = -20\mu\text{A}$ ; $V_{CC} = 6.0\text{V}$	5.9	6.0	-	V
			Q7S output; $I_O = -4.0\text{mA}$ ; $V_{CC} = 4.5\text{V}$	3.84	4.32	-	V
			Q7S output; $I_O = -5.2\text{mA}$ ; $V_{CC} = 6.0\text{V}$	5.34	5.81	-	V
			Qn bus driver outputs; $I_O = -6.0\text{mA}$ ; $V_{CC} = 4.5\text{V}$	3.84	4.32	-	V
			Qn bus driver outputs; $I_O = -7.8\text{mA}$ ; $V_{CC} = 6.0\text{V}$	5.34	5.81	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	all outputs; $I_O = 20\mu\text{A}$ ; $V_{CC} = 2.0\text{V}$	-	0	0.1	V
			all outputs; $I_O = 20\mu\text{A}$ ; $V_{CC} = 4.5\text{V}$	-	0	0.1	V
			all outputs; $I_O = 20\mu\text{A}$ ; $V_{CC} = 6.0\text{V}$	-	0	0.1	V
			Q7S output; $I_O = 4.0\text{mA}$ ; $V_{CC} = 4.5\text{V}$	-	0.15	0.33	V
			Q7S output; $I_O = 5.2\text{mA}$ ; $V_{CC} = 6.0\text{V}$	-	0.16	0.33	V
			Qn bus driver outputs; $I_O = 6.0\text{mA}$ ; $V_{CC} = 4.5\text{V}$	-	0.15	0.33	V
			Qn bus driver outputs; $I_O = 7.8\text{mA}$ ; $V_{CC} = 6.0\text{V}$	-	0.16	0.33	V
input leakage current	$I_I$	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{V}$	-	-	$\pm 1.0$	$\mu\text{A}$	
OFF-state output current	$I_{OZ}$	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 6.0\text{V}$ ; $V_O = V_{CC}$ or GND	-	-	$\pm 5.0$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_I = V_{CC}$ or GND; $I_O = 0\text{A}$ ; $V_{CC} = 6.0\text{V}$	-	-	80	$\mu\text{A}$	
input capacitance	$C_I$	-	-	3.5	-	pF	
<b>AiP74HCT595</b>							
HIGH-level input voltage	$V_{IH}$	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$	2.0	1.6	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$	-	1.2	0.8	V	





HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC}=4.5V$	all outputs; $I_O=-20\mu A$	4.4	4.5	-	V
			Q7S output; $I_O=-4.0mA$	3.84	4.32	-	V
			Qn bus driver outputs; $I_O=-6.0mA$	3.7	4.32	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC}=4.5V$	all outputs; $I_O=20\mu A$	-	0	0.1	V
			Q7S output; $I_O=4.0mA$	-	0.15	0.33	V
			Qn bus driver outputs; $I_O=6.0mA$	-	0.16	0.33	V
input leakage current	$I_I$	$V_I=V_{CC} \text{ or } GND; V_{CC}=5.5V$	-	-	$\pm 1.0$	$\mu A$	
OFF-state output current	$I_{OZ}$	$V_I=V_{IH} \text{ or } V_{IL}; V_{CC}=5.5V; V_O=V_{CC} \text{ or } GND$	-	-	$\pm 5.0$	$\mu A$	
supply current	$I_{CC}$	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=5.5V$	-	-	80	$\mu A$	
additional supply current	$\Delta I_{CC}$	per input pin; $V_I=V_{CC}-2.1V$ ; other inputs at $V_{CC}$ or $GND; I_O=0A; V_{CC}=4.5V \text{ to } 5.5V$	pins MR, SHCP, STCP, OE	-	150	675	$\mu A$
			pin DS	-	25	113	$\mu A$
input capacitance	$C_I$	-	-	3.5	-	pF	

### 3.3.2、DC Characteristics 2

( $T_{amb}=-40^{\circ}C$  to  $+125^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>AiP74HC595</b>							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	-	-	V	
		$V_{CC}=4.5V$	3.15	-	-	V	
		$V_{CC}=6.0V$	4.2	-	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	-	0.5	V	
		$V_{CC}=4.5V$	-	-	1.0	V	
		$V_{CC}=6.0V$	-	-	1.5	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}$	all outputs; $I_O=-20\mu A; V_{CC}=2.0V$	1.9	-	-	V
			all outputs; $I_O=-20\mu A; V_{CC}=4.5V$	4.4	-	-	V
			all outputs; $I_O=-20\mu A; V_{CC}=6.0V$	5.9	-	-	V
			Q7S output; $I_O=-4.0mA; V_{CC}=4.5V$	3.7	-	-	V
			Q7S output; $I_O=-5.2mA; V_{CC}=6.0V$	5.2	-	-	V
			Qn bus driver outputs; $I_O=-6.0mA; V_{CC}=4.5V$	3.7	-	-	V
			Qn bus driver outputs; $I_O=-7.8mA; V_{CC}=6.0V$	5.2	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	all outputs; $I_O=20\mu A; V_{CC}=2.0V$	-	-	0.1	V
			all outputs; $I_O=20\mu A; V_{CC}=4.5V$	-	-	0.1	V
			all outputs;	-	-	0.1	V



			$I_O=20\mu\text{A}; V_{CC}=6.0\text{V}$				
			Q7S output; $I_O=4.0\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.4	V
			Q7S output; $I_O=5.2\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.4	V
			Qn bus driver outputs; $I_O=6.0\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.4	V
			Qn bus driver outputs; $I_O=7.8\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.4	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=6.0\text{V}$		-	-	$\pm 1.0$	$\mu\text{A}$
OFF-state output current	$I_{OZ}$	$V_I=V_{IH}$ or $V_{IL}; V_{CC}=6.0\text{V};$ $V_O=V_{CC}$ or GND		-	-	$\pm 10$	$\mu\text{A}$
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_O=0\text{A}; V_{CC}=6.0\text{V}$		-	-	160	$\mu\text{A}$
<b>AiP74HCT595</b>							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=4.5\text{V}$ to $5.5\text{V}$		2.0	-	-	V
LOW-level input voltage	$V_{IL}$	$V_{CC}=4.5\text{V}$ to $5.5\text{V}$		-	-	0.8	V
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL};$ $V_{CC}=4.5\text{V}$	all outputs; $I_O=-20\mu\text{A}$	4.4	-	-	V
			Q7S output; $I_O=-4.0\text{mA}$	3.7	-	-	V
			Qn bus driver outputs; $I_O=-6.0\text{mA}$	3.7	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL};$ $V_{CC}=4.5\text{V}$	all outputs; $I_O=20\mu\text{A}$	-	-	0.1	V
			Q7S output; $I_O=4.0\text{mA}$	-	-	0.4	V
			Qn bus driver outputs; $I_O=6.0\text{mA}$	-	-	0.4	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=5.5\text{V}$		-	-	$\pm 1.0$	$\mu\text{A}$
OFF-state output current	$I_{OZ}$	$V_I=V_{IH}$ or $V_{IL}; V_{CC}=5.5\text{V};$ $V_O=V_{CC}$ or GND		-	-	$\pm 10$	$\mu\text{A}$
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_O=0\text{A}; V_{CC}=5.5\text{V}$		-	-	160	$\mu\text{A}$
additional supply current	$\Delta I_{CC}$	per input pin; $V_I=V_{CC}-2.1\text{V};$ other inputs at $V_{CC}$ or GND; $I_O=0\text{A};$ $V_{CC}=4.5\text{V}$ to $5.5\text{V}$	pins $\overline{\text{MR}}, \text{SHCP},$ $\text{STCP}, \overline{\text{OE}}$	-	-	735	$\mu\text{A}$
			pin DS	-	-	123	$\mu\text{A}$



### 3.3.3、AC Characteristics 1

( $T_{amb}=25^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ. <sup>[1]</sup>	Max.	Unit	
<b>AiP74HC595</b>							
propagation delay	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	$V_{CC}=2.0V$	-	75	160	ns
			$V_{CC}=4.5V$	-	19	32	ns
			$V_{CC}=6.0V$	-	15	27	ns
		STCP to Qn; see Figure 7	$V_{CC}=2.0V$	-	85	175	ns
			$V_{CC}=4.5V$	-	20	35	ns
			$V_{CC}=6.0V$	-	16	30	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Q7S; see Figure 9	$V_{CC}=2.0V$	-	47	175	ns
			$V_{CC}=4.5V$	-	17	35	ns
			$V_{CC}=6.0V$	-	14	30	ns
$\overline{OE}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	$V_{CC}=2.0V$	-	47	150	ns
			$V_{CC}=4.5V$	-	17	30	ns
			$V_{CC}=6.0V$	-	14	26	ns
$\overline{OE}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	$V_{CC}=2.0V$	-	41	150	ns
			$V_{CC}=4.5V$	-	15	30	ns
			$V_{CC}=6.0V$	-	12	27	ns
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	$V_{CC}=2.0V$	75	17	-	ns
			$V_{CC}=4.5V$	15	6	-	ns
			$V_{CC}=6.0V$	13	5	-	ns
		STCP HIGH or LOW; see Figure 7	$V_{CC}=2.0V$	75	11	-	ns
			$V_{CC}=4.5V$	15	4	-	ns
			$V_{CC}=6.0V$	13	3	-	ns
		$\overline{MR}$ LOW; see Figure 9	$V_{CC}=2.0V$	75	17	-	ns
			$V_{CC}=4.5V$	15	6	-	ns
			$V_{CC}=6.0V$	13	5	-	ns
set-up time	$t_{su}$	DS to SHCP; see Figure 8	$V_{CC}=2.0V$	50	11	-	ns
			$V_{CC}=4.5V$	10	4	-	ns
			$V_{CC}=6.0V$	9	3	-	ns
		SHCP to STCP; see Figure 7	$V_{CC}=2.0V$	75	22	-	ns
			$V_{CC}=4.5V$	15	8	-	ns
			$V_{CC}=6.0V$	13	7	-	ns
DS to SHCP hold time	$t_h$	see Figure 8	$V_{CC}=2.0V$	3	-6	-	ns
			$V_{CC}=4.5V$	3	-2	-	ns
			$V_{CC}=6.0V$	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	$t_{rec}$	see Figure 9	$V_{CC}=2.0V$	50	-19	-	ns
			$V_{CC}=4.5V$	10	-7	-	ns
			$V_{CC}=6.0V$	9	-6	-	ns
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	$V_{CC}=2.0V$	9	-	-	MHz
			$V_{CC}=4.5V$	30	-	-	MHz
			$V_{CC}=6.0V$	35	-	-	MHz
<b>AiP74HCT595; <math>V_{CC}=4.5V</math> to <math>5.5V</math></b>							
propagation	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	-	25	42	ns	



delay		STCP to Qn; see Figure 7	-	24	40	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Q7S; see Figure 9	-	23	40	ns
$\overline{OE}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	-	21	35	ns
$\overline{OE}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	-	18	30	ns
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	16	6	-	ns
		STCP HIGH or LOW; see Figure 7	16	5	-	ns
		$\overline{MR}$ LOW; see Figure 9	20	8	-	ns
set-up time	$t_{su}$	DS to SHCP; see Figure 8	16	5	-	ns
		SHCP to STCP; see Figure 7	16	8	-	ns
DS to SHCP hold time	$t_h$	see Figure 8	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	$t_{rec}$	see Figure 9	10	-7	-	ns
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	30	-	-	MHz

Note:

[1] Typical values are measured at nominal supply voltage.

### 3.3.4、AC Characteristics 2

( $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>AiP74HC595</b>							
propagation delay	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	$V_{CC}=2.0V$	-	-	200	ns
			$V_{CC}=4.5V$	-	-	40	ns
			$V_{CC}=6.0V$	-	-	34	ns
		STCP to Qn; see Figure 7	$V_{CC}=2.0V$	-	-	220	ns
			$V_{CC}=4.5V$	-	-	44	ns
			$V_{CC}=6.0V$	-	-	37	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Q7S; see Figure 9	$V_{CC}=2.0V$	-	-	220	ns
			$V_{CC}=4.5V$	-	-	44	ns
			$V_{CC}=6.0V$	-	-	37	ns
$\overline{OE}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	$V_{CC}=2.0V$	-	-	190	ns
			$V_{CC}=4.5V$	-	-	38	ns
			$V_{CC}=6.0V$	-	-	33	ns
$\overline{OE}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	$V_{CC}=2.0V$	-	-	190	ns
			$V_{CC}=4.5V$	-	-	38	ns
			$V_{CC}=6.0V$	-	-	33	ns
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns
			$V_{CC}=6.0V$	16	-	-	ns
		STCP HIGH or LOW;	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns



		see Figure 7	$V_{CC}=6.0V$	16	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns
			$V_{CC}=6.0V$	16	-	-	ns
set-up time	$t_{su}$	DS to SHCP; see Figure 8	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
		SHCP to STCP; see Figure 7	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns
			$V_{CC}=6.0V$	16	-	-	ns
DS to SHCP hold time	$t_h$	see Figure 8	$V_{CC}=2.0V$	3	-	-	ns
			$V_{CC}=4.5V$	3	-	-	ns
			$V_{CC}=6.0V$	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	$t_{rec}$	see Figure 9	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	$V_{CC}=2.0V$	4.8	-	-	MHz
			$V_{CC}=4.5V$	24	-	-	MHz
			$V_{CC}=6.0V$	28	-	-	MHz
<b>AiP74HCT595; <math>V_{CC}=4.5V</math> to <math>5.5V</math></b>							
propagation delay	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	-	-	53	ns	
		STCP to Qn; see Figure 7	-	-	50	ns	
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Q7S; see Figure 9	-	-	50	ns	
$\overline{OE}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	-	-	44	ns	
$\overline{OE}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	-	-	38	ns	
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	20	-	-	ns	
		STCP HIGH or LOW; see Figure 7	20	-	-	ns	
		$\overline{MR}$ LOW; see Figure 9	25	-	-	ns	
set-up time	$t_{su}$	DS to SHCP; see Figure 8	20	-	-	ns	
		SHCP to STCP; see Figure 7	20	-	-	ns	
DS to SHCP hold time	$t_h$	see Figure 8	3	-	-	ns	
$\overline{MR}$ to SHCP recovery time	$t_{rec}$	see Figure 9	13	-	-	ns	
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	24	-	-	MHz	



### 3.3.5、AC Characteristics 3

( $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>AiP74HC595</b>							
propagation delay	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	240	ns
			$V_{CC}=4.5\text{V}$	-	-	48	ns
			$V_{CC}=6.0\text{V}$	-	-	41	ns
		STCP to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	265	ns
			$V_{CC}=4.5\text{V}$	-	-	53	ns
			$V_{CC}=6.0\text{V}$	-	-	45	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{\text{MR}}$ to Q7S; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	265	ns
			$V_{CC}=4.5\text{V}$	-	-	53	ns
			$V_{CC}=6.0\text{V}$	-	-	45	ns
$\overline{\text{OE}}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	225	ns
			$V_{CC}=4.5\text{V}$	-	-	45	ns
			$V_{CC}=6.0\text{V}$	-	-	38	ns
$\overline{\text{OE}}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	225	ns
			$V_{CC}=4.5\text{V}$	-	-	45	ns
			$V_{CC}=6.0\text{V}$	-	-	38	ns
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	$V_{CC}=2.0\text{V}$	110	-	-	ns
			$V_{CC}=4.5\text{V}$	22	-	-	ns
			$V_{CC}=6.0\text{V}$	19	-	-	ns
		STCP HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	110	-	-	ns
			$V_{CC}=4.5\text{V}$	22	-	-	ns
			$V_{CC}=6.0\text{V}$	19	-	-	ns
		$\overline{\text{MR}}$ LOW; see Figure 9	$V_{CC}=2.0\text{V}$	110	-	-	ns
			$V_{CC}=4.5\text{V}$	22	-	-	ns
			$V_{CC}=6.0\text{V}$	19	-	-	ns
set-up time	$t_{su}$	DS to SHCP; see Figure 8	$V_{CC}=2.0\text{V}$	75	-	-	ns
			$V_{CC}=4.5\text{V}$	15	-	-	ns
			$V_{CC}=6.0\text{V}$	13	-	-	ns
		SHCP to STCP; see Figure 7	$V_{CC}=2.0\text{V}$	110	-	-	ns
			$V_{CC}=4.5\text{V}$	22	-	-	ns
			$V_{CC}=6.0\text{V}$	19	-	-	ns
DS to SHCP hold time	$t_h$	see Figure 8	$V_{CC}=2.0\text{V}$	3	-	-	ns
			$V_{CC}=4.5\text{V}$	3	-	-	ns
			$V_{CC}=6.0\text{V}$	3	-	-	ns
$\overline{\text{MR}}$ to SHCP recovery time	$t_{rec}$	see Figure 9	$V_{CC}=2.0\text{V}$	75	-	-	ns
			$V_{CC}=4.5\text{V}$	15	-	-	ns
			$V_{CC}=6.0\text{V}$	13	-	-	ns
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	$V_{CC}=2.0\text{V}$	4	-	-	MHz
			$V_{CC}=4.5\text{V}$	20	-	-	MHz
			$V_{CC}=6.0\text{V}$	24	-	-	MHz
<b>AiP74HCT595; <math>V_{CC}=4.5\text{V}</math> to <math>5.5\text{V}</math></b>							
propagation	$t_{PLH}, t_{PHL}$	SHCP to Q7S; see Figure 6	-	-	63	ns	



delay		STCP to Qn; see Figure 7	-	-	60	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Q7S; see Figure 9	-	-	60	ns
$\overline{OE}$ to Qn enable time	$t_{PZH}, t_{PZL}$	see Figure 10	-	-	53	ns
$\overline{OE}$ to Qn disable time	$t_{PLZ}, t_{PHZ}$	see Figure 10	-	-	45	ns
pulse width	$t_w$	SHCP HIGH or LOW; see Figure 6	24	-	-	ns
		STCP HIGH or LOW; see Figure 7	24	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	30	-	-	ns
set-up time	$t_{su}$	DS to SHCP; see Figure 8	24	-	-	ns
		SHCP to STCP; see Figure 7	24	-	-	ns
DS to SHCP hold time	$t_h$	see Figure 8	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	$t_{rec}$	see Figure 9	15	-	-	ns
maximum frequency	$f_{max}$	SHCP or STCP; see Figure 6 and Figure 7	20	-	-	MHz

#### 4、Testing Circuit

##### 4.1、AC Testing Circuit

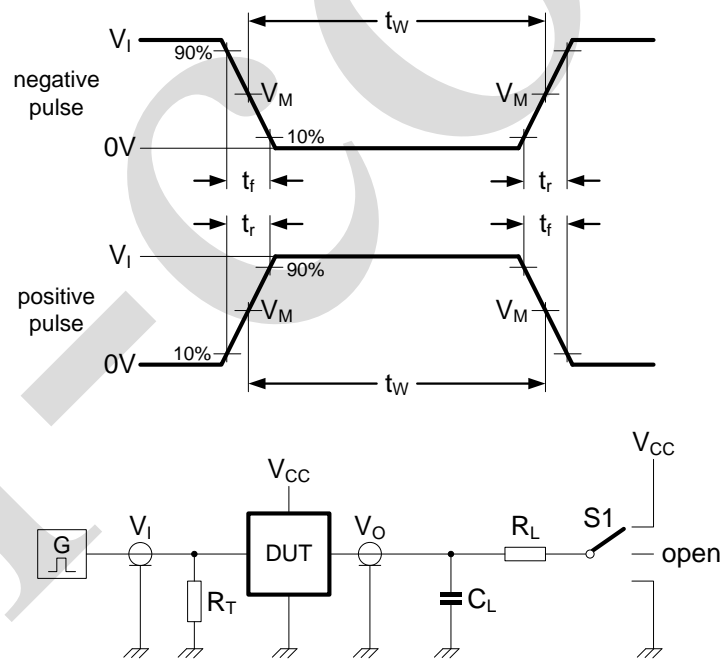


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

$R_L$ =Load resistance.

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

S1=Test selection switch.



4.2、AC Testing Waveforms

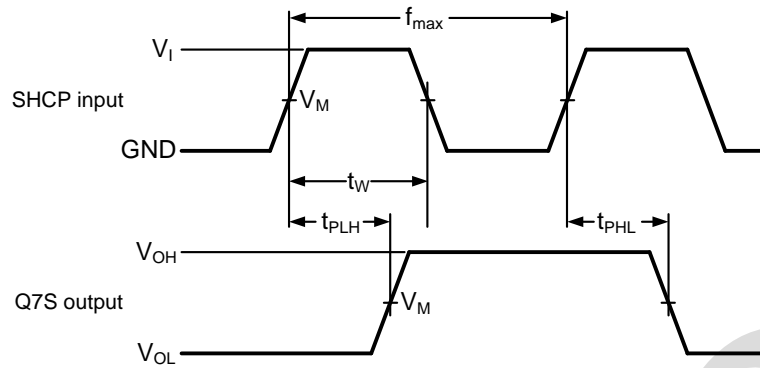


Figure 6. Shift clock pulse, maximum frequency and input to output propagation delays

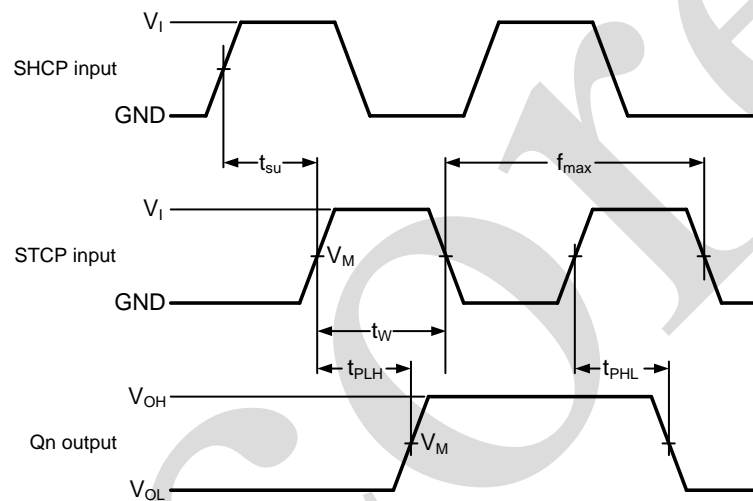


Figure 7. Storage clock to output propagation delays

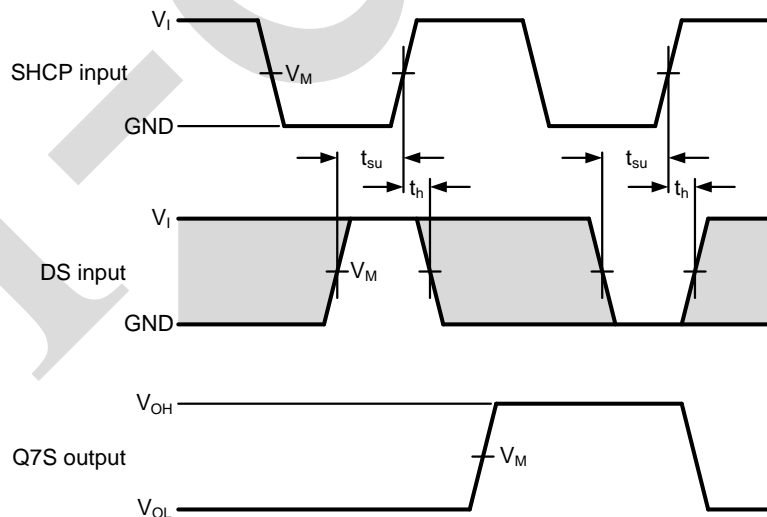


Figure 8. Data set-up and hold times



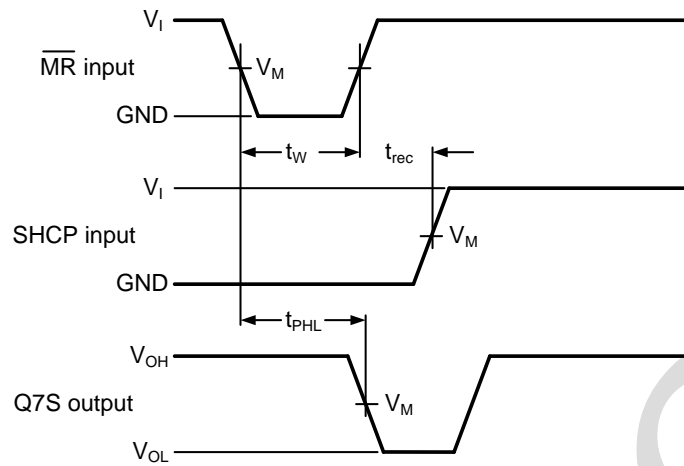


Figure 9. Master reset to output propagation delays

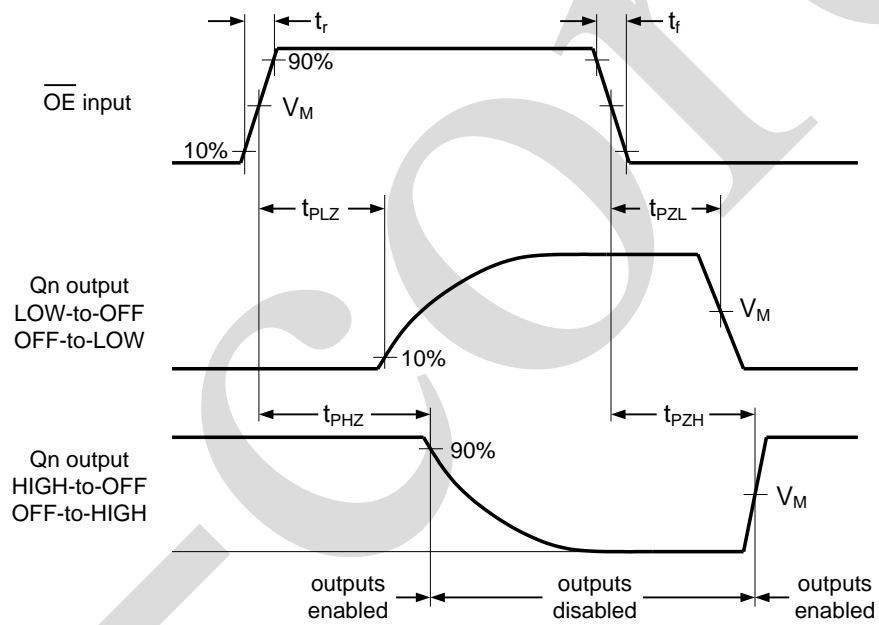


Figure 10. Enable and disable times



### 4.3、Measurement Points

Type	Input	Output
	$V_M$	$V_M$
AiP74HC595	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
AiP74HCT595	1.3V	1.3V

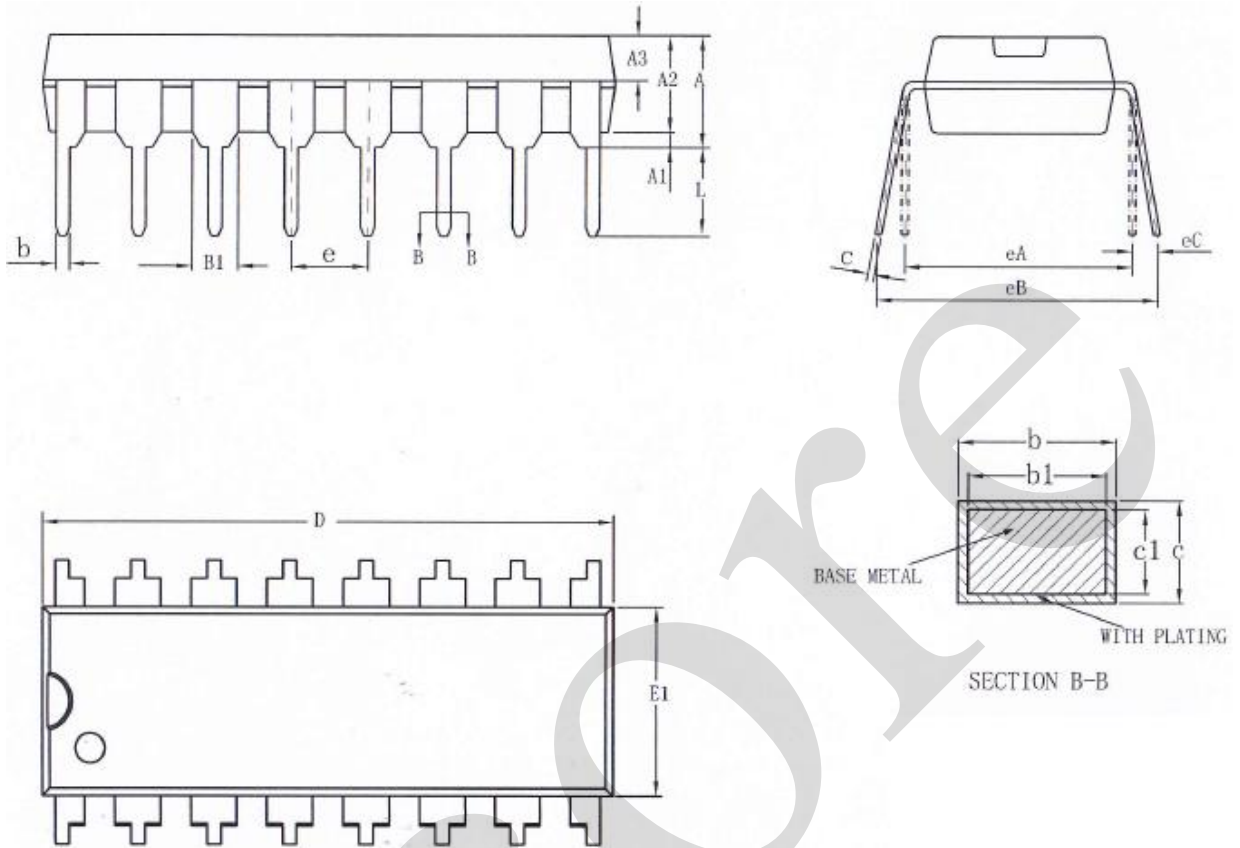
### 4.4、Test Data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL},$ $t_{PLH}$	$t_{PZH},$ $t_{PHZ}$	$t_{PZL},$ $t_{PLZ}$
AiP74HC595	$V_{CC}$	6ns	50pF	1k $\Omega$	open	GND	$V_{CC}$
AiP74HCT595	3V	6ns	50pF	1k $\Omega$	open	GND	$V_{CC}$



5、Package Information

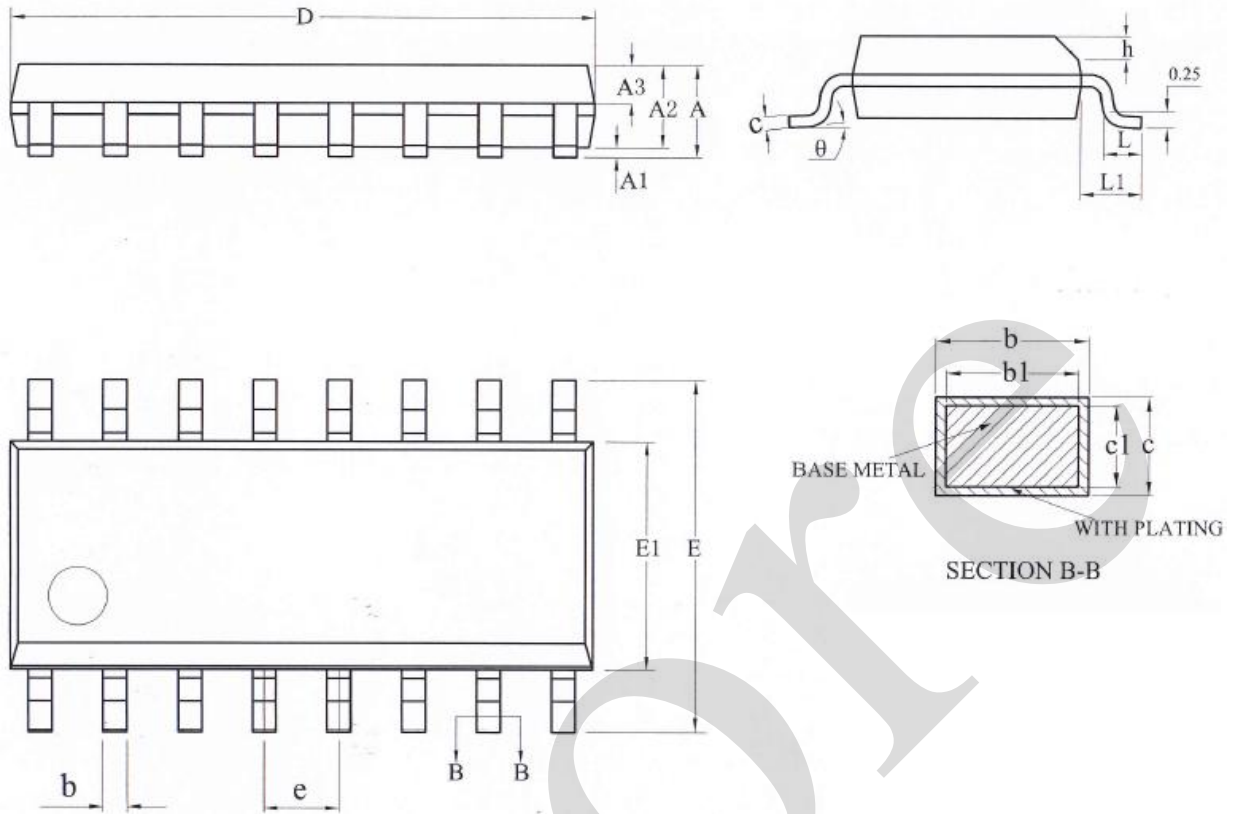
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	3.6	4.0
A1	0.51	-
A2	3.2	3.4
A3	1.47	1.57
b	0.44	0.52
b1	0.43	0.49
B1	1.52 (REF)	
c	0.25	0.29
c1	0.24	0.26
D	19.00	19.20
E1	6.25	6.45
e	2.54 (BSC)	
eA	7.62 (REF)	
eB	7.62	9.30
eC	0	0.84
L	3.00	-



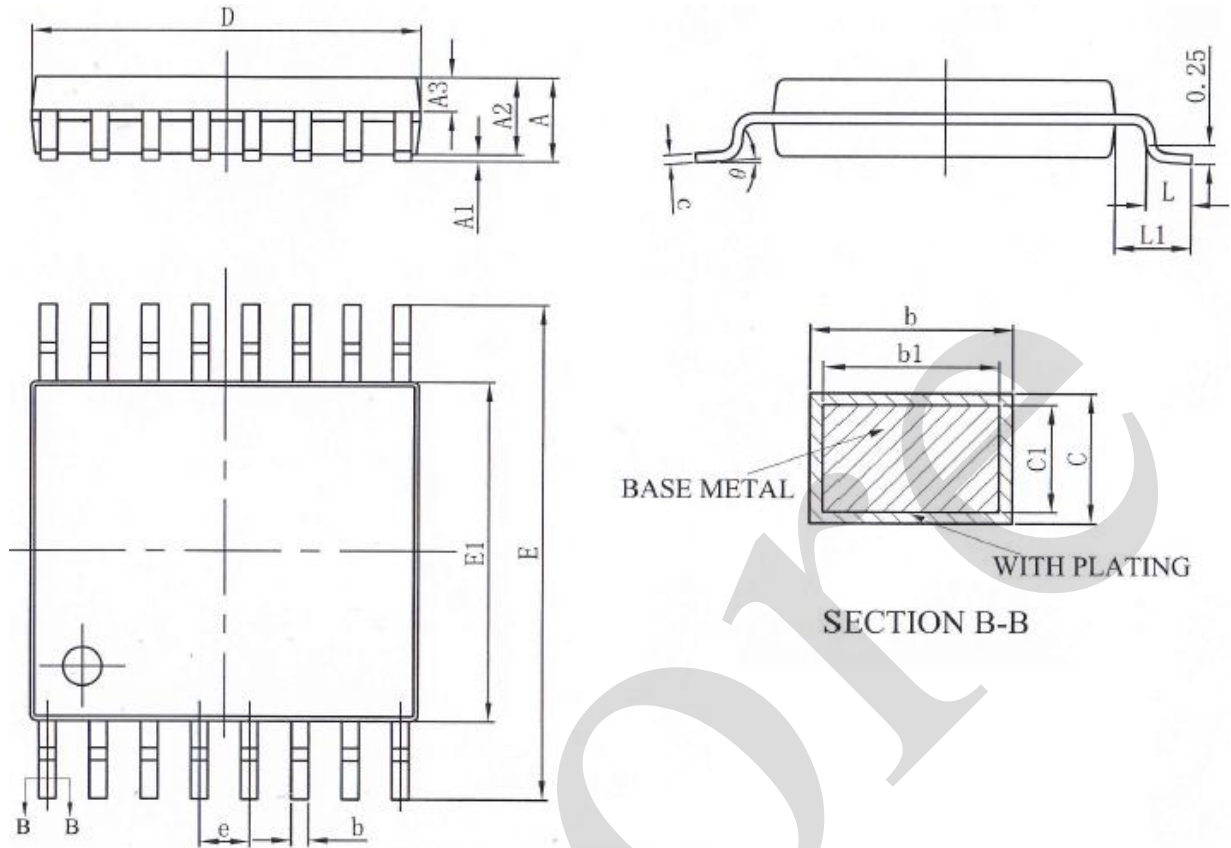
## 5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.75
A1	0.10	0.225
A2	1.30	1.50
A3	0.60	0.70
b	0.39	0.47
b1	0.38	0.44
c	0.20	0.24
c1	0.19	0.21
D	9.80	10.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 (BSC)	
h	0.25	0.50
L	0.50	0.80
L1	1.05 (REF)	
$\theta$	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.28
b1	0.19	0.25
c	0.13	0.17
c1	0.12	0.14
D	4.90	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65 (BSC)	
L	0.45	0.75
L1	1.00 (REF)	
θ	0°	8°



## 6、 Statements And Notes

### 6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

### 6.2、 Notes

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.