AiP74LVC/LVCH16T245
16-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2019-12-A1	2019-12	New
2021-12-A2	2021-12	Modify Ordering Information
2022-02-A3	2022-02	Modify ambient temperature to -40℃~+105℃ and add electrical characteristics of -40℃~+105℃

1、General Description

The AiP74LVC/LVCH16T245 are 16-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation.The device can be used as two 8-bit transceivers or as a 16-bit transceiver.It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation and four 8-bit input-output ports (nAn and nBn) each with its own output enable ($n\overline{OE}$) and send/receive (nDIR) input for direction control.Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input ($n\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn port and nBn port are in the high-impedance OFF-state.

Active bus hold circuitry in the AiP74LVCH16T245 holds unused or floating data inputs at a valid logic level.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 1.2V to 5.5V
  $V_{CC(B)}$: 1.2V to 5.5V
- Suspend mode
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption: 30uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40℃ to +105℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC16T245 TA48.TB	TSSOP48(1)	74LVC16T245	38 PCS/tube	200 tube/box	7600 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH16T245 TA48.TB	TSSOP48(1)	74LVCH16T245	38 PCS/tube	200 tube/box	7600 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVC16T245 TA48.TB	TSSOP48(2)	74LVC16T245	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH16T245 TA48.TB	TSSOP48(2)	74LVCH16T245	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

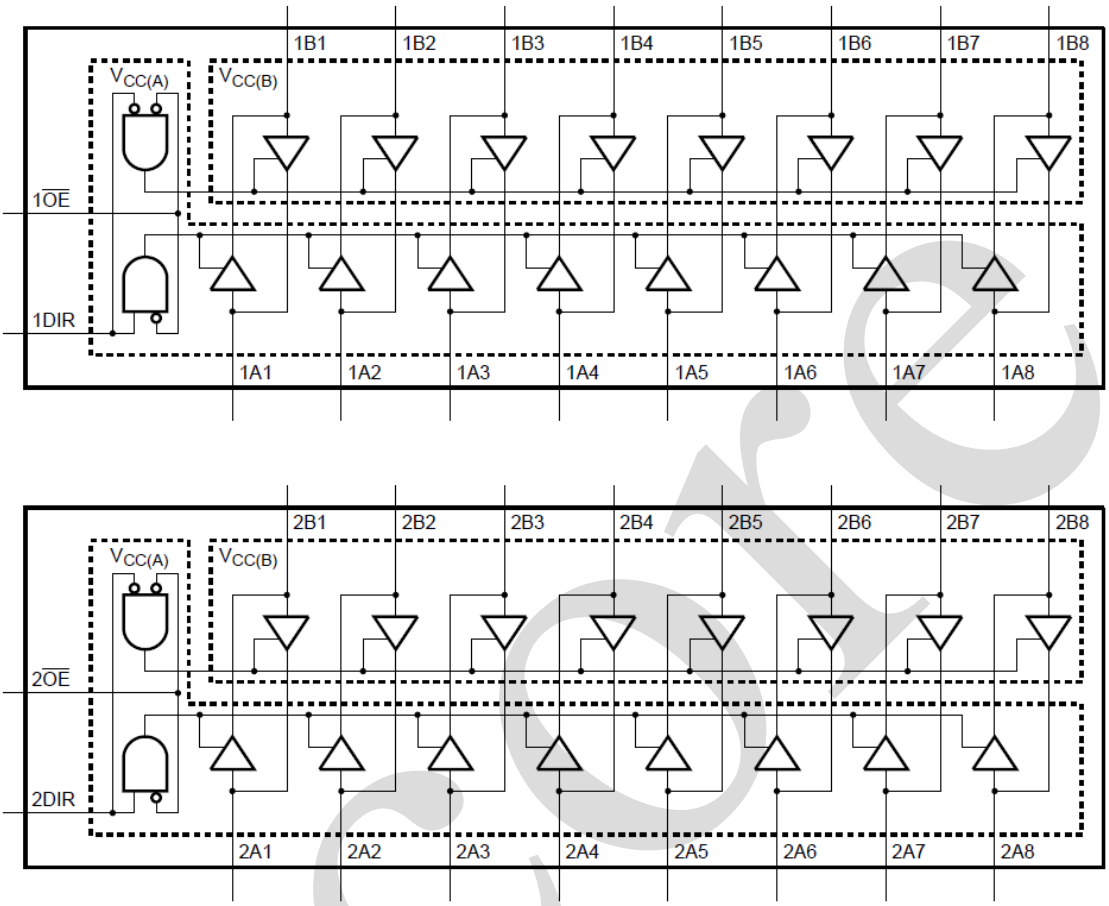


Figure 1. Logic symbol

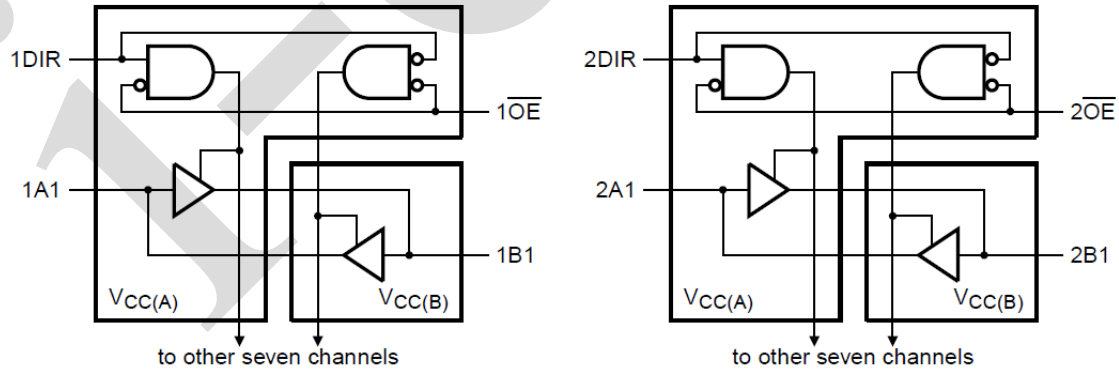
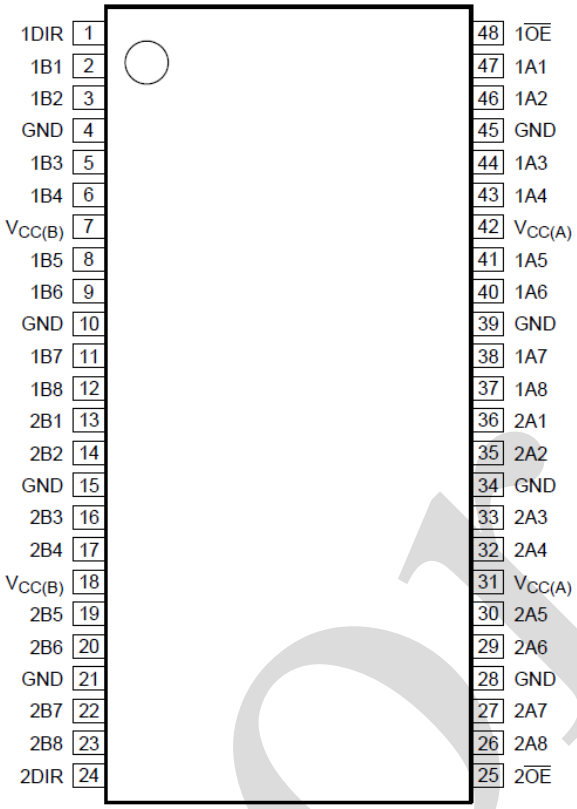


Figure 2. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1,24	1DIR,2 DIR	direction control
2,3,5,6,8,9,11,12	1B1,1B2,1B3,1B4,1B5,1B6,1B7,1B8	data input or output
13,14,16,17,19,20,22, 23	2B1,2B2,2B3,2B4,2B5,2B6,2B7,2B8	data input or output
4,10,15,21,28,34,39,45	GND[1]	ground (0V)
7,18	$V_{CC(B)}$	supply voltage B (nBn inputs/outputs are referenced to $V_{CC(B)}$)
48,25	$1\overline{OE}$,$2\overline{OE}$	output enable input (active LOW)
47,46,44,43,41,40,38,37	1A1,1A2,1A3,1A4,1A5,1A6,1A7,1A8	data input or output
36,35,33,32,30,29,27,26	2A1,2A2,2A3,2A4,2A5,2A6,2A7,2A8	data input or output
31,42	$V_{CC(A)}$	supply voltage A (nAn inputs/outputs,n$\overline{OE}$ and nDIR inputs are referenced to $V_{CC(A)}$)

Note:[1] All GND pins must be connected to ground (0V).

2.4、Function Table

Supply voltage	Input		Input/output[2]	
$V_{CC(A)}$, $V_{CC(B)}$	$n\overline{OE}$[1]	nDIR[1]	nAn[1]	nBn[1]
1.2V to 5.5V	L	L	nAn=nBn	input
1.2V to 5.5V	L	H	input	nBn=nAn
1.2V to 5.5V	H	X	Z	Z
GND[2]	X	X	Z	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[1] The nAn inputs/outputs, nDIR and $n\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The nBn inputs/outputs circuit is referenced to $V_{CC(B)}$.

[2] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output voltage	V_O	Active mode[1][2][3]	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode[1]	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CCO}[2]	-	±50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA
ground current	I_{GND}	per GND pin	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-[4]	-	500	mW
Soldering temperature	T_L	10s	250		℃

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO}+0.5V should not exceed 6.5V.

[4] For TSSOP48 package: P_{tot} derates linearly at 5.5mW/K above 60℃.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	1.2	-	5.5	V
supply voltage B	$V_{CC(B)}$	-	1.2	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+105	℃
input transition rise and fall rate	Δt/ΔV	V_{CCI}=1.2V[2]	-	-	20	ns/V
		V_{CCI}=1.4V to 1.95V	-	-	20	ns/V
		V_{CCI}=2.3V to 2.7V	-	-	20	ns/V
		V_{CCI}=3.0V to 3.6V	-	-	10	ns/V
		V_{CCI}=4.5V to 5.5V	-	-	5	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL} [1]	I_O=-3mA; V_{CCO}=1.2V	-	1.09	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=3mA; V_{CCO}=1.2V[1]	-	0.07	-	V
input leakage current	I_I	nDIR,n$\overline{OE}$ input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V[2]		-	-	±1	uA
bus hold LOW current	I_{BHL}	A or B port; V_I=0.42V; V_{CCI}=1.2V[2]		-	19	-	uA
bus hold HIGH current	I_{BHH}	A or B port; V_I=0.78V; V_{CCI}=1.2V[2]		-	-19	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port; V_{CCI}=1.2V[2][3]		-	19	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port; V_{CCI}=1.2V[2][3]		-	-19	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[1]		-	-	±1	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[1]		-	-	±1	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[1]		-	-	±1	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±1	uA

input capacitance	C_I	nDIR,n$\overline{OE}$ input; V_I=0V or 3.3V; $V_{CC(A)}$=3.3V	-	3	-	pF
input/output capacitance	$C_{I/O}$	A and B port; V_O=3.3V or 0V; $V_{CC(A)}$ =$V_{CC(B)}$=3.3V	-	6.5	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		nDIR,n$\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		nDIR,n$\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IL}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V

			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	nDIR,n$\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	15	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	25	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	100	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-15	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-25	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-100	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±2	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±2	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±2	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±2	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	15	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-2	-	-	uA

			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	15	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	25	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$= 3.0V to 5.5V	nDIR and n$\overline{OE}$ input; nDIR or n$\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	50	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open[4]	-	-	50	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC16T245).

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		nDIR,n$\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		nDIR,n$\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V

			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	$0.3V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IL}$[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	nDIR,n$\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±10	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	10	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	20	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	80	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-10	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-20	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-80	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±10	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±10	uA

		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±10	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±10	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	20	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-4	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-4	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	20	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	30	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$= 3.0V to 5.5V	nDIR and n$\overline{OE}$ input; nDIR or n$\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open[4]	-	-	75	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC16T245).

3.3.4、AC Characteristics 1

($V_{CC(A)}$=1.2V and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$						Unit
			1.2V	1.5V	1.8V	2.5V	3.3V	5.0V	
propagation delay	t_{pd}	nAn to nBn	11.0	8.5	7.4	6.2	5.7	5.4	ns
		nBn to nAn	11.0	10.0	9.5	9.1	8.9	8.9	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	9.5	9.5	9.5	9.5	9.5	9.5	ns
		n$\overline{OE}$ to nBn	10.2	8.2	7.8	6.7	7.3	6.4	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	13.5	13.5	13.5	13.5	13.5	13.5	ns
		n$\overline{OE}$ to nBn	13.6	10.3	8.9	7.5	7.1	7.0	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.5、AC Characteristics 2

($V_{CC(B)}$=1.2V and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}$						Unit
			1.2V	1.5V	1.8V	2.5V	3.3V	5.0V	
propagation delay	t_{pd}	nAn to nBn	11.0	10.0	9.5	9.1	8.9	8.8	ns
		nBn to nAn	11.0	8.5	7.3	6.2	5.7	5.4	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	9.5	6.8	5.4	3.8	4.1	3.1	ns
		n$\overline{OE}$ to nBn	10.2	9.1	8.6	8.1	7.8	7.8	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	13.5	9.0	6.9	4.8	3.8	3.2	ns
		n$\overline{OE}$ to nBn	13.6	12.5	12.0	11.5	11.4	11.4	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.6、AC Characteristics 3

($V_{CC(A)}$=$V_{CC(B)}$ and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$				Unit
			1.8V	2.5V	3.3V	5.0V	
power dissipation capacitance	C_{PD}	A port: (direction A to B); B port: (direction B to A)	1	1	1	2	pF
		A port: (direction B to A); B port: (direction A to B)	13	13	13	13	pF

Note:

C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs.

f_i=10MHz; V_I=GND to V_{CC}; $t_r=t_f$=1ns; C_L=0pF; $R_L=\infty\Omega$.

3.3.7、DC Characteristics 4

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{pd}	nAn to nBn	1.7	27	1.7	23	1.3	18	1.0	15	0.8	13	ns
		nBn to nAn	0.9	27	0.9	25	0.8	23	0.7	23	0.7	22	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.5	30	1.5	30	1.5	30	1.5	30	1.4	30	ns
		n$\overline{OE}$ to nBn	2.4	34	2.4	33	1.9	15	1.7	14	1.3	12	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.4	34	0.4	34	0.4	34	0.4	34	0.4	34	ns
		n$\overline{OE}$ to nBn	1.8	36	1.8	34	1.5	18	1.2	15	0.9	13	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{pd}	nAn to nBn	1.7	25	1.7	21.9	1.3	9.2	1.0	7.4	0.8	7.1	ns
		nBn to nAn	0.9	23	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.5	30	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
		n$\overline{OE}$ to nBn	2.4	33	2.4	32.2	1.9	13.1	1.7	12.0	1.3	10.3	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.4	24	0.4	24.0	0.4	23.8	0.4	23.7	0.4	23.7	ns
		n$\overline{OE}$ to nBn	1.8	34	1.8	32.0	1.5	16.0	1.2	12.6	0.9	10.8	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{pd}	nAn to nBn	1.5	23	1.5	21.4	1.2	9.0	0.8	6.2	0.6	4.8	ns
		nBn to nAn	1.2	18	1.2	9.3	1.0	9.1	1.0	8.9	0.9	8.8	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.4	9.0	1.4	9.0	1.4	9.0	1.4	9.0	1.4	9.0	ns
		n$\overline{OE}$ to nBn	2.3	31	2.3	29.6	1.8	11.0	1.7	9.3	0.9	6.9	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	1.0	10.9	1.0	10.9	1.0	10.9	1.0	10.9	1.0	10.9	ns
		n$\overline{OE}$ to nBn	1.7	32	1.7	28.2	1.5	12.9	1.2	9.4	1.0	6.9	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{pd}	nAn to nBn	1.5	23	1.5	21.2	1.1	8.8	0.8	6.3	0.5	4.4	ns
		nBn to nAn	0.8	15	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6.0	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
		n$\overline{OE}$ to nBn	2.1	30	2.1	29.0	1.7	10.3	1.5	8.6	0.8	6.3	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	ns
		n$\overline{OE}$ to nBn	1.8	31	1.8	27.7	1.4	12.4	1.1	8.5	0.9	6.4	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{pd}	nAn to nBn	1.5	22	1.5	21.4	1.0	8.8	0.7	6.0	0.4	4.2	ns
		nBn to nAn	0.7	13	0.7	7.0	0.4	4.8	0.3	4.5	0.3	4.3	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
		n$\overline{OE}$ to nBn	2.0	30	2.0	28.7	1.6	9.7	1.4	8.0	0.7	5.7	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
		n$\overline{OE}$ to nBn	1.5	31	1.5	27.6	1.3	11.4	1.0	8.1	0.9	6.0	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.8、DC Characteristics 5

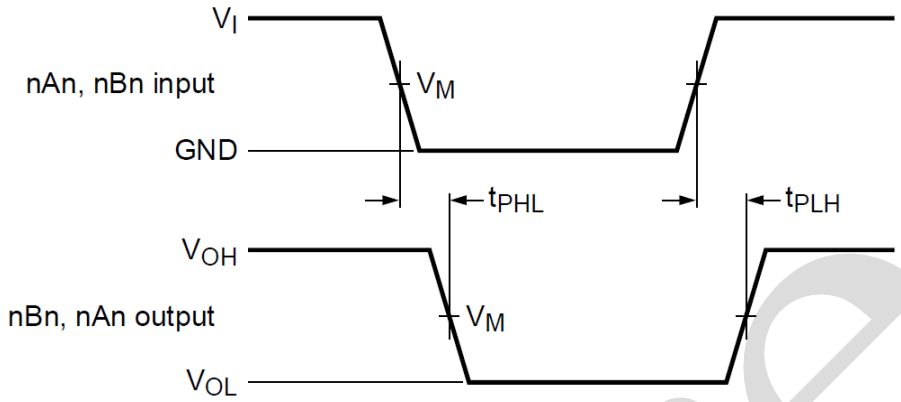
(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{pd}	nAn to nBn	1.7	32	1.7	27	1.3	21	1.0	18	0.8	16	ns
		nBn to nAn	0.9	32	0.9	30	0.8	28	0.7	28	0.7	26	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.5	34	1.5	34	1.5	34	1.5	34	1.4	34	ns
		n$\overline{OE}$ to nBn	2.4	41	2.4	40	1.9	18	1.7	17	1.3	15	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.4	40	0.4	40	0.4	40	0.4	40	0.4	40	ns
		n$\overline{OE}$ to nBn	1.8	43	1.8	41	1.5	22	1.2	18	0.9	16	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{pd}	nAn to nBn	1.7	30	1.7	25.9	1.3	13.2	1.0	11.4	0.8	11.1	ns
		nBn to nAn	0.9	27	0.9	28.8	0.8	27.6	0.7	27.4	0.7	27.4	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.5	34	1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2	ns
		n$\overline{OE}$ to nBn	2.4	40	2.4	36.2	1.9	17.1	1.7	16.0	1.3	14.3	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.4	28	0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	ns
		n$\overline{OE}$ to nBn	1.8	41	1.8	40	1.5	20	1.2	16.6	0.9	14.8	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{pd}	nAn to nBn	1.5	28	1.5	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
		nBn to nAn	1.2	23	1.2	13.3	1.0	13.1	1.0	12.9	0.9	12.8	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.4	13	1.4	13	1.4	13	1.4	13	1.4	13	ns
		n$\overline{OE}$ to nBn	2.3	37	2.3	33.6	1.8	15	1.7	14.3	0.9	10.9	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	1.0	17.2	1.0	17.2	1.0	17.3	1.0	17.2	1.0	17.3	ns
		n$\overline{OE}$ to nBn	1.7	38	1.7	32.2	1.5	18.1	1.2	14.1	1.0	11.2	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{pd}	nAn to nBn	1.5	28	1.5	25.2	1.1	12.8	0.8	10.3	0.5	10.4	ns
		nBn to nAn	0.8	18	0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	ns
		n$\overline{OE}$ to nBn	2.1	36	2.1	33	1.7	14.3	1.5	12.6	0.8	10.3	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.8	14.1	0.8	14.1	0.8	13.6	0.8	13.2	0.8	13.6	ns
		n$\overline{OE}$ to nBn	1.8	37	1.8	31.7	1.4	18.4	1.1	12.9	0.9	10.9	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{pd}	nAn to nBn	1.5	26	1.5	25.4	1.0	12.8	0.7	10	0.4	8.2	ns
		nBn to nAn	0.7	16	0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	ns
disable time	t_{dis}	n$\overline{OE}$ to nAn	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	ns
		n$\overline{OE}$ to nBn	2.0	36	2.0	32.7	1.6	13.7	1.4	12	0.7	9.7	ns
enable time	t_{en}	n$\overline{OE}$ to nAn	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	ns
		n$\overline{OE}$ to nBn	1.5	37	1.5	31.6	1.3	18.4	1.0	13.7	0.9	10.7	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

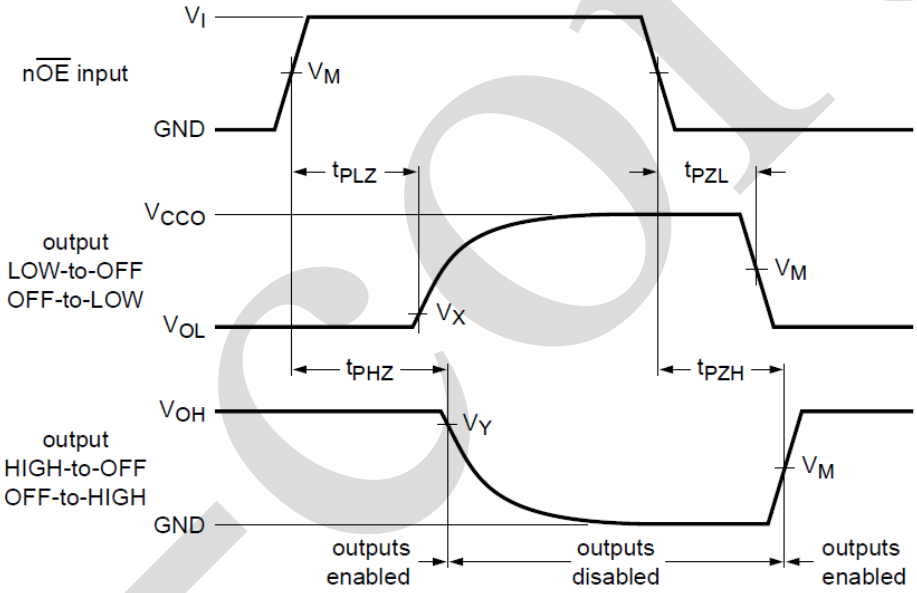
4、Testing Circuit

4.1、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times

4.2、Measurement Points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$,$V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

4.3、AC Testing Circuit

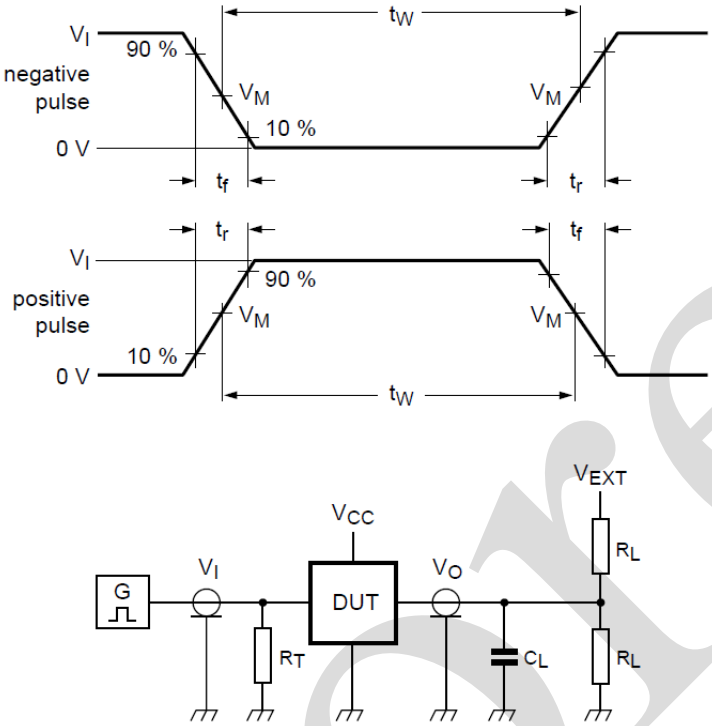


Figure 5. Load circuitry for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$,$V_{CC(B)}$	V_I[1]	$\Delta t/\Delta V$[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
1.2V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$

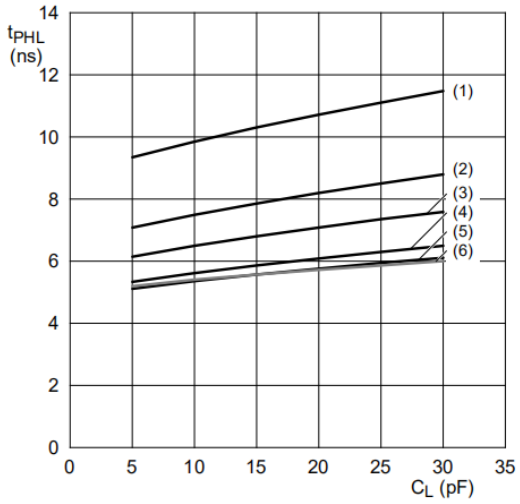
Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

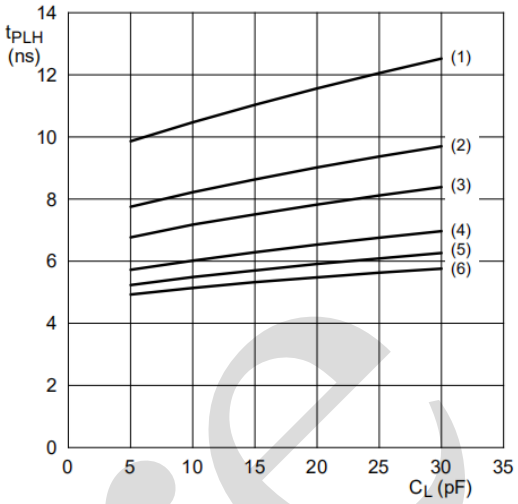
[2] dV/dt≥1.0V/ns.

[3] V_{CCO} is the supply voltage associated with the output port.

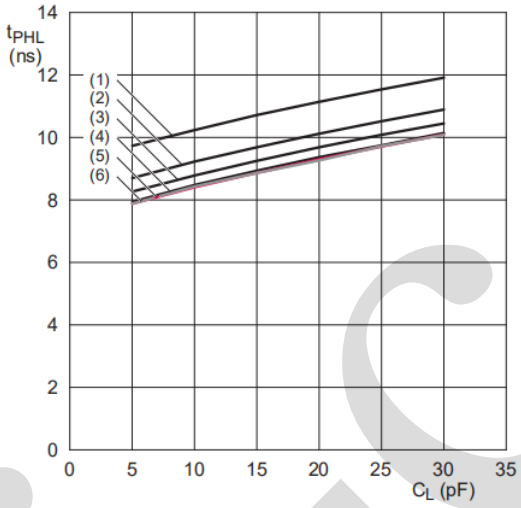
5、Characteristic Curve



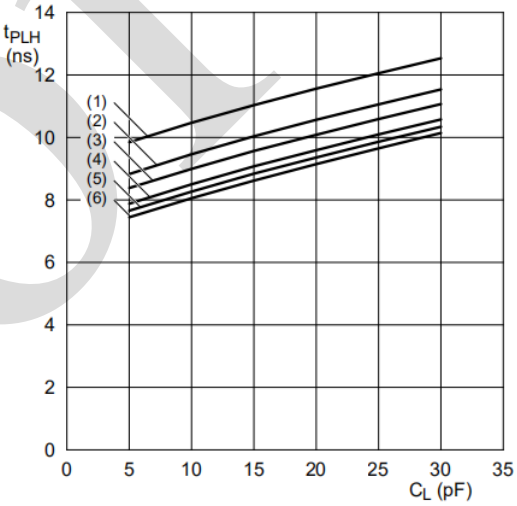
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



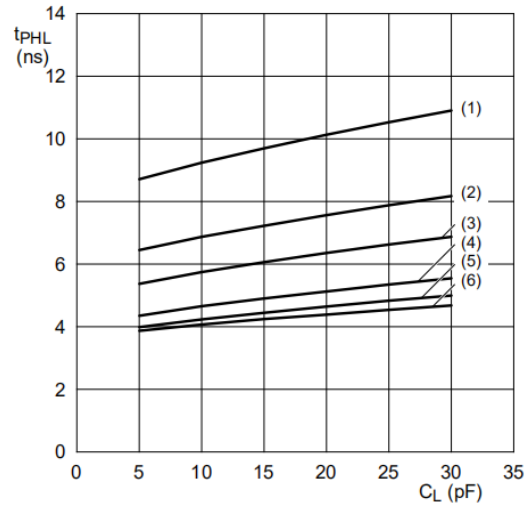
c. HIGH to LOW propagation delay (nBn to nAn)



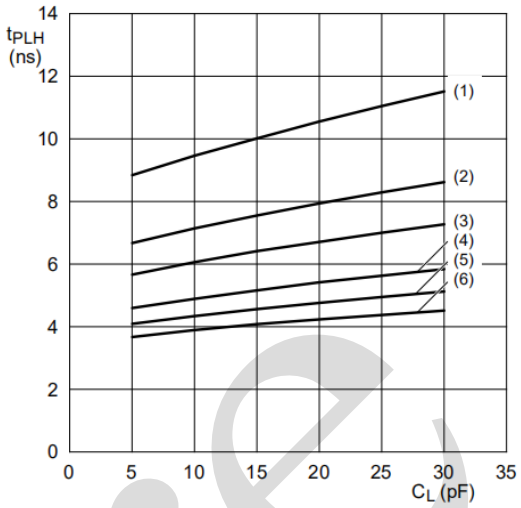
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

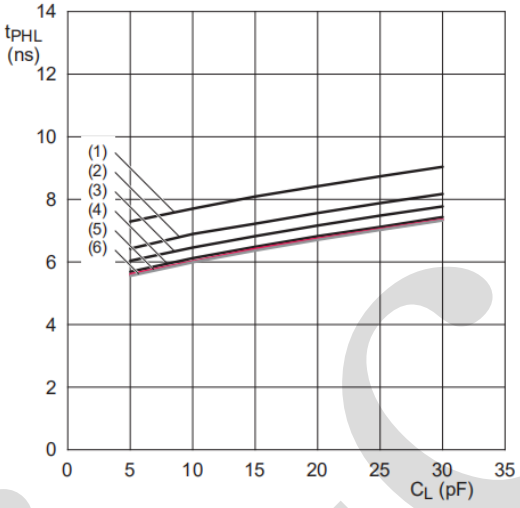
Figure 6. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.2V



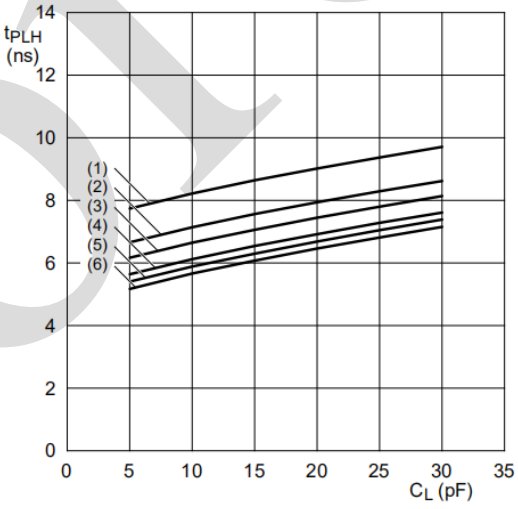
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



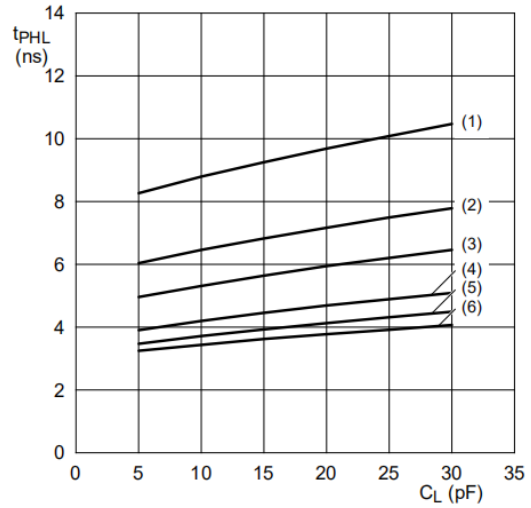
c. HIGH to LOW propagation delay (nBn to nAn)



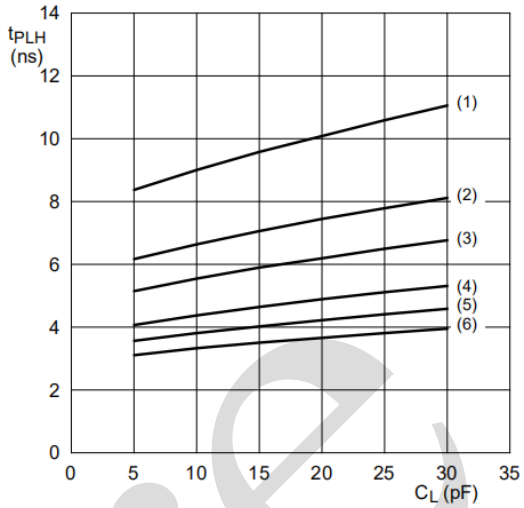
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

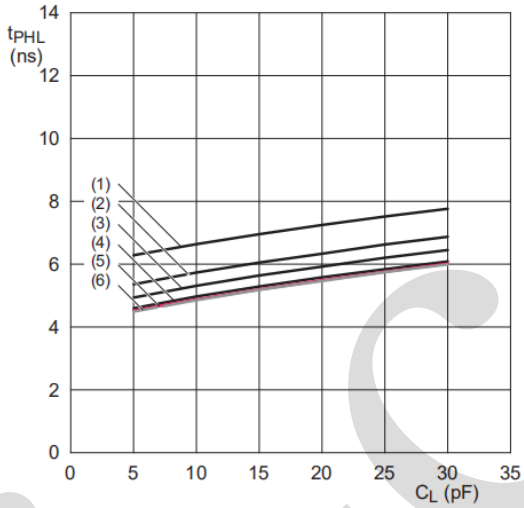
Figure 7. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.5V



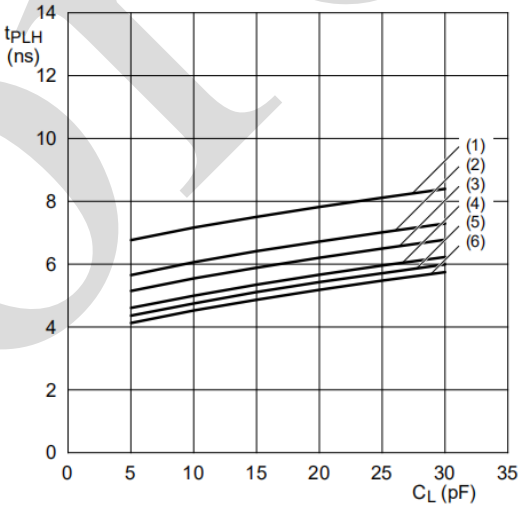
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



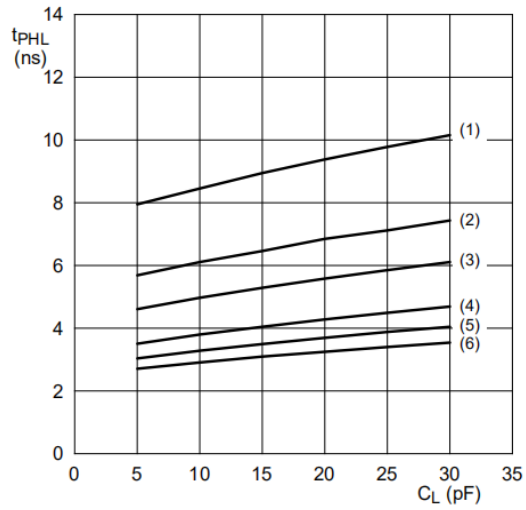
c. HIGH to LOW propagation delay (nBn to nAn)



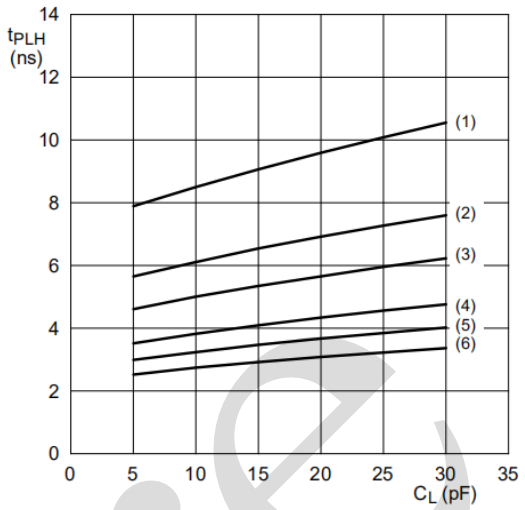
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

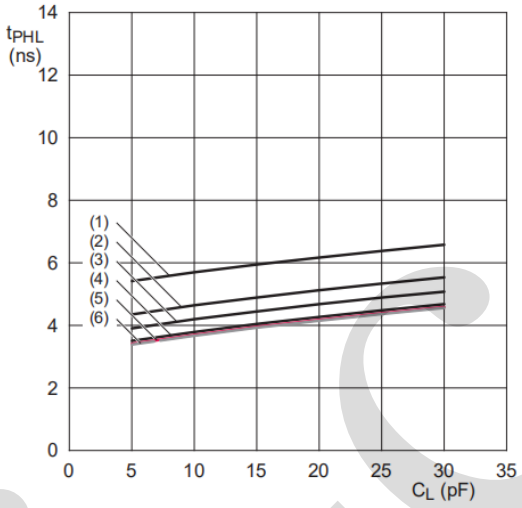
Figure 8. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.8V



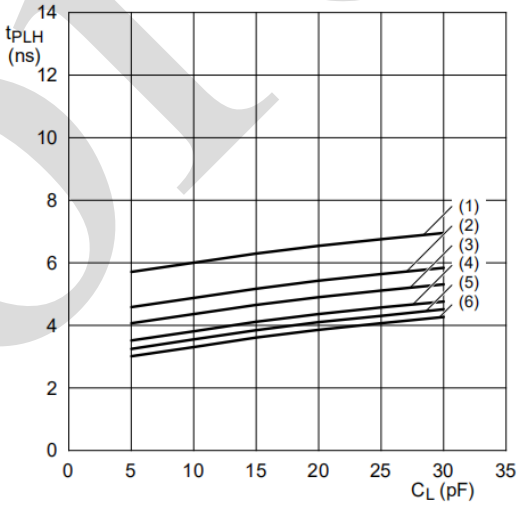
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



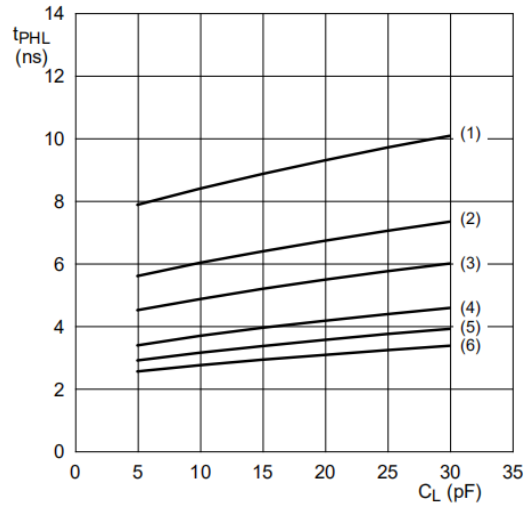
c. HIGH to LOW propagation delay (nBn to nAn)



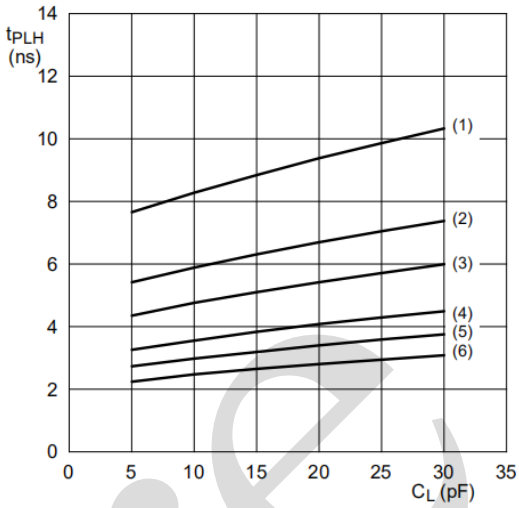
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

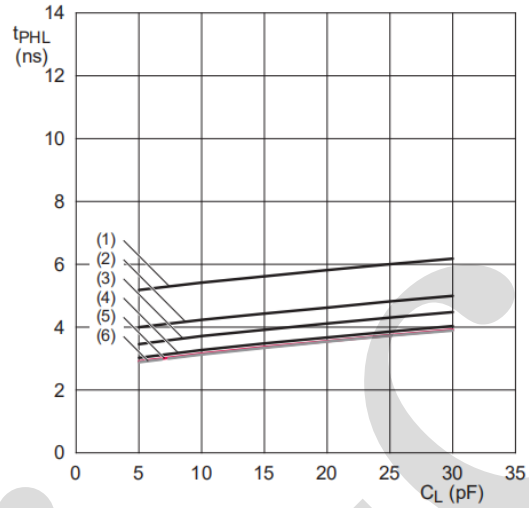
Figure 9. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=2.5V



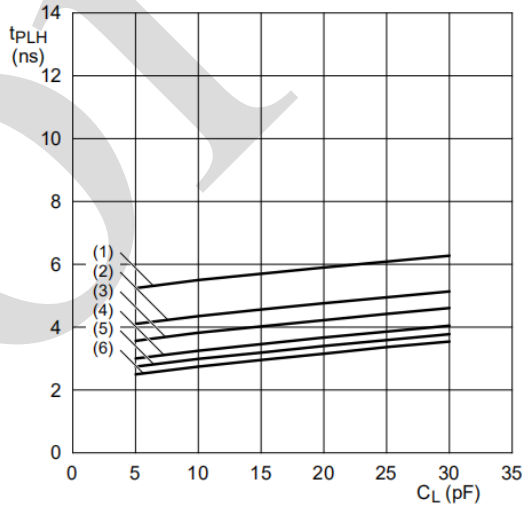
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



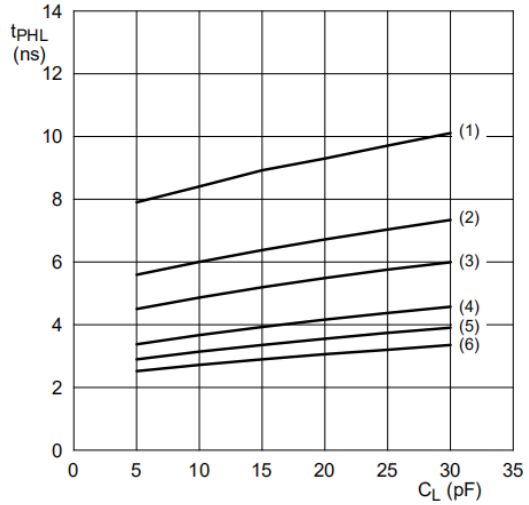
c. HIGH to LOW propagation delay (nBn to nAn)



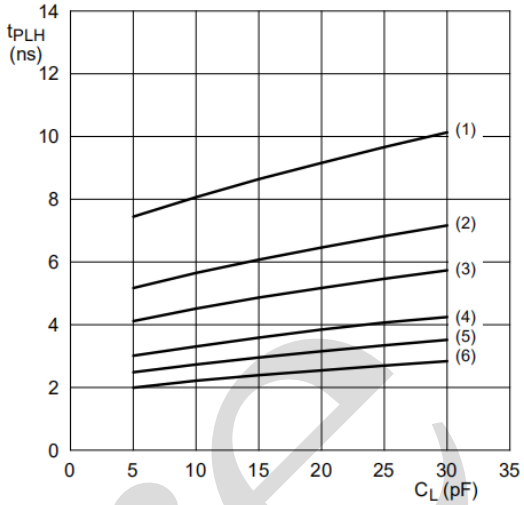
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

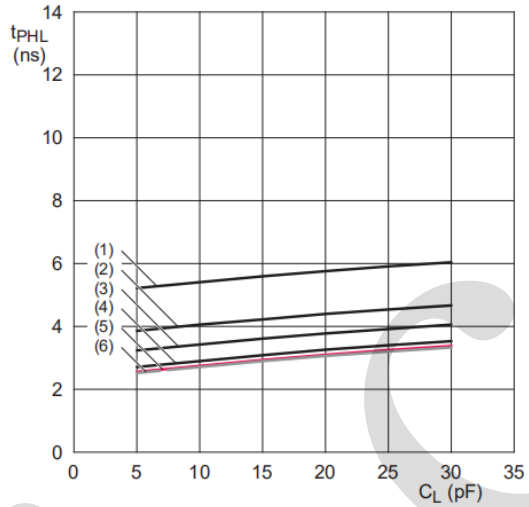
Figure 10. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=3.3V



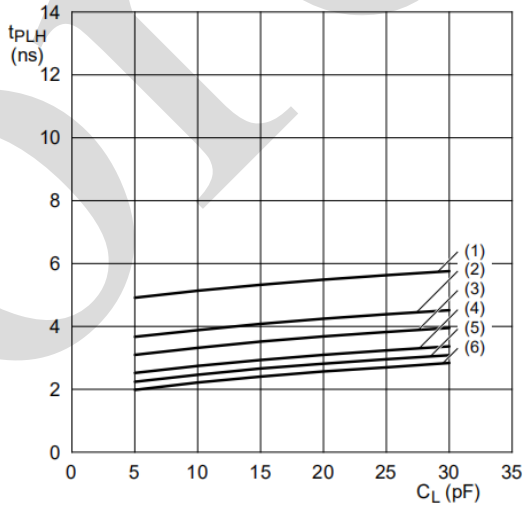
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



c. HIGH to LOW propagation delay (nBn to nAn)



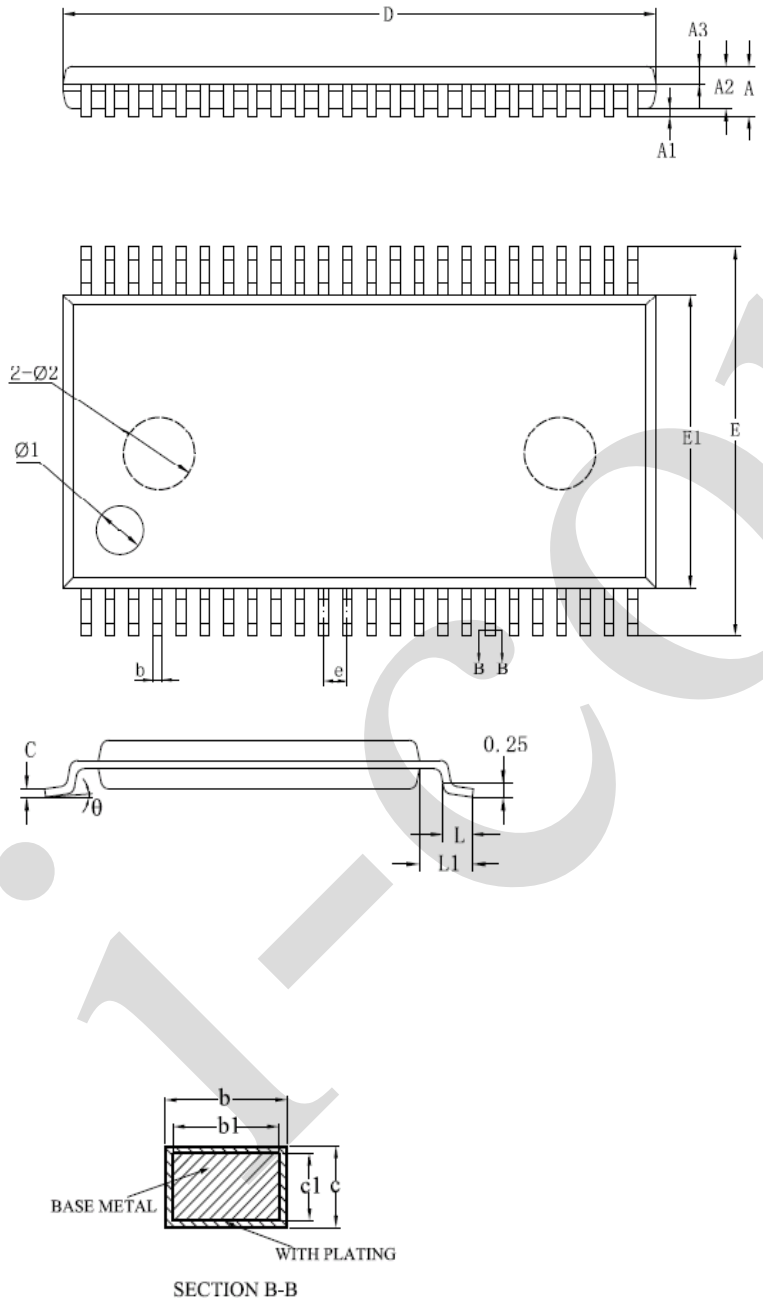
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

Figure 11. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=5.0V

6、Package Information

6.1、TSSOP48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
A3	0.35	0.40	0.45
b	0.19	—	0.28
b1	0.18	0.20	0.23
c	0.15	—	0.21
c1	0.14	0.15	0.16
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°
Ø1	Ø1.00×0.10±0.05DP		
Ø2	Ø1.50×0.075±0.025DP		

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.