Am14/1506 • Am14/1507

Dual 100-Bit Dynamic Shift Registers

Distinctive Characteristics

- Dual 100-bit silicon gate MOS shift registers
- DTL and TTL compatible
- Low-power dissipation of 0.4 mW/bit at 1 MHz
- 2 MHz frequency operation guaranteed
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

The Advanced Micro Devices dual 100-bit dynamic MOS shift registers are built using enhancement mode P-channel silicon gate MOS devices. The circuits use low-voltage circuitry for low-power dissipation and ease of interfacing into bipolar DTL and TTL circuits.

The shift registers can be driven by either DTL or TTL circuits or by MOS circuits and provide driving capability to MOS or bipolar circuits.

Silicon gate technology gives high-speed operation, low-power dissipation and low clock input capacitance.

The shift registers are ideal for low-cost buffer memories, long serial digital delay lines, etc. The devices are available in the commercial (0°C to +70°C) temperature range and the military (−55°C to +125°C) temperature range and are available with open drain output (Am14/1506), or with a 20kΩ pull-down resistor (Am14/1507) for easier interface to other circuitry.

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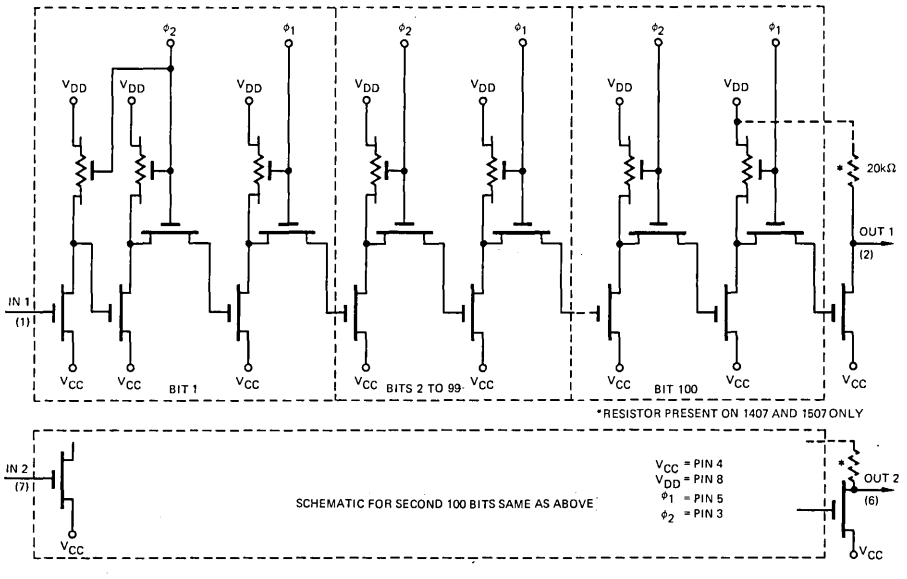
CIRCUIT DIAGRAM



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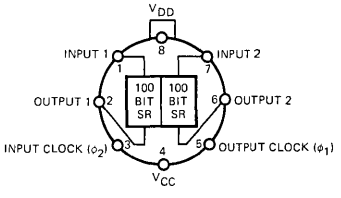
ORDERING INFORMATION

Package Type	Ambient Temperature	Output Resistor	Part Number
TO-99	$0°C \leq T_A \leq +70°C$	No	AM1506
		Yes	AM1507
	$-55°C \leq T_A \leq +125°C$	No	AM1406
		Yes	AM1407

CONNECTION DIAGRAM
Top View



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Power Dissipation	500 mW
Data and Clock Input Voltages with respect to most Positive Supply Voltage, V_{CC}	+0.5 V to −25 V
Power Supply Voltage, V_{DD} with respect to V_{CC}	+0.5 V to −25 V

ELECTRICAL CHARACTERISTICS

Am1506/1507 $T_A = 0°C$ to $+70°C$
Am1406/1407 $T_A = -55°C$ to $+125°C$
} unless otherwise specified

DC Characteristics Over Operating Temperature Range ($V_{DD} = -5.0$ V ±5%, $V_{CC} = +5.0$ V ±5% unless otherwise specified)

Parameters	Test Conditions	Limits Over Specified Temperature Range Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2) Output HIGH Voltage	$I_{OH} = -2.5$ mA, Load = 20 kΩ	2.5	4.0		Volts
V_{OL} (Note 2) Output LOW Voltage	$I_{OL} = 200\ \mu A$, 1407, 1507 only		−1.2	0.4	Volts
V_{IH} Input HIGH Voltage	$V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V	2.5	5.0	5.3	Volts
V_{IL} Input LOW Voltage	$V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V	−10	0.2	0.8	Volts
V_{IHC} Clock Input HIGH Voltage	$V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V	3.5		5.3	Volts
V_{ILC} Clock Input LOW Voltage	$V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V	−13		−9.5	Volts
I_L Input Load Current	Input Pin 1: Pins 2, 3, 4, 5, 6, 7 = 0 V; Pin 1 = −18 V; Pin 8 = −8 V; $T_A = 25°C$			500	nA
	Input Pin 7: Pins 1, 2, 3, 4, 5, 6 = 0 V; Pin 7 = −18 V; Pin 8 = −8 V; $T_A = 25°C$				
I_{LC} Clock Input Current	Clock Input Pins 3, 5 = −18 V; All Other Pins = 0 V; $T_A = 25°C$			500	nA
I_{LO} (Note 3) Output Leakage Current	Output Pin 2: Pins 1, 4, 6, 7, 8 = 0 V; Pin 2 = −18 V; Pins 3, 5 = −8 V			500	nA
	Output Pin 6: Pins 1, 2, 4, 7, 8 = 0 V; Pin 6 = −18 V; Pins 3, 5 = −8 V				
I_{DD} (See Graphs) Power Supply Current (Note 4)	f = 1MHz, Duty Cycle = 60%; $T_A = 25°C$		4.0	8.0	mA
	$T_A = 0°C$		5.0	10	
	$T_A = -55°C$		8.0	13	
Z_{out} Output ON Impedance	$V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V, $I_{OH} = -2.5$ mA		300	750	Ω
C_{IN} * Input Capacitance	Input Pins 1, 7; $V_{IN} = V_{CC}$			4	pF
C_ϕ * Clock Input Capacitance	Clock Input Pins 3, 5 $V_\phi = V_{CC}$			40	pF
	Clock Input Pins 3, 5 $V_\phi = -20$ V Bias			35	
C_{out} (Note 4) * Output Capacitance	Output Pins 2, 6; $V_{out} = V_{CC}$			5	pF

Note 1: Typical values are at $V_{CC} - V_{DD} = 10$ V and $T_A = 25°C$.

Note 2: In the logic HIGH level the MOS register output can supply 2.5 mA into the load combination of the internal pull-down resistor and the external load. In logic LOW level, I_{OL} represents the current the internal 20 kΩ resistor will sink. In order to insure current sinking capability for one standard TTL load, an external p down resistor must be added. See applications.

Note 3: Leakage current for 1406 and 1506 only. For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias c ditions: pins 1, 6, and 8 at GND; pins 3 and 5 at −16 V; pin 4 open; measure pins 2 and 6. 25 kΩ ≥ R_{OUT} ≥ 15 kΩ.

Note 4: Power dissipation is directly proportional to clock duty cycle. Duty cycle is defined as: clock frequency ($t\phi_1 pw + t\phi_2 pw + \frac{1}{2}[t_r + t_f]$).

***This paramenter is periodically sampled and is not 100% tested.**

SWITCHING CHARACTERISTICS ($V_{DD} = -5\ V \pm 5\%$; $V_{CC} = +5\ V \pm 5\%$ unless otherwise specified)

Parameter	Description	Test Conditions	Limits Over Specified Temperature Range Min.	Max.	Units
f_c	Clock Frequency	$V_{IH} \geq 3.0\ V$	(Note 5)	2	MHz
		$V_{IH} \geq 2.5\ V$		1	
$t_{\phi PW}$	Clock Pulse Width	$V_{IH} \geq 3.0\ V$	130		ns
		$V_{IH} \geq 2.5\ V$	200		
$t\phi_d$	Clock Pulse Delay	$\phi_{1\ PW} = 0.4\ \mu s$ $\phi_{2\ PW} = 0.2\ \mu s$ $f_c = 1\ MHz$	100		ns
t_f, t_r	Clock Pulse Rise/Fall Time	$f_c = 1\ MHz$		50	ns
t_s	Input Data Set Up Time	$f_c = 2\ MHz$	100		ns
		$f_c = 1\ MHz$	200		
t_h	Input Data Hold Time		100		ns
t_{pd}	Propagation Delay ϕ_1 to Output	$V_{ILC} - V_{CC} = -16\ V$		100	ns

Note 5: See "Minimum Operating Frequency" graph for low limits on clock rate.

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ESCRIPTION OF TERMS

PERATIONAL TERMS

OH Minimum logic HIGH output voltage with output HIGH current H flowing out of output.

OL Maximum logic LOW output voltage with output LOW current L into output.

H Logic HIGH input voltage.

L Logic LOW input voltage.

LC Clock LOW input voltage.

HC Clock HIGH input voltage.

Input load current.

Output leakage current.

Power supply current.

t Output impedance with output sourcing 2.5 mA.

Input capacitance.

Input clock capacitance.

UT Output capacitance.

NCTIONAL TERMS

ϕ_2 The two clock phases required by the dynamic shift register.

The clock frequency of the shift register.

SWITCHING TERMS

$t\phi_d$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

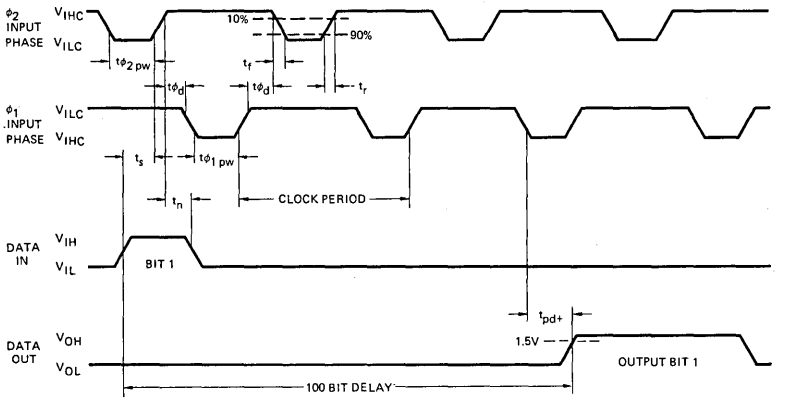
t_f, t_r The clock pulse rise and fall times necessary for correct operation.

t_s The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase ϕ_2 to ensure correct operation.

t_h The time required for the input data to remain present after the LOW to HIGH transition of the clock phase ϕ_2 to ensure correct operation.

t_{pd+} The propagation delay from the HIGH to LOW clock phase ϕ_1 transition to the output LOW to HIGH transition.

SWITCHING WAVEFORMS



Clock Rise Time 10ns
Clock Fall Time 10ns
Data Amplitude +0.8V to +2.5V
Output Load 1 TTL Unit Load

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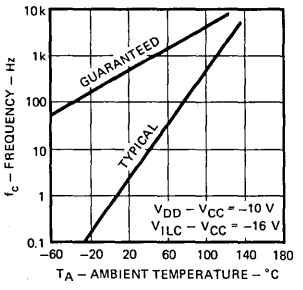
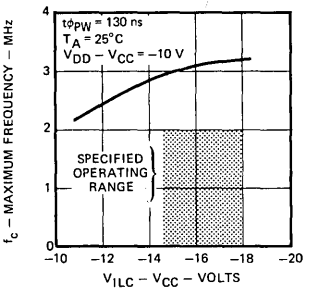
SWITCHING CHARACTERISTICS

Minimum Operating Frequency Versus Temperature



Maximum Frequency Versus Clock Amplitude



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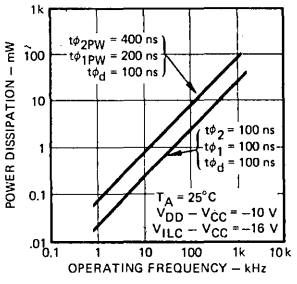
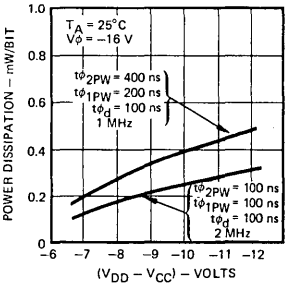
SWITCHING CHARACTERISTICS

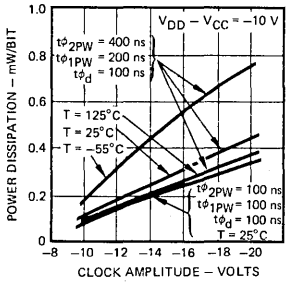
Power Dissipation Versus Frequency



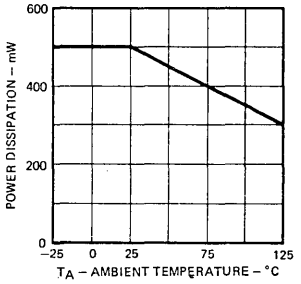
Power Dissipation/Bit Versus Supply Voltage



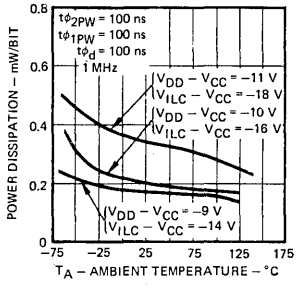
Power Dissipation/Bit Versus Clock Amplitude



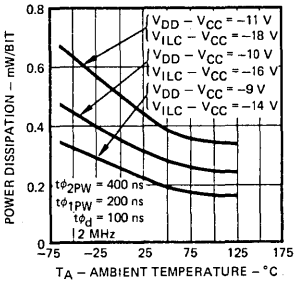
Maximum Package Power Dissipation Versus Temperature



Power Dissipation/Bit at 2 MHz Versus Temperature



Power Dissipation/Bit at 1 MHz Versus Temperature



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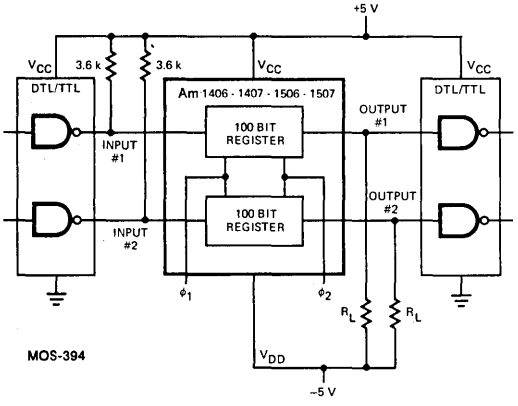
APPLICATIONS

DTL/TTL/MOS Interfaces

Dual 100-Bit Delay



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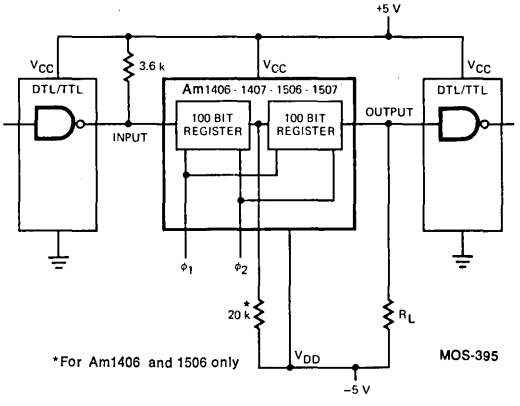
200-Bit Delay



*For Am1406 and 1506 only

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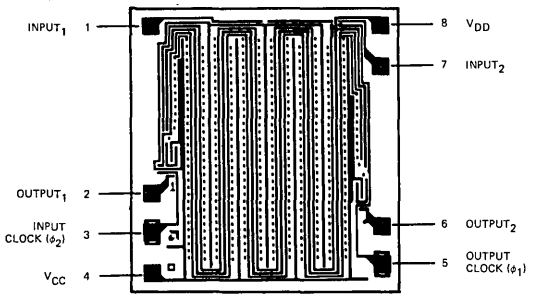
Value of R_L (V_{DO} = −5.0 ±5%)

Gate Type	1406, 1506	1407, 1507
Standard TTL	3.2k	3.8k
93L Low Power	12.8k	35k
74L Low Power	28k	none required

Metallization and Pad Layout



69 x 74 Mils