Am2814/3114

Dual 128-Bit Static Shift Register

Distinctive Characteristics

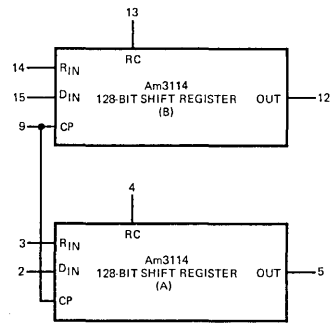
- 2nd Source to Texas Instruments 3114
- Operation guaranteed from DC to 2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883
- Full military grade devices available

FUNCTIONAL DESCRIPTION

The Am3114 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Both registers have a common clock input, and operate with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the D_{in} input; when RC is HIGH, data is accepted on the R_{in} input. The Am2814 is functionally identical to the Am3114, but is specified with higher performance.

LOGIC SYMBOL



V_{SS} = Pin 7
V_{DD} = Pin 6
V_{GG} = Pin 11

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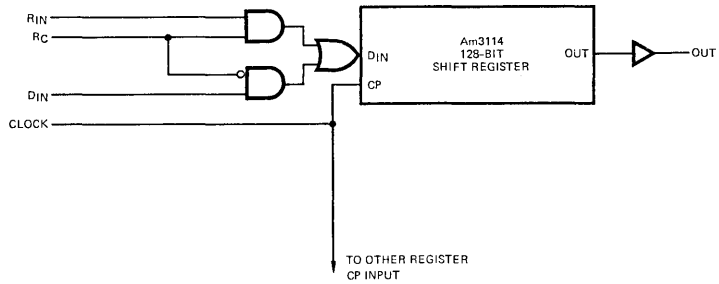
LOGIC BLOCK DIAGRAM (One Register Shown)



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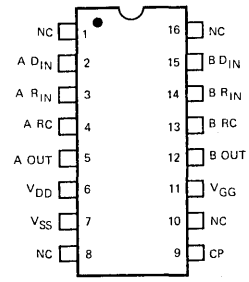
ORDERING INFORMATION

Package Type	Temperature Range	Am3114 Order Number	Am2814 Order Number
Molded DIP	−25°C to +85°C	TMS3114NC	AM2814PC
Hermetic DIP	−25°C to +85°C	TMS3114JC	AM2814DC
Hermetic DIP	−55°C to +125°C		AM2814DM

CONNECTION DIAGRAM



Notes: 1. Pin 1 is marked for orientation.
2. NC = No Connection.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −15V to V_{SS} +0.3V

OPERATING RANGE

Part Number	T_A	V_{SS}	V_{GG}	V_{DD}
Am2814PC, DC Am3114JC, NC	−25°C to +85°C	5.0V ±5%	−11V to −13V	GND
Am2814DM	−55°C to +125°C	5.0V ±5%	−11.4V to −12.6V	GND

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{SS}−1			Volts
V_{OH}	Output LOW Voltage	I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	Am3114	3.5			Volts
			Am2814	V_{SS} −1.5			
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.6	Volts
I_{IL}	Input LOW Current	V_{SS} = MAX., V_{IN} = 0.6V				0.5	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS}				0.5	μA
I_{SS}	V_{SS} Power Supply Current	Inputs and Outputs Open f = 1MHz	Am3114		15		mA
			Am2814XC		14	25	
			Am2814XM		14	35	
I_{GG}	V_{GG} Power Supply Current	Inputs and Outputs Open f = 1MHz	Am3114		−4		
			Am2814XC		−4	−10	
			Am2814XM		−4	−15	

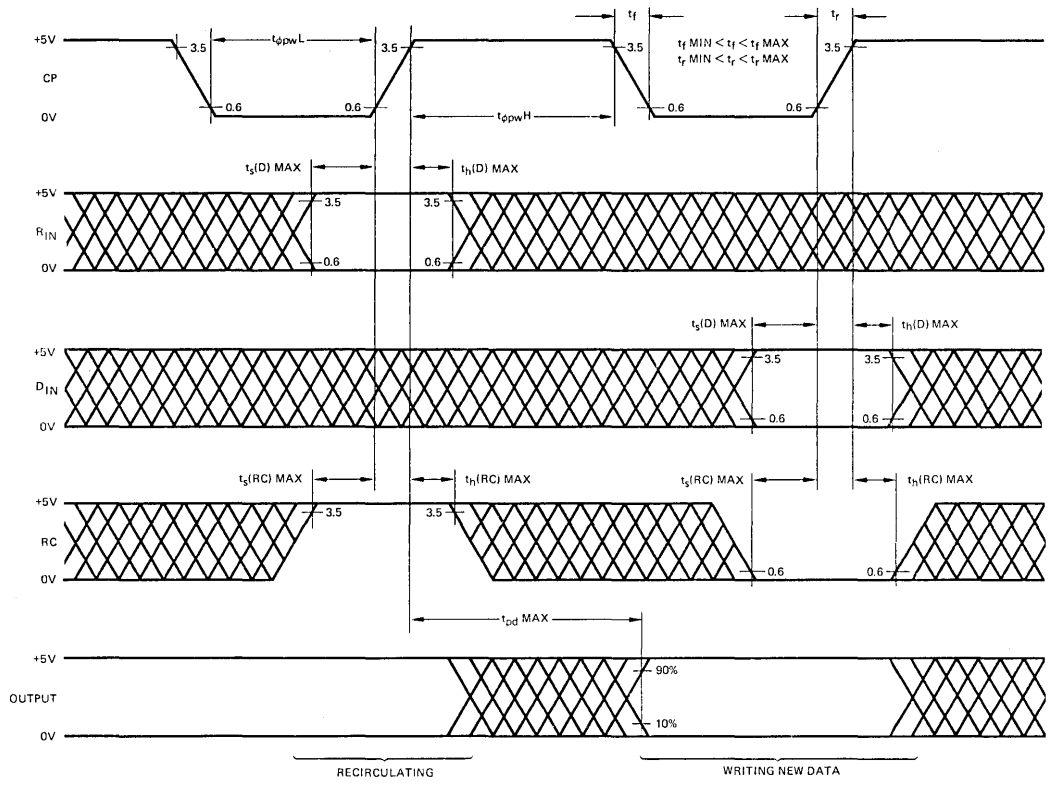
Note 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am3114 Min.	Am3114 Typ.	Am3114 Max.	Am2814 Min.	Am2814 Typ.	Am2814 Max.	Units
f_{max}	Maximum Clock Frequency		2.0			2.5			MHz
$t_{\phi pw}H$	Clock HIGH Time		.330		∞	.200		∞	μs
$t_{\phi pw}L$	Clock LOW Time		.130		100	.170		100	μs
t_r, t_f	Clock Rise and Fall Times				5			5	μs
t_s(D)	Set-up Time, D or R Inputs (see definitions)	t_r = t_f ≤ 50ns	100			100			ns
t_h(D)	Hold Time, D or R Inputs (see definitions)		100			100			ns
t_s(RC)	Set-up Time, RC Input (see definitions)		100			100			ns
t_h(RC)	Hold Time, RC Input (see definitions)		150			150			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.7k, C_L = 20pF			350	(Note 4)		250	ns
t_{pr}, t_{pF}	Output Rise and Fall Times	10% to 90%						100	ns
C_{in}	Capacitance, Any Input (Note 3)	f = 1MHz, V_{IN} = V_{SS}			13		3	7	pF

Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM



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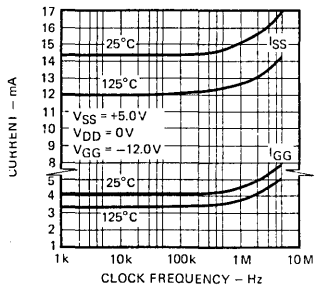
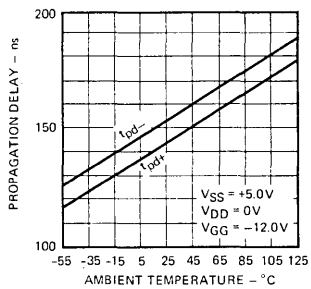
Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



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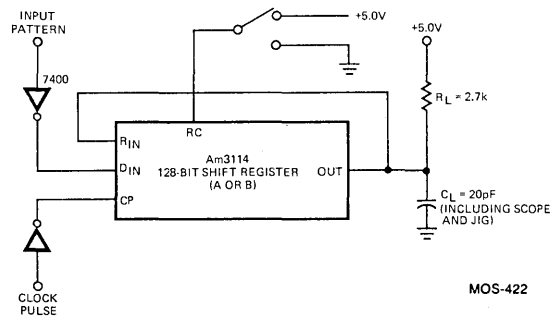
TEST CIRCUIT



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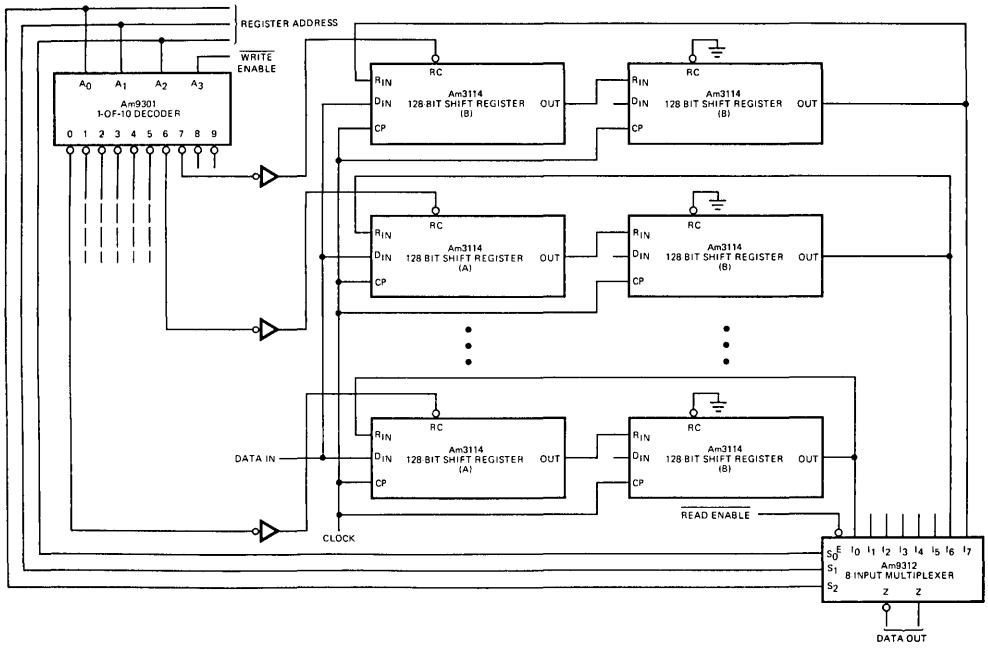
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS



Eight Register 256-Bit Memory System

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Pull-up resistors are required on all register inputs driven from TTL.

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TRUTH TABLE

RC	D_{IN}	R_{IN}	Data Entered
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care