Am2825 • Am2826 • Am2827

2048-Bit Dynamic Shift Registers

Distinctive Characteristics

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Plug-in replacement for National 5025/26/27
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

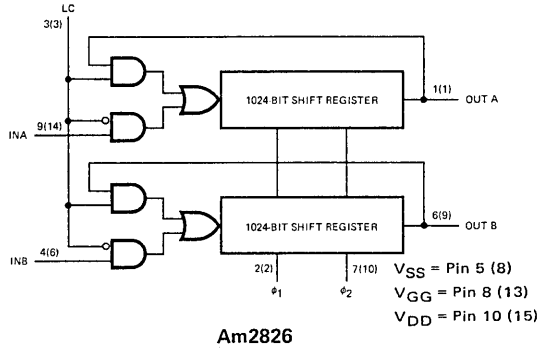
The Am2825/26/27 are military and commercial grade 2048-bit dynamic shift registers. The Am2825 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am2826 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am2827 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

ORDERING INFORMATION

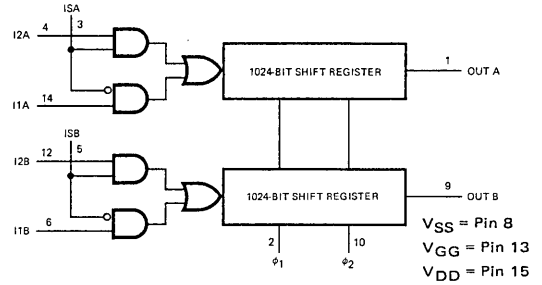
Package Type	Temperature Range	Order Number
10-Pin Molded	0°C to +70°C	AM2825PC
16-Pin Hermetic	0°C to +70°C	AM2825DC
16-Pin Hermetic	–55°C to +125°C	AM2825DM
16-Pin Molded	0°C to +70°C	AM2826PC
16-Pin Hermetic	0°C to +70°C	AM2826DC
16-Pin Hermetic	–55°C to +125°C	AM2826DM
8-Pin Molded	0°C to +70°C	AM2827PC
8-Pin Hermetic	–55°C to +125°C	AM2827DM
8-Pin Hermetic	0°C to +70°C	AM2827DC

LOGIC DIAGRAMS

Am2825



Am2826



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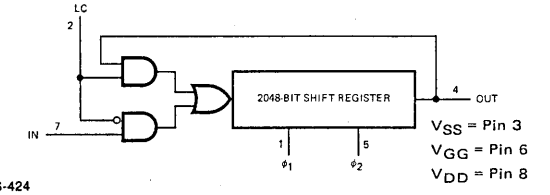
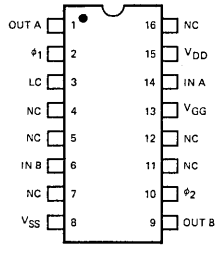


MOS-424

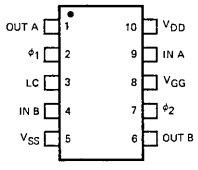
CONNECTION DIAGRAMS

Top View

Am2825



Am2825



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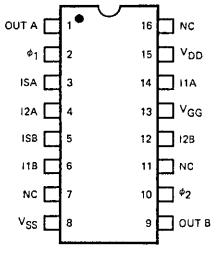
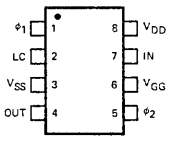


Am2827



MOS-425

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
DC Input Voltage with Respect to V_{SS}	−20V to +0.3V

OPERATING RANGE

Part Number	V_{SS}	V_{DD}	V_{GG}	T_A
AM2825/6/7DM	+5.0V ±5%	0V	−10.0V to −11.0V	−55°C to +125°C
AM2825/6/7PC,DC	+5.0V ±5%	0V	−10.0V to −11.0V	0°C to +70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = −0.5mA		2.4		V_{SS}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA		0.0		0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs except clocks		V_{SS} −1.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs except clocks		V_{SS} −10		V_{SS} −4.2	Volts
I_I	Input Leakage Current	V_{IN} = −10V, T_A = 25°C			10	500	nA
I_ϕ	Clock Input Leakage Current	V_ϕ = −15V, T_A = 25°C			50	1000	nA
$V_{\phi H}$	Clock HIGH Level			V_{SS} −1.0		V_{SS} +0.3	Volts
$V_{\phi L}$	Clock LOW Level			V_{GG} −0.3		V_{GG} +0.8	Volts
I_{GG}	V_{GG} Current	T_A = 25°C V_{SS} = 5.25V V_{GG} = −11.0V $V_{\phi L}$ = −11.0V $t_{\phi pw}$ = 125ns Data = 11110000...	.01MHz<f_ϕ<0.1MHz		2.5	5	mA
			f_ϕ = 1.0MHz		2.5	5	
			f_ϕ = 3.0MHz		2.5	5	
I_{DD}	V_{DD} Current		.01MHz<f_ϕ<0.1MHz		4	6	mA
			f_ϕ = 1.0MHz		20	30	
			f_ϕ = 3.0MHz		45	65	

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −10.5V and 25°C ambient.

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

Parameters	Definition	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
f_D	Data Rate (Note 2)	T_A = 0°C to +70°C		0.02		6.0	MHz
		T_A = −55°C to +125°C		0.12		4.0	
f_ϕ	Clock Frequency (Note 3)	T_A = 0°C to +70°C		0.01		3.0	
		T_A = −55°C to +125°C		0.06		2.0	
$t_{\phi d}$	Delay Between Clocks (Note 3)			10		Note 3	ns
$t_{\phi pw}$	Clock LOW Time	$t_{\phi t}$ = 20ns	0°C to +70°C	0.125		10	µs
			−55°C to +125°C	0.180		10	
$t_{\phi t}$	Clock Rise and Fall Times	10% to 90%				0.5	µs
t_s	Set-Up Time, Data and Select Inputs (See Definitions)		0°C to 70°C	40			ns
			−55°C to +125°C	60			
t_h	Hold Time, Data and Select Inputs (See Definitions)		0°C to 70°C	30			ns
			−55°C to +125°C	50			
t_{pd}	Delay, Clock to Data Out	C_L = 15pF	0°C to +70°C			80	ns
			−55°C to +125°C			120	
$C_{(D)}$	Capacitance, Data Input	Note 4 f = 1 MHz, V_{IN} = 0V All other pins at GND				5	pF
$C_{(S)}$	Capacitance, Select Input or L_C					7	pF
$C_{(\phi)}$	Capacitance, Clock Input				175	220	

Notes: 2. The Data Rate is twice the frequency of either clock phase.
3. The maximum delay between clocks (ϕ_1 and ϕ_2 both HIGH) is a function of junction temperature. The junction temperature is a functi of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TRUTH TABLES

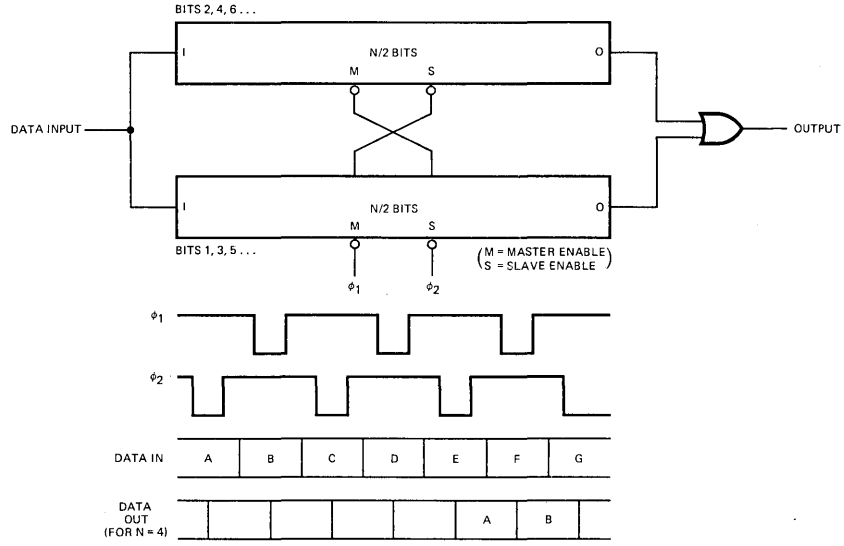
Am2825 and Am2827

LC	IN	OUT	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Am2826

IS	INPUT 1	INPUT 2	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

FUNCTIONAL EQUIVALENT OF EACH REGISTER



Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2. Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

MOS-426

EFINITION OF TERMS

namic Shift Register A shift register in which data storage ;urs on small capacitive nodes rather than in bistable logic ;uits. Dynamic shift registers must be clocked continuously to intain the charge stored on the nodes.

, ϕ**2** The two clock pulses applied to the register. The clock is I when it is at its negative voltage level and OFF when it is at ;. Data is accepted into the master of each bit during one ıse and is transferred to the slave of each bit during the other ıse.

Clock delay time. The time elapsing between the LOW-to-3H transition of one clock input and the HIGH-toLOW tran-on of the other clock input. During $t_{\phi d}$ both clocks are HIGH l all data is stored on capacitive nodes.

$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

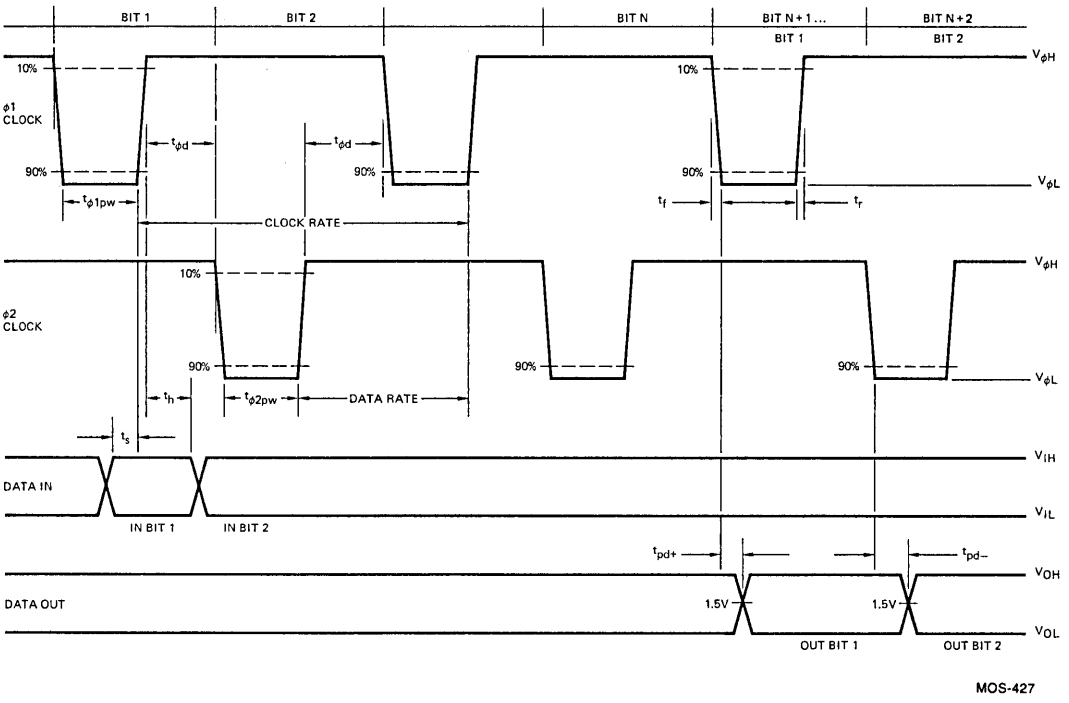
$t_{\phi t}$ Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

t_s**(D)** Data set-up time. The time prior to the LOW-to-HIGH transition of ϕ during which the data on the data input must be steady to be correctly written into the memory.

t_h**(D)** Data hold time. The time following the LOW-to-HIGH transition of ϕ during which the data must be steady. To correctly write data into the register, the data must be applied by t_s(D) before this transition and must not be changed until t_h(D) after this transition.

t_{pd} The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

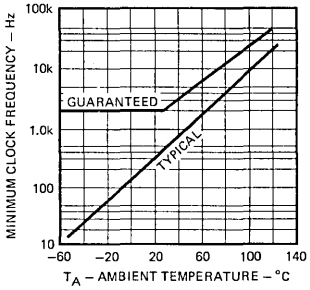
SWITCHING WAVEFORMS



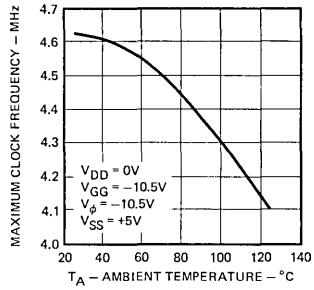
Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

OPERATING CHARACTERISTICS

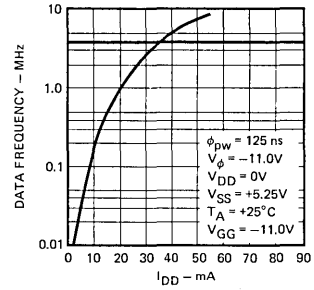
Guaranteed Minimum Clock Frequency Versus Temperature



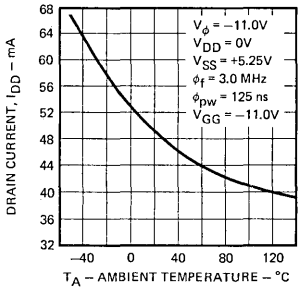
Maximum Clock Frequency Versus Temperature



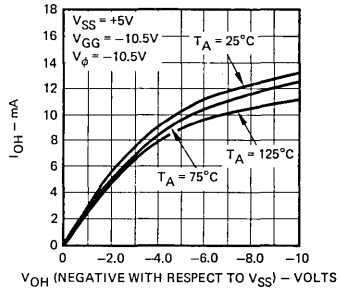
Typical Power Supply Current Versus Data Rate



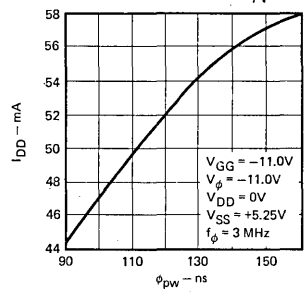
Typical Power Supply Current Versus Temperature



V_{OH} Versus I_{OH}



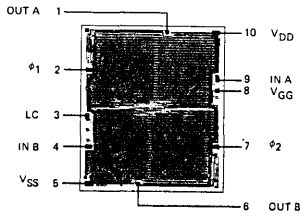
Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$



MOS-428

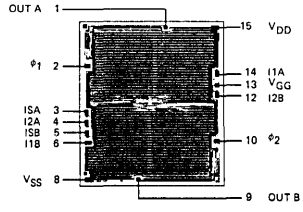
Metallization and Pad Layouts

Am2825



DIE SIZE 0.145" X 0.162"

Am2826



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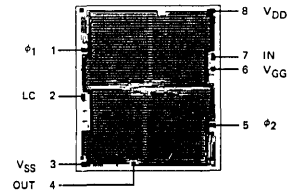
Am2827



DIE SIZE 0.145" X 0.162"