PRELIMINARY

AMD

Am29F002NT/Am29F002NB

2 Megabit (262,144 x 8-Bit)
CMOS 5.0 Volt-only, Sector Architecture Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system-level power requirements
- **Compatible with JEDEC-standard commands**
  - — Pinout and software compatible with single-power-supply flash standards
  - — Superior inadvertent write protection
- **Package options**
  - — 32-pin PDIP
  - — 32-pin PLCC
  - — 32-pin TSOP
- **Minimum 100,000 write erase cycles guaranteed**
- **High performance**
  - — Access times as fast as 55 ns
- **Sector architecture**
  - — One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and three 64 Kbytes
  - — Any combination of sectors can be erased. Also supports full chip erase.
- **Sector protection**
  - — Hardware method that disables any combination of sectors from write or erase operations. Implemented using standard PROM programming equipment.
- **Embedded Erase Algorithm**
  - — Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithm**
  - — Automatically programs and verifies data at a specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature**
  - — Detects program or erase cycle completion
- **Erase Suspend/Resume**
  - — Supports reading data from or programming data to a sector not being erased
- **Low power consumption**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
- **Enhanced power management for standby mode**
  - — 400 µA typical TTL standby current
  - — 1 µA typical CMOS standby current
  - — Standard access time from standby modes
- **Boot code sector architecture**
  - — T = Top sector
  - — B = Bottom sector
- **Low V_{CC} write inhibit ≤ 3.2 V**

GENERAL DESCRIPTION

The Am29F002N is a 2 Mbit, 5.0 Volt-only Flash memory organized as 256 Kbytes of 8 bits each. The 2 Mbits of data is divided into 7 sectors of one 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and three 64 Kbytes, for flexible erase capability. The 8 bits of data appear on DQ0-DQ7. The Am29F002N is offered in a 32-pin PDIP, PLCC, and TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A power supply providing 12.0 Volt V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F002N offers access times of 55 ns, 70 ns, 90 ns, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$) controls.

The Am29F002N is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

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The Am29F002N is programmed by executing the program command sequence, which invokes the Embedded Program Algorithm. This internal algorithm automatically times the program pulse widths and verifies proper cell margin. The Am29F002N is erased by executing the erase command sequence, which invokes the Embedded Erase Algorithm. Before executing the erase operation, this internal algorithm automatically preprograms the array if it is not already programmed. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture, which allows sectors of memory to be erased and reprogrammed without affecting the data contents of other sectors. A sector is typically erased and verified within one second if already pre-programmed. The Am29F002N is erased when shipped from the factory.

The Am29F002N also features hardware sector protection. This feature disables both program and erase operations in any combination of the seven sectors of memory.

AMD has implemented an Erase Suspend/Resume feature that enables the user to put erase on hold for any period of time to read data from or program data to a sector not being erased. Thus, true background erase can be achieved.

The device features single 5.0 Volt power supply operation for both read and write functions.

Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations when a loss of device power occurs. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7, or by the Toggle Bit (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The Am29F002N memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection. AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness.

FLEXIBLE SECTOR ARCHITECTURE

- One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and three 64 Kbyte sectors
- Individual-sector or multiple-sector erase capability
- Sector protection is user definable

Sector	Sector Size	Address Range
SA6	16 Kbytes	3C000h-3FFFFh
SA5	8 Kbytes	3A000h-3BFFFh
SA4	8 Kbytes	38000h-39FFFh
SA3	32 Kbytes	30000h-37FFFh
SA2	64 Kbytes	20000h-2FFFFh
SA1	64 Kbytes	10000h-1FFFFh
SA0	64 Kbytes	00000h-0FFFFh

Am29F002NT Sector Architecture

Sector	Sector Size	Address Range
SA6	64 Kbytes	30000h-3FFFFh
SA5	64 Kbytes	20000h-2FFFFh
SA4	64 Kbytes	10000h-1FFFFh
SA3	32 Kbytes	08000h-0FFFFh
SA2	8 Kbytes	06000h-07FFFh
SA1	8 Kbytes	04000h-05FFFh
SA0	16 Kbytes	00000h-03FFFh

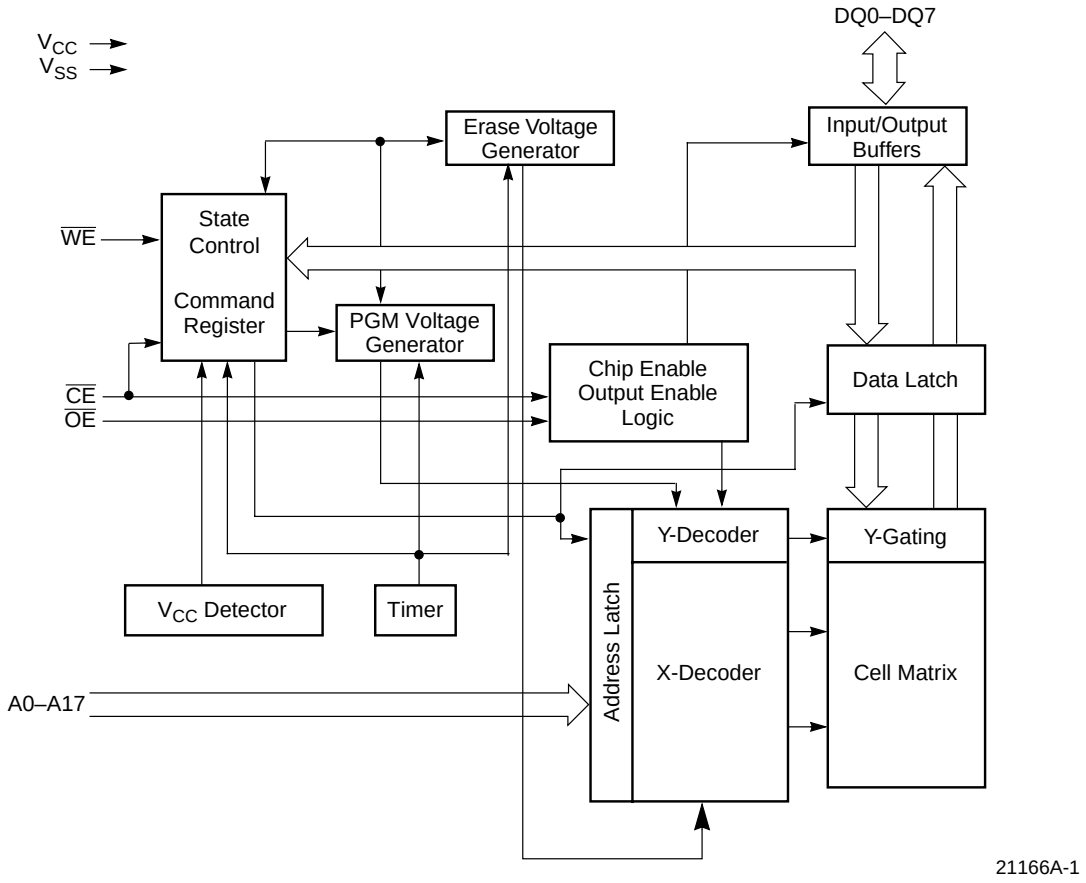
Am29F002NB Sector Architecture

Notes:
Refer to Table 3 and Table 4 for a more information on addresses.

PRODUCT SELECTOR GUIDE

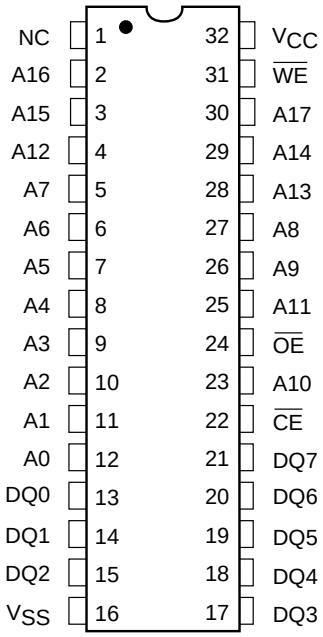
Family Part No:	Am29F002N			
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-55**			
V_{CC} = 5.0 V ± 10%		**-70**	**-90**	**-120**
Max Access Time (ns)	55	70	90	120
$\overline{CE}$ Access (ns)	55	70	90	120
$\overline{OE}$ Access (ns)	30	30	35	50

BLOCK DIAGRAM



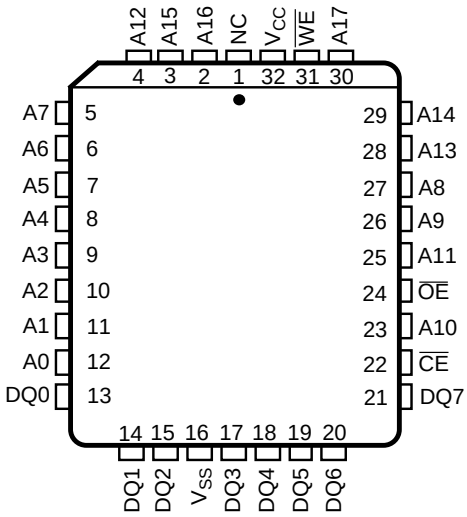
CONNECTION DIAGRAMS

PDIP



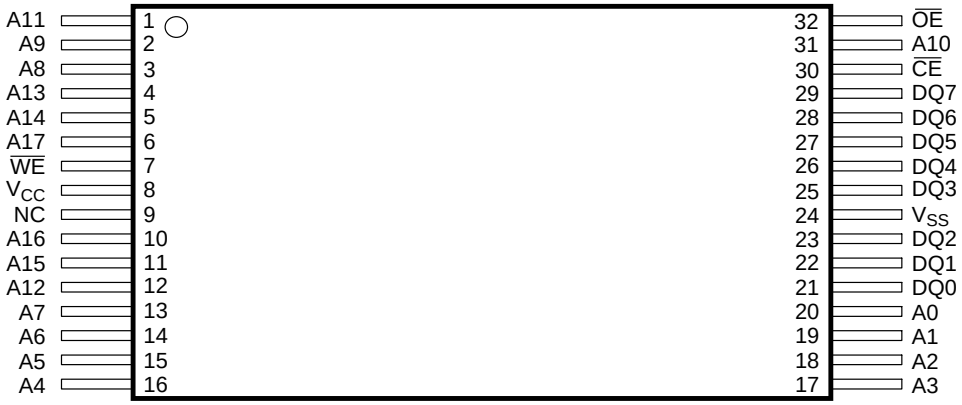
21166A-2

PLCC



21166A-3

Standard TSOP

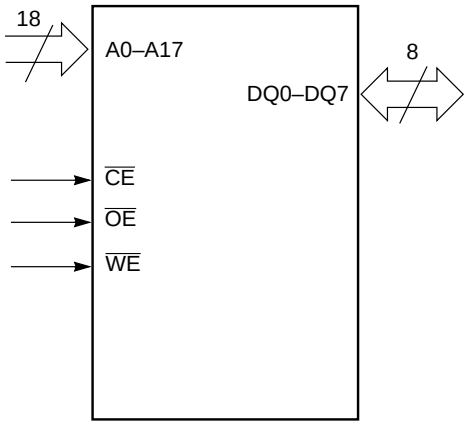


21166A-4

PIN DESCRIPTION

A0-A17	=	18 Addresses
DQ0-DQ7	=	8 Data Inputs/Outputs
$\overline{CE}$	=	Chip Enable
$\overline{WE}$	=	Write Enable
$\overline{OE}$	=	Output Enable
V_{CC}	=	+5.0 Volt Single Power Supply (±5% for -55) or (±10% for -70, -90, -120)
V_{SS}	=	Device Ground

LOGIC SYMBOL

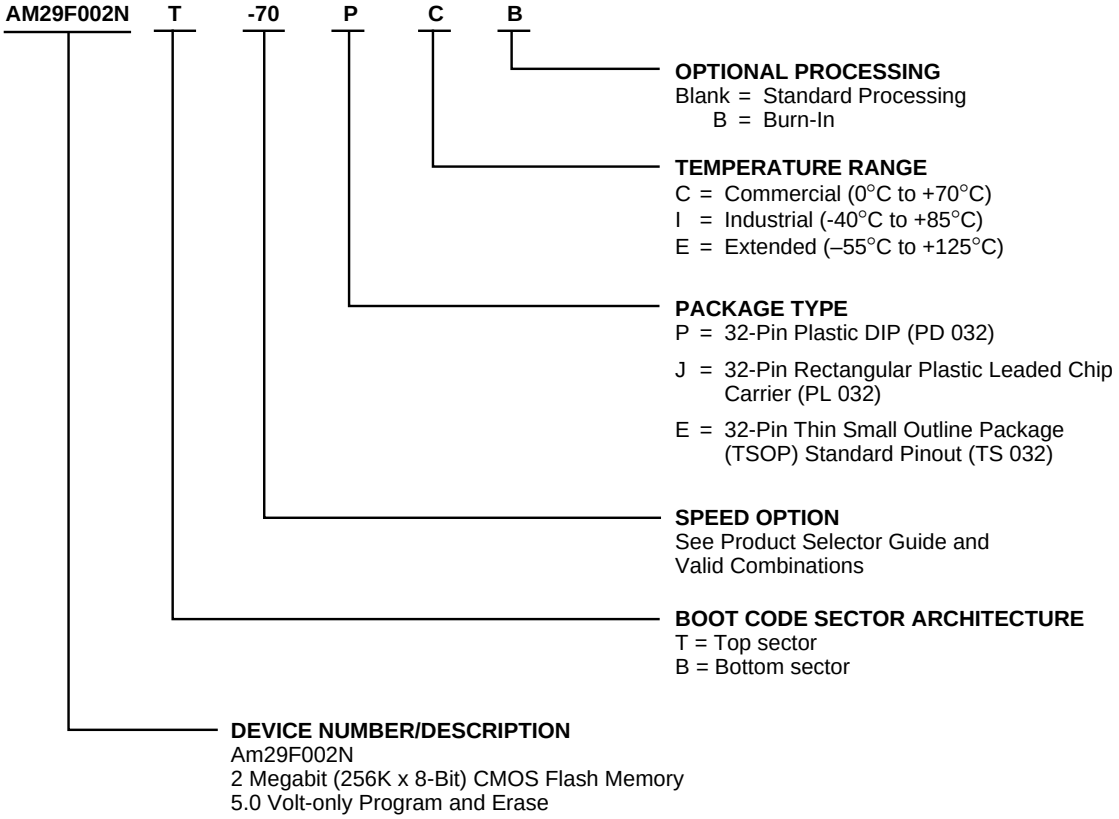


21166A-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F002NT/B-55	PC, JC, JI, EC, EI
AM29F002NT/B-70	PC, PI, JC, JI, EC, EI
AM29F002NT/B-90	PC, PI, PE, JC, JI, JE, EC, EI, EE
AM29F002NT/B-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1. Am29F002N User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ7
Autoselect Manufacturer Code (Note 1)	L	L	H	L	L	L	V_{ID}	CODE
Autoselect Device Code (Note 1)	L	L	H	H	L	L	V_{ID}	CODE
Read	L	L	H	A0	A1	A6	A9	RD
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	PD (Note 2)
Enable Sector Protect (Note 3)	L	V_{ID}	L	X	X	L	V_{ID}	X
Verify Sector Protect	L	L	H	L	H	L	V_{ID}	CODE

Legend:

L = V_{IL}, H = V_{IH}, V_{ID} = 12.0 ± 0.5 Volts, X = Don't Care. See DC Characteristics on page 19 for voltage levels.

PD = program data, RD = read data. Refer to Table 5 for more information.

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5.*
2. *Refer to Table 5 for valid PD during a write operation.*
3. *Refer to "Sector Protection" on page 9.*

Read Mode

The Am29F002N has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time (t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time).

Standby Mode

The standby mode is supported on the Am29F002N for both TTL- and CMOS-compatible operation, and is enabled using the $\overline{CE}$ pin.

The device enters the CMOS-compatible standby mode when the $\overline{CE}$ pin is held at V_{CC} ± 0.3 V. Under this condition the current is typically reduced to less than 1 µA. The device enters the TTL-compatible standby mode when the $\overline{CE}$ pin is held at V_{IH}. Under this condition the current is typically reduced to 400 µA. *The device can be read with standard access time (t_{CE}) from either of these standby modes.*

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6 (see Table 2).

The manufacturer and device codes may also be read via the command register for instances when the Am29F002N is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 5.

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F002NT = B0H and Am29F002NB = 34H). These two bytes are given in Table 2. All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A1 must be V_{IL} (see Table 2).

The Autoselect mode also facilitates the determination of sector protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A13 - A17 set to the desired sector address, the device will return 01H for a protected sector and 00H for a non-protected sector.

Table 2. Am29F002N Autoselect and Sector Protection Verify Codes

Type	A13-A17	A6	A1	A0	Code (Hex)	DQ 7	DQ 6	DQ 5	DQ 4	DQ 3	DQ 2	DQ 1	DQ 0
AMD Manufacturer Code	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
29F002 Device (Top Boot Block)	X	V_{IL}	V_{IL}	V_{IH}	B0H	1	0	1	1	0	0	0	0
29F002 Device (Bottom Boot Block)	X	V_{IL}	V_{IL}	V_{IH}	34H	0	0	1	1	0	1	0	0
Sector Protection	Sector Addresses	V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

** Outputs 01H at protected sector addresses and 00H at non-protected sector addresses.*

Table 3. Sector Address Tables (Am29F002NT)

Sector	A17	A16	A15	A14	A13	Sector Size	Address Range
SA0	0	0	X	X	X	64 Kbytes	00000h-0FFFFh
SA1	0	1	X	X	X	64 Kbytes	10000h-1FFFFh
SA2	1	0	X	X	X	64 Kbytes	20000h-2FFFFh
SA3	1	1	0	X	X	32 Kbytes	30000h-37FFFh
SA4	1	1	1	0	0	8 Kbytes	38000h-39FFFh
SA5	1	1	1	0	1	8 Kbytes	3A000h-3BFFFh
SA6	1	1	1	1	X	16 Kbytes	3C000h-3FFFFh

Table 4. Sector Address Tables (Am29F002NB)

Sector	A17	A16	A15	A14	A13	Sector Size	Address Range
SA0	0	0	0	0	X	16 Kbytes	00000h-03FFFh
SA1	0	0	0	1	0	8 Kbytes	04000h-05FFFh
SA2	0	0	0	1	1	8 Kbytes	06000h-07FFFh
SA3	0	0	1	X	X	32 Kbytes	08000h-0FFFFh
SA4	0	1	X	X	X	64 Kbytes	10000h-1FFFFh
SA5	1	0	X	X	X	64 Kbytes	20000h-2FFFFh
SA6	1	1	X	X	X	64 Kbytes	30000h-3FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the commands. The command register is written to by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F002N features hardware sector protection. This feature will disable both program and erase operations in any combination of seven sectors of memory. The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD offers ExpressFlash™, a value-added service that provides customers with programmed, sector-protected Flash devices direct from the factory.

It is possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address bits (A17, A16, A15, A14, and A13) are the desired sector address, will produce a logical “1” at DQ0 for a protected sector and a logical “0” for a non-protected sector. See Table 2 for Autoselect codes.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. In addition, note that both Read/Reset commands are functionally equivalent for resetting the device to the read mode.

Read/Reset Command

The read or reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reading data until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 5. Am29F002N Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	555H	AAH	AAAH	55H	555H	F0H	RA	RD				
Autoselect Manufacturer ID	4	555H	AAH	AAAH	55H	555H	90H	00H	01H				
Autoselect Device ID (Top Boot Device)	4	555H	AAH	AAAH	55H	555H	90H	01H	B0H				
Autoselect Device ID (Bottom Boot Device)	4	555H	AAH	AAAH	55H	555H	90H	01H	34H				
Autoselect Sector Protect Verify (Note 4)	4	555H	AAH	AAAH	55H	555H	90H	SA/ 02H	00H				
									01H				
Byte Program	4	555H	AAH	AAAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	AAAH	55H	555H	80H	555H	AAH	AAAH	55H	555H	10H
Sector Erase	6	555H	AAH	AAAH	55H	555H	80H	555H	AAH	AAAH	55H	SA	30H
Sector Erase Suspend (Note 5)	1	XXXH	B0H										
Sector Erase Resume (Note 5)	1	XXXH	30H										

Legend:

Addr = Address. Note that addresses A12–A17 are don't care, except for RA, PA, and SA.
RA = Read Address: address of the memory location to be read.
RD = Read Data: Data read from location RA during read operation.
PA = Program Address: address of the memory location to be programmed.
PD = Program Data: data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.
SA = Sector Address: address of the sector to be erased. Address bits A17–A13 together uniquely select any sector.

Notes:

1. *Bus operations are defined in Table 1.*
2. *Addresses are latched on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse.*
3. *Reading from and programming to non-erasing sectors is allowed in the Erase Suspend mode.*
4. *The device returns 00H for an unprotected sector and 01H for a protected sector.*
5. *The Sector Erase Suspend and Sector Erase Resume commands are valid only during sector erase.*

Autoselect Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacturer code of 01H. A read cycle from address XX01H returns the device code (Am29F002NT = B0H and Am29F002NB = 34H) (see Table 2).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Furthermore, the write protect status of sectors can be read in this mode. Scanning the sector addresses A17–A13 while holding A6, A1, A0 at 0,1,0, respectively, (equivalent to asserting 02H on A7–-A0) produces a logical "1" at device output DQ0 for a protected sector and a logical "0" for a non-protected sector.

To terminate the autoselect operation, it is necessary to write the Read/Reset command sequence to the command register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) initiates programming. The system is not required to provide further controls or timings while the Embedded Program algorithm is in progress. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. Any commands written to the chip during the Embedded Program algorithm will be ignored.

The automatic programming operation is completed when the data on DQ7 (also used for $\overline{Data}$ Polling) is equivalent to the data written to this bit (see Table 6). The device then immediately returns to the read mode and addresses are no longer latched. Therefore, the device requires that the system provide a valid address. The sector address used during $\overline{Data}$ Polling must the same as that of the location being programmed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may cause the device to exceed programming time limits (DQ5 = 1) or result in an apparent success, according to the $\overline{Data}$ Polling algorithm, but a read from Read/Reset mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Program Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erasing. Upon executing the Embedded Erase algorithm command sequence the device automatically programs and verifies the entire memory for an all zero data pattern before erasing to an all one data pattern. The erase is performed sequentially, one sector at a time (see "Erase And Programming Performance" on page 29 for erase times). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see "Write Operation Status" on page 12). At that time, the device returns to the read mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six-bus-cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. After a time-out of 80 µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased sequentially by writing the six-bus-cycle operation just described. This sequence is followed with additional Sector Erase commands to other sector addresses. The time between these commands must be less than 80 µs, otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The time-out begins at the rising edge of the last $\overline{WE}$ or $\overline{CE}$. If another falling edge of $\overline{WE}$ or $\overline{CE}$ occurs within the 80 µs time-out window, the timer will be reset. The interrupts can be re-enabled after the last Sector Erase command is written. Monitoring DQ3 will determine whether the sector erase time-out window is still open (see "DQ3 Sector Erase Timer"). During this window, only the Sector Erase or Erase Suspend command is allowed. Any other command resets the device to the read mode and cancels the previous sector erase command. In this case, restart the erase on the desired sectors and allow for completion of the erase procedure. The sector erase buffer may be loaded in any sequence of up to seven sectors (0 to 6).

Sector erase does not require the user to program the device prior to erasing. Upon executing the sector erase command sequence, the device automatically programs and verifies the selected sectors for an all zero data pattern before erasing to an all one data pattern. When performing a sector erase, sectors that are protected or not selected for erasure will not be changed. The system is not required to provide any controls or timings during these operations.

The automatic sector erase is complete when the data on DQ7, $\overline{Data}$ Polling, is "1" (see "Write Operation Status"). The device then returns to the read mode. During the execution of the sector erase command, only the erase suspend and erase resume commands are allowed. All other commands are ignored. $\overline{Data}$

Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

The erase suspend command allows the user to interrupt a sector erase operation and then read data from or program data to a sector not being erased. This command is applicable *only* during the sector erase operation including the associated time-out period for sector erase. The erase suspend command will be ignored if written during a program or chip erase operation. Writing the erase suspend command during the sector erase time-out results in termination of the time-out period and suspension of the erase operation.

Any commands other than the read, program, or erase resume commands written during the erase suspend mode will be ignored. Writing the erase resume command resumes the erase operation. The addresses are “don’t cares” when writing the erase suspend or erase resume command.

When the erase suspend command is written during the sector erase operation, the device will take a maximum of 20 µs to suspend the erase operation. When the device has entered the erase-suspended mode, DQ7 will be at a logic “1”, and DQ6 will stop toggling. The user must use the address of an erasing sector when reading DQ6 and DQ7 to determine if the erase operation has been suspended. Further writes of the erase suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspended read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Monitor DQ2 to determine if a sector is being erased. DQ2, the erase toggle bit, will toggle with $\overline{OE}$ or $\overline{CE}$, when a read is attempted within a sector that is being erased. (see “Write Operation Status”).

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. The device then enters the erase-suspend-program mode. All conditions that apply to Byte Program also apply in this mode, except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode causes DQ2 to toggle. The completion of the erase-suspend-program operation is detected by $\overline{Data}$ Polling of DQ7, or by the Toggle Bit (DQ6), just as in Byte Program operations. Note that DQ7 must be read from the byte program address while DQ6 can be read from any address. See the following section, “Write Operation Status”, for information on DQ7, DQ6, and DQ2.

To resume the operation of sector erase, the erase resume command (30H) must be written. Any further writes of the resume command are ignored. The erase suspend command can be written again after the chip has resumed erasing.

Write Operation Status

There are several methods for determining the state of the Am29F002N during write operations.

DQ7
$\overline{Data}$ Polling

The Am29F002N provides $\overline{Data}$ Polling on DQ7 to indicate to the host system whether the Embedded Algorithms are in progress or completed. The $\overline{Data}$ Polling feature is active during the Embedded Program algorithm, Embedded Erase algorithm, erase suspend, program, and sector erase time-out (see Table 6 on page 14).

If the host system attempts to read ($\overline{Data}$ poll) the device while the Embedded Program algorithm is in progress, the device produces the complement of the data last written to DQ7. If the host system attempts to read the device after the Embedded Program algorithm is complete, the device produces the true data last written to DQ7. For the Embedded Program algorithm, $\overline{Data}$ Polling is valid after the rising edge of the fourth $\overline{WE}$ or $\overline{CE}$ pulse in the four-cycle sequence.

During the Embedded Erase algorithm, an attempt to read the device produces a “0” at the DQ7 output. After the Embedded Erase algorithm is complete, an attempt to read the device produces a “1” at the DQ7 output. For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ or $\overline{CE}$ pulse in the six cycle sequence. For sector erase, $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ or $\overline{CE}$ pulse.

$\overline{Data}$ Polling can be done at any address within a sector that is being programmed or erased. $\overline{Data}$ Polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of Embedded Algorithm operations, DQ7 may change asynchronously when the output enable ($\overline{OE}$) is low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempt.

The flowchart for $\overline{Data}$ Polling (DQ7) is shown in Figure 3; the $\overline{Data}$ Polling timing specifications and diagrams are shown in Figure 11.

DQ6
Toggle Bit

The Am29F002N provides a "Toggle Bit" on DQ6 as another method of indicating to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Program or Embedded Erase algorithms, successive attempts to read data from the device at any address (by toggling $\overline{OE}$ or $\overline{CE}$) results in DQ6 toggling. Once the Embedded Program or Erase algorithm is complete, DQ6 will stop toggling and valid data will be read on the next attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four cycle sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six cycle sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector erase time-out window.

If a program command is sent to a protected sector, DQ6 toggles for ~2 µs, then returns to the read mode; the data in the sector is not changed. An erase command erases only sectors that are *not* protected. If all selected sectors are protected, the chip will toggle DQ6 for ~100 µs, then return to the read mode; no chip data is changed.

Toggling either $\overline{CE}$ or $\overline{OE}$ toggling causes DQ6 to toggle. An Erase Suspend/Resume command also causes DQ6 to toggle.

The flowchart for the Toggle Bit (DQ6) is shown in Figure 4; the Toggle Bit timing specifications and diagrams are shown in Figure 12.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling (DQ7), Toggle Bit (DQ6), and Erase Toggle Bit (DQ2) still function under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1, "Am29F002N User Bus Operations," on page 7.

The DQ5 failure condition will also appear if a user tries to program a "1" to a location that was previously programmed to "0." In this case the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads valid data on DQ7 and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was used incorrectly. If timing limits are exceeded, reset the device.

DQ3
Sector Erase Timer

After the completion of the initial Sector Erase command sequence the Sector Erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{Data}$ Polling and the Toggle Bit are valid after the initial Sector Erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid Sector Erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun, attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or the Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted. Refer to Table 6, "Hardware Sequence Flags," on page 14.

DQ2
Erase Toggle Bit

In the Sector Erase operation, DQ2 will toggle with $\overline{OE}$ or $\overline{CE}$ when a read is attempted within the sector that is being erased. DQ2 will NOT toggle if the read address is NOT within the sector that is being erased. In the chip erase operation, however, DQ2 will toggle with $\overline{OE}$ or $\overline{CE}$ regardless of the address given by the user because all sectors have been selected to be erased (see Table 6).

When erasing multiple sectors, DQ2 can be used to indicate which sector is being erased. DQ2 can also be used to detect which sector exceeded timing limits during erasure, if such an error occurs. When DQ5 is high ("1"), DQ2 will toggle only if the address applied is within the sector that exceeded timing limits. DQ2 will not toggle if the address applied is not within the sector that exceeded timing limits.

Table 6. Hardware Sequence Flags

Operations	Status		DQ7	DQ6	DQ5	DQ3	DQ2
In Progress	Byte Program in Embedded Program Algorithm		$\overline{DQ7}$	Toggle	0	0	No Toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Note 1
	Erase Suspend Mode	Read Erasing Sector	1	1	0	0	Toggle
		Read Non-erasing Sector	Data	Data	Data	Data	Data
		Program in Erase Suspend	$\overline{DQ7}$	Toggle	0	0	Note 1
Exceeded Time Limits	Byte Program in Embedded Program Algorithm		$\overline{DQ7}$	Toggle	1	0	No Toggle
	Erase during Embedded Erase		0	Toggle	1	1	Note 2
	Program in Erase Suspend		$\overline{DQ7}$	Toggle	1	0	Note 2

Notes:

1. *DQ2 will toggle (with $\overline{OE}$ or $\overline{CE}$) if the sector address applied is of an erasing sector. DQ2 will not toggle if the address applied is not within an erasing sector. DQ2 is used for indicating which sector is being erased.*
2. *If DQ5=1, DQ2 will toggle if the address applied is within the sector that exceeded timing limits. DQ2 will NOT toggle for an address in any other sector.*

Data Protection

The Am29F002N is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine to the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the Am29F002N locks out write cycles for $V_{CC} < V_{LKO}$ (see “DC Characteristics” on page 19 and page 20 for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The Am29F002N ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logical state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will neither initiate a write cycle nor change the command registers.

Logical Inhibit

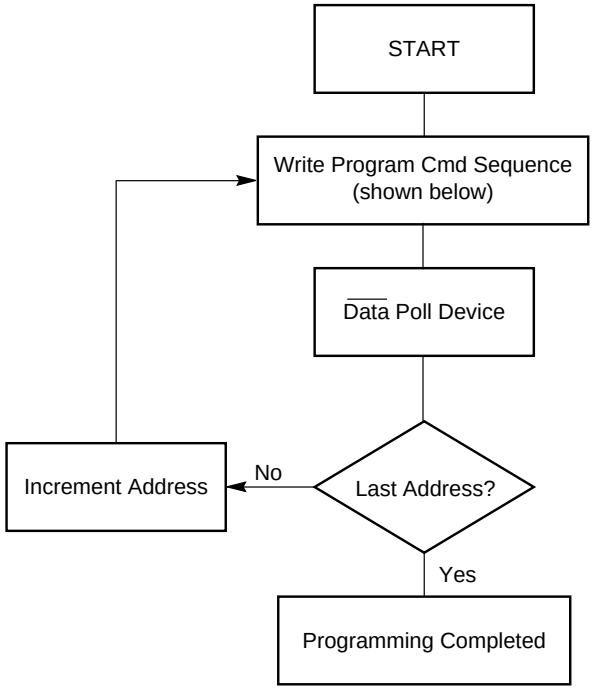
Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{CE} = \overline{WE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

EMBEDDED ALGORITHMS

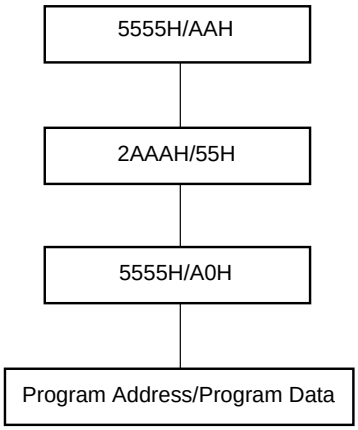
Embedded Program



21166A-6

Command Sequence

See the Command Definitions section for more information.

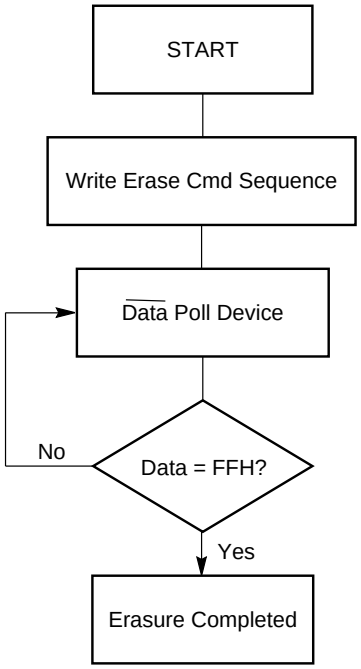


21166A-7

Figure 1. Embedded Program Algorithm

EMBEDDED ALGORITHMS (CONTINUED)

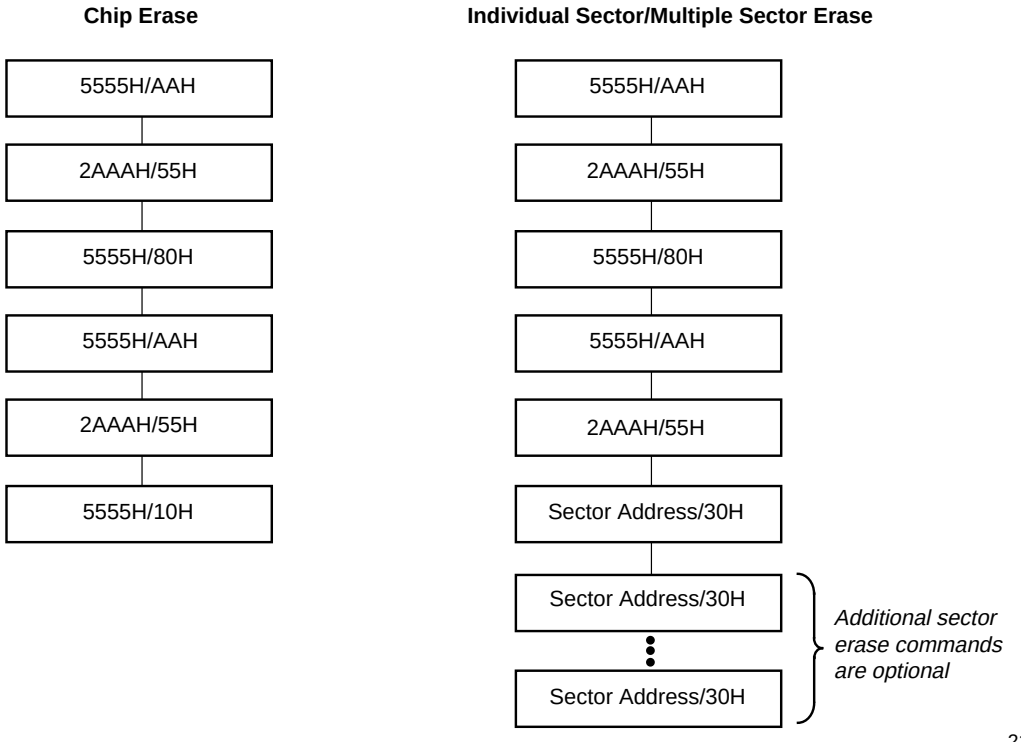
Embedded Erase



21166A-8

Command Sequence

See the Command Definitions section for more information.



21166A-9

Figure 2. Embedded Erase Algorithm

EMBEDDED ALGORITHMS (CONTINUED)

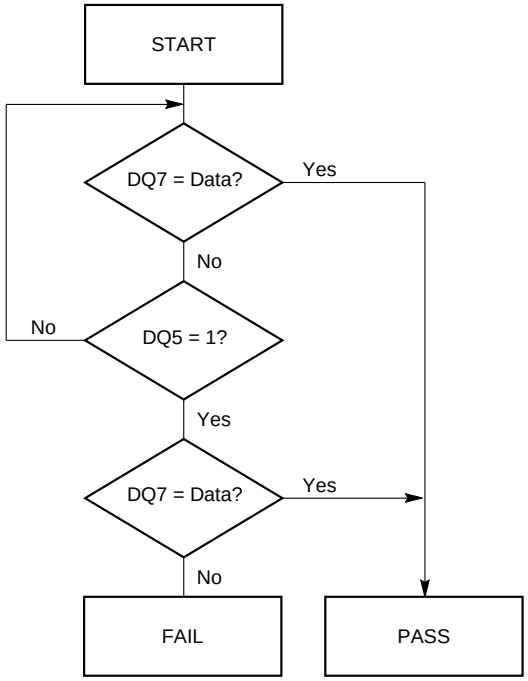


Figure 3. $\overline{\text{Data}}$ Polling Algorithm

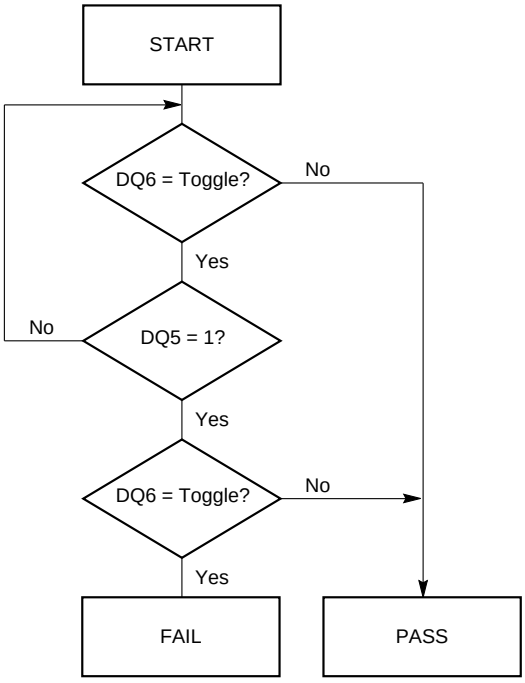


Figure 4. Toggle Bit Algorithm

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . -65°C to +125°C

Ambient Temperature
with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground
All pins except A9, $\overline{OE}$ (Note 1) . . . . . -2.0 V to +7.0 V

V_{CC} (Note 1). . . . . -2.0 V to +7.0 V

A9, $\overline{OE}$ (Note 2) . . . . . -2.0 V to +13.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 6 and Figure 7.*
2. *Minimum DC input voltage on pins A9 and $\overline{OE}$ is -0.5 V. During voltage transitions, A9 and $\overline{OE}$ may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns. See Figure 6 and Figure 7.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0˚C to +70˚C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40˚C to +85˚C

Extended (E) Devices

Ambient Temperature (T_A). . . . . -55˚C to +125˚C

V_{CC} Supply Voltages

V_{CC} for Am29F002NT/B-55 . . . . . +4.75 V to +5.25 V

V_{CC} for Am29F002NT/B-70,
-90, -120 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{LIT}	High Voltage Input Load Current (Note 3)	$V_{CC} = V_{CC\ max}$; A9, $\overline{OE}$ = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		20	30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	40	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC\ max}$; $\overline{CE}$, $\overline{OE}$, $\overline{RESET} = V_{IH}$		400		µA
					1	mA
I_{CC4}	V_{CC} Reset Current	$V_{CC} = V_{CC\ max}$; $\overline{RESET} = V_{IL}$		400		µA
					1	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC\ min}$			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA, $V_{CC} = V_{CC\ min}$	2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{LIT}	High Voltage Input Load Current	$V_{CC} = V_{CC\ max}$; A9, $\overline{OE}$ = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		20	30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	40	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	$V_{CC} = V_{CC\ max}$; $\overline{CE} = V_{CC} \pm 0.5$ V; $\overline{OE} = V_{IH}$		1	5	µA
I_{CC4}	V_{CC} Reset Current	$V_{CC} = V_{CC\ max}$		1	5	µA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect, and Temporary Sector Unprotect	V_{CC} = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC\ min}$			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5 mA, $V_{CC} = V_{CC\ min}$	0.85 V_{CC}			V
V_{OH2}		I_{OH} = -100 µA, $V_{CC} = V_{CC\ min}$	V_{CC} - 0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Not 100% tested.*
4. *I_{CC3} = 20 µA max at extended temperature (> +85°C).*

AC CHARACTERISTICS

Read-Only Operations Characteristics

Parameter Symbols		Description	Test Setup		Speed Options (Note 1)				Unit
JEDEC	Standard				-55	-70	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)		Min	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	55	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 2, 3)		Max	15	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 2, 3)		Max	15	20	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	ns

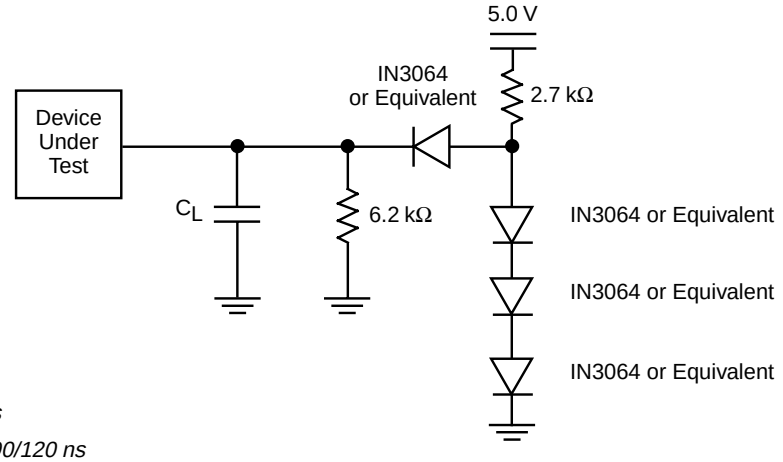
Notes:

1. *Test Conditions:*

   for -55: Output Load: 1 TTL gate and 30 pF
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level, Input and Output: 1.5 V

   for all others: Output Load: 1 TTL gate and 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level, Input and Output: 0.8 V and 2.0 V

2. *Output Driver Disable Time*
3. *Not 100% tested.*



Notes:

C_L *= 30 pF for 55 ns*

C_L *= 100 pF for 70/90/120 ns*

21166A-10

Figure 5. Test Conditions

AC CHARACTERISTICS

Write (Erase/Program) Operations

Parameter Symbols		Description			-55	-70	-90	-120	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time		Min	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	25	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold TIme	Read (Note 2)	Min	0	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling (Note 2)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30	35	45	50	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	300	300	300	300	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1	1	1	1	s
				Max	8	8	8	8	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Note 1)		Typ	7	7	7	7	s
				Max	56	56	56	56	s
	t_{VCS}	V_{CC} Setup Time (Note 2)		Min	50	50	50	50	µs

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

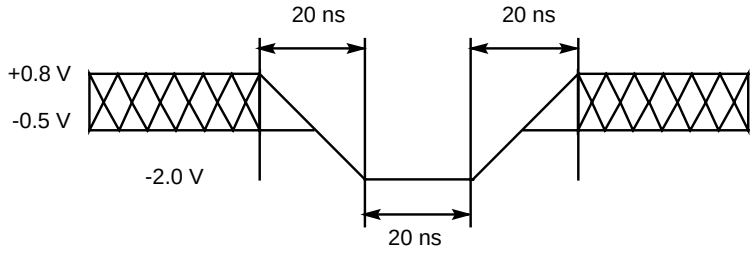


Figure 6. Maximum Negative Overshoot Waveform

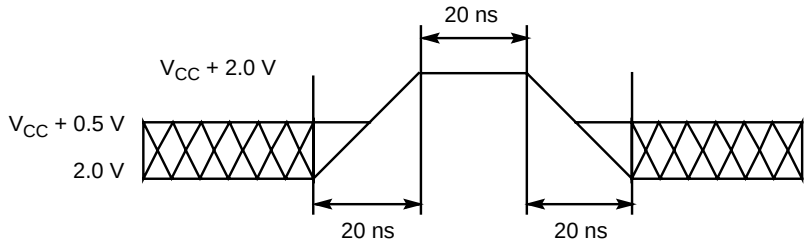
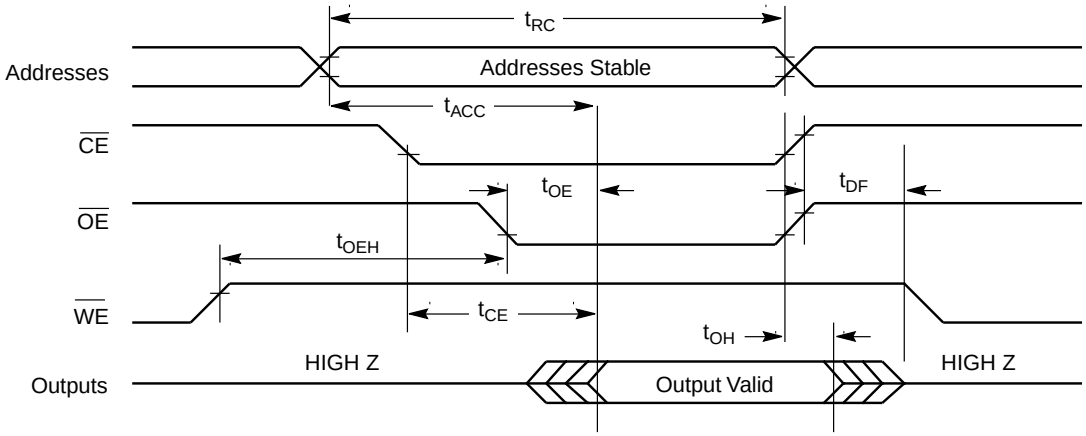
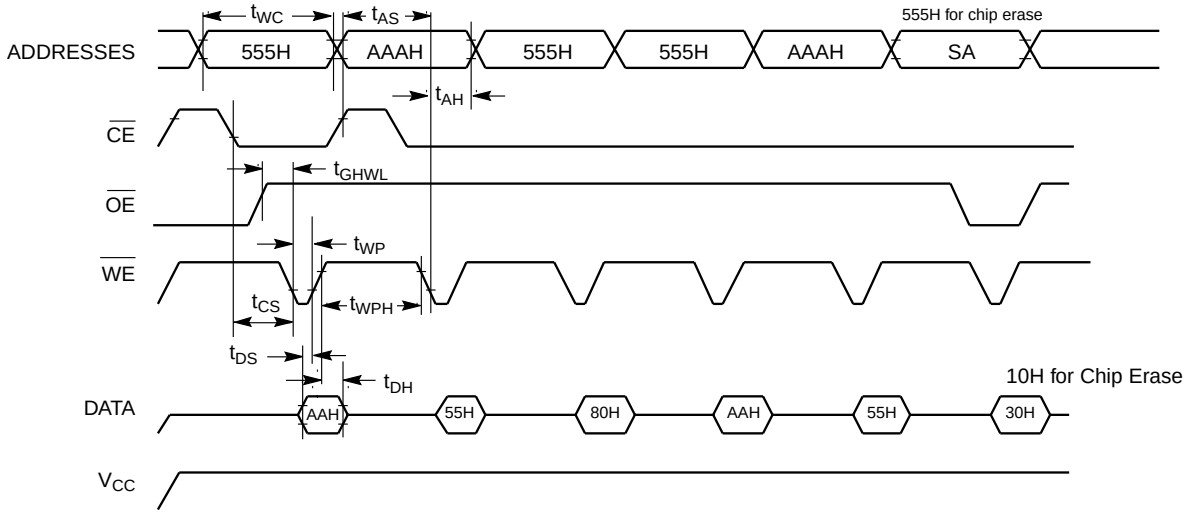


Figure 7. Maximum Positive Overshoot Waveform



21166A-11

Figure 8. AC Waveforms for Read Operations



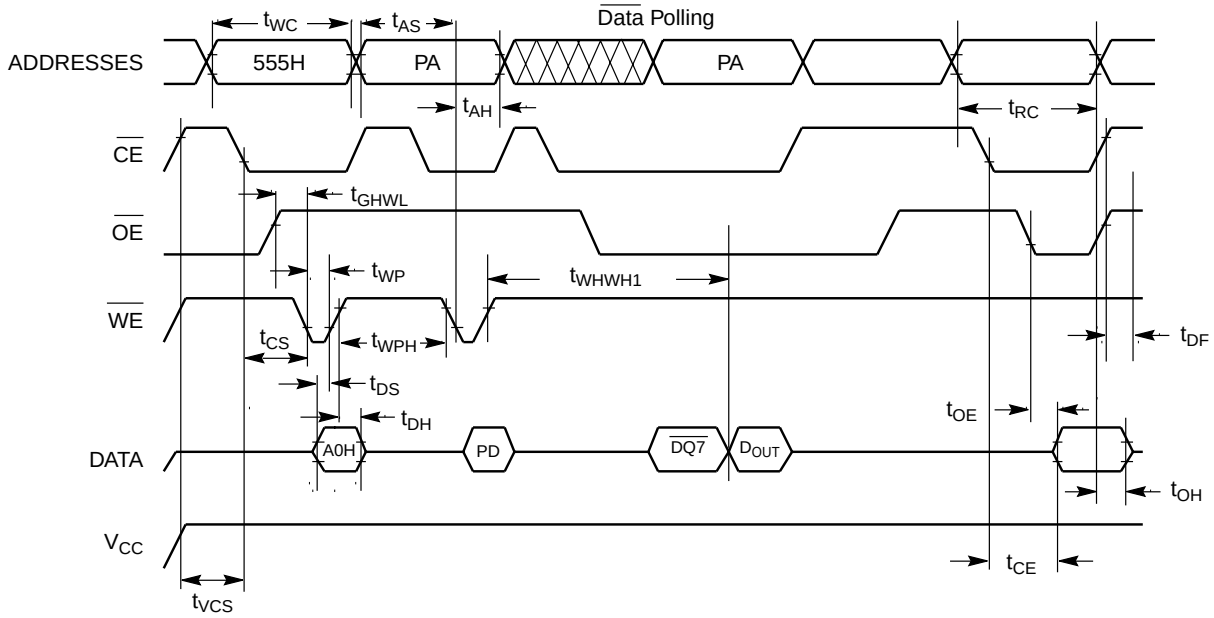
Notes:

1. SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

21166A-12

Figure 9. AC Waveforms for Chip/Sector Erase Operations

SWITCHING WAVEFORMS (CONTINUED)

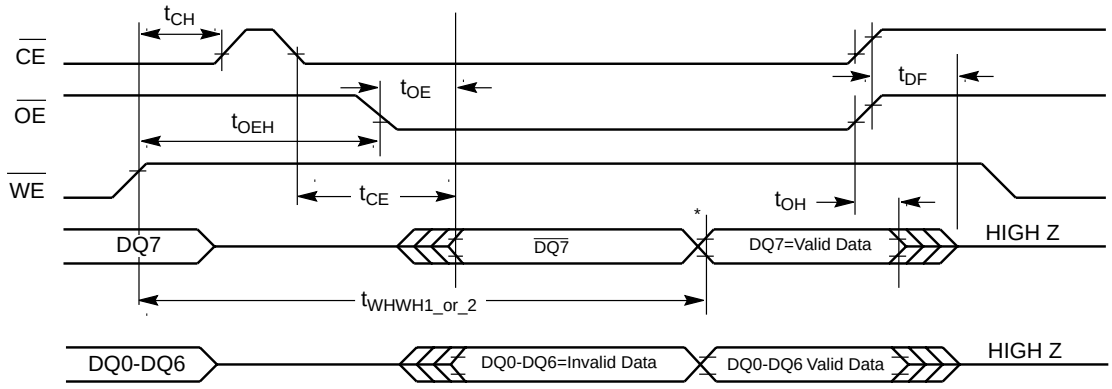


Notes:

1. *DQ7 is the output of the complement of the data written to the device.*
2. *D_{OUT} is the output of the data written to the device.*
3. *PA is the address of the memory location to be programmed.*
4. *PD is the data to be programmed at the byte address.*
5. *Illustration shows the last two cycles of a two-bus-cycle sequence.*

21166A-13

Figure 10. Program Operation Timings

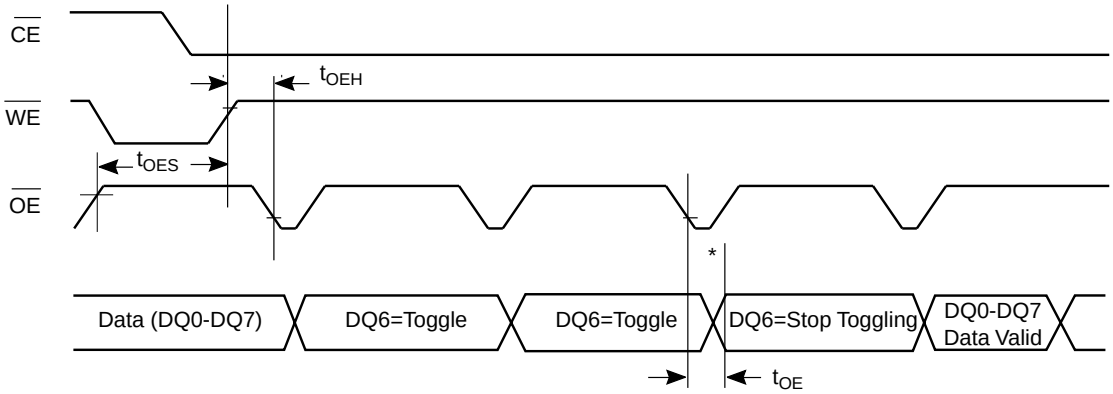


Note:

** DQ7 = Valid Data (The device has completed the embedded operation.)*

21166A-14

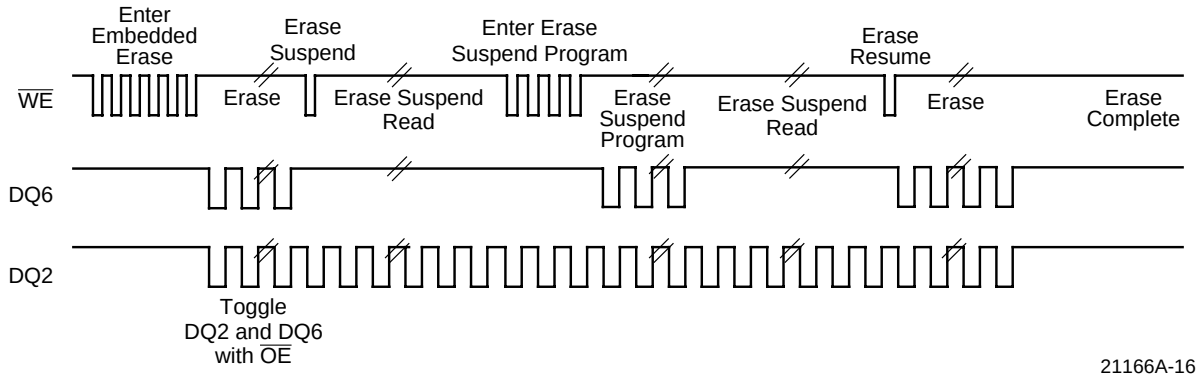
Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



Note:
** DQ6 stops toggling (The device has completed the embedded operation.)*

21166A-15

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



21166A-16

Note:
DQ2 is read from the erase-suspended sector.

Figure 13. DQ2 vs. DQ6

AC CHARACTERISTICS

Write(Erase/Program) Operations

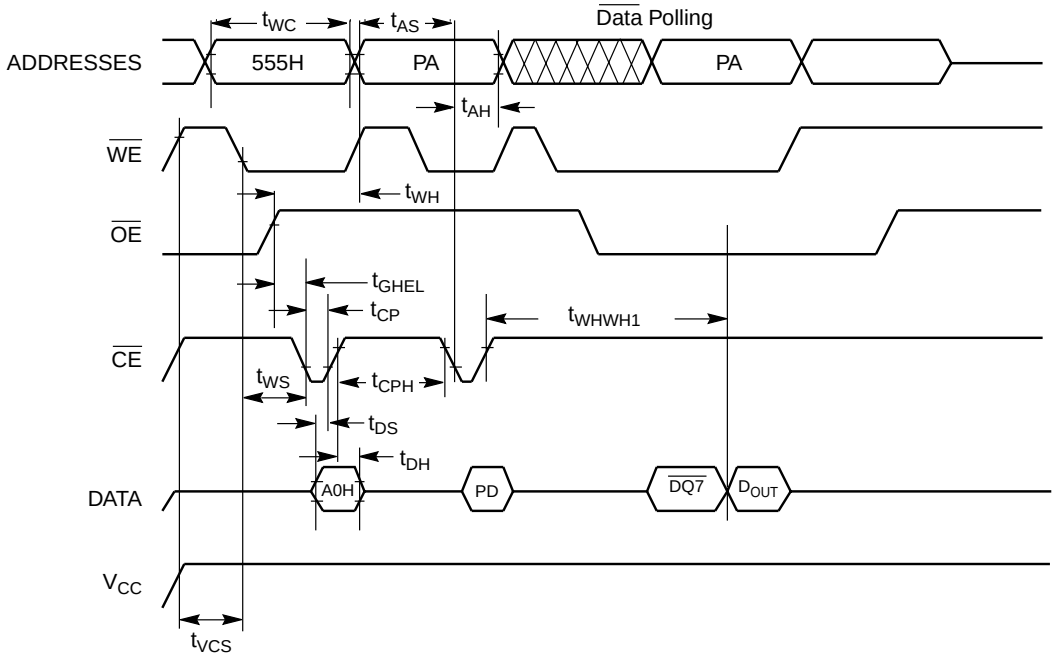
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			-55	-70	-90	-120	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time		Min	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	25	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold TIme	Read (Note 2)	Min	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recovery TIme Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup TIme		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold TIme		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	30	35	45	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	300	300	300	300	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1	1	1	1	s
				Max	8	8	8	8	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Note 1)		Typ	7	7	7	7	s
				Max	56	56	56	56	s
	t_{VCS}	V_{CC} Setup TIme (Note 2)		Min	50	50	50	50	µs

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

21166A-17

Figure 14. Alternate $\overline{CE}$ Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Comments
	Typ (Note 1)	Max (Note 3)	Unit	
Sector Erase Time	1	8	sec	Excludes 00H programming prior to erasure
Chip Erase Time (Note 2)	7	56	sec	
Byte Programming Time	7	300	µs	Excludes system level overhead (Notes 4, 5)
Chip Programming Time (Note 2)	1.8	5.4	sec	
Erase/Program Endurance	1,000,000		cycles	Minimum 100,000 cycles guaranteed

Notes:

1. *Except for erase/program endurance, the following conditions apply to erase and program times: 25°C, 5 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Although Embedded Algorithms allow for a longer chip program and erase time, the actual time will be considerably less since most bytes program or erase significantly faster than the worst case byte.*
3. *Under worst case condition of 90°C, V_{CC} = 4.5 V, 100,000 cycles.*
4. *System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the pre-programming step of the Embedded Erase Algorithm, all bytes are programmed to 00H before erasure.*
5. *The Embedded Algorithms allow for 1.8 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum programming times listed above.*

LATCHUP CHARACTERISTICS

	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9 and $\overline{OE}$)	-1.0 V	13.0 V
Input voltage with respect to V_{SS} on all I/O pins	-1.0 V	V_{CC} + 1.0 V
V_{CC} Current	-100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

32-PIN PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = l.0 MHz.*

32-PIN TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25˚C, f = 1.0 MHz.*

32-PIN PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	12	pF

Notes:

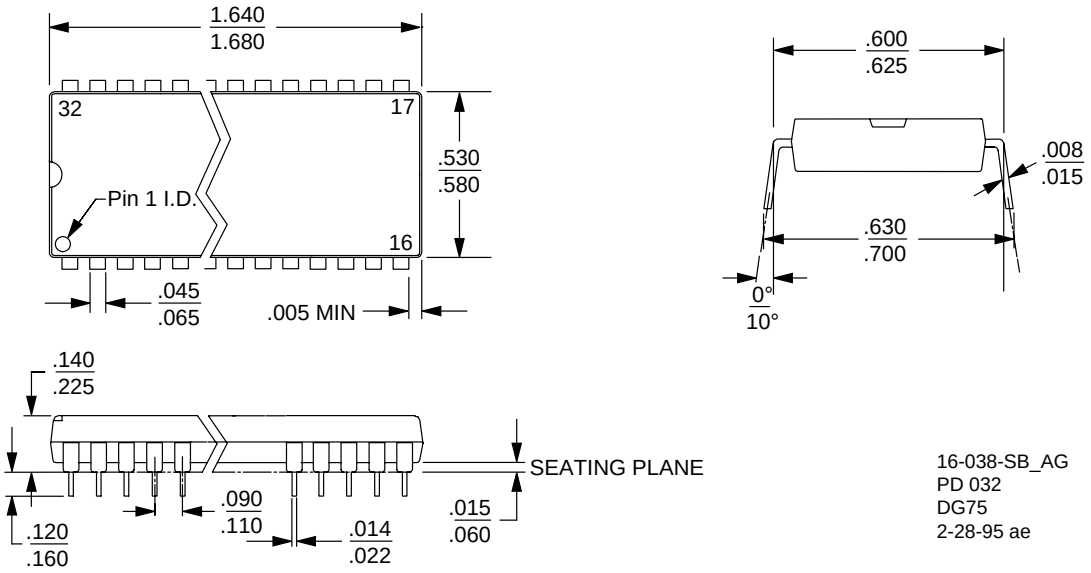
1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25˚C, f = l.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention TIme	150˚C	10	Years
	125˚C	20	Years

PHYSICAL DIMENSIONS

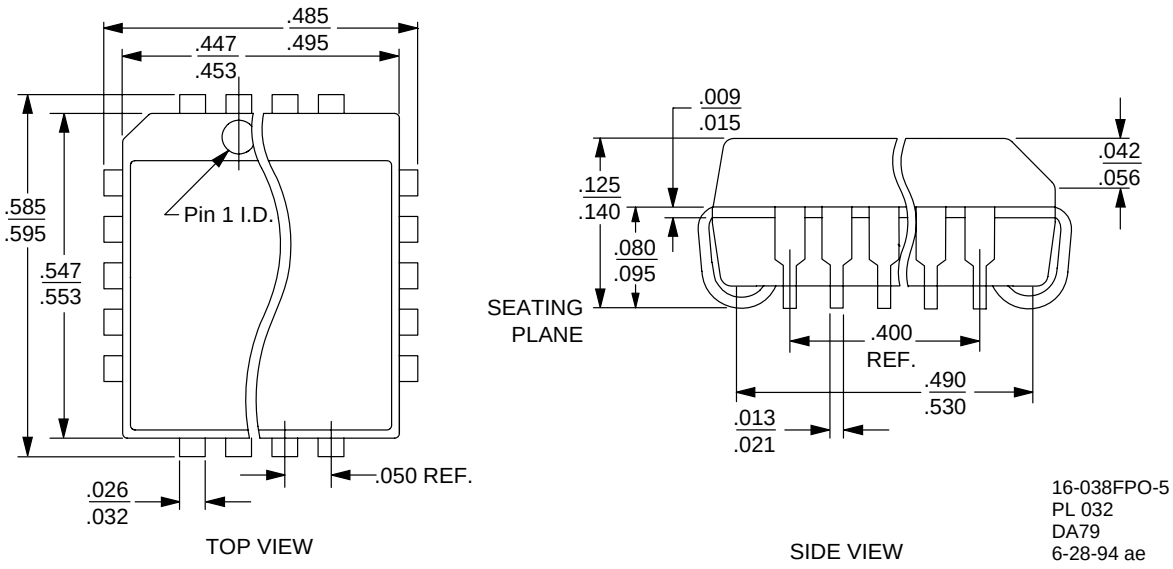
PD 032
32-Pin Plastic DIP (measured in inches)



16-038-SB_AG
PD 032
DG75
2-28-95 ae

PHYSICAL DIMENSIONS

PL 032
32-Pin Plastic Leaded Chip Carrier (measured in inches)



PHYSICAL DIMENSIONS (continued)

TS 032
32-Pin Standard Thin Small Outline Package (measured in millimeters)