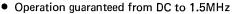
Am4055/5055 • Am4056/5056 • Am4057/5057

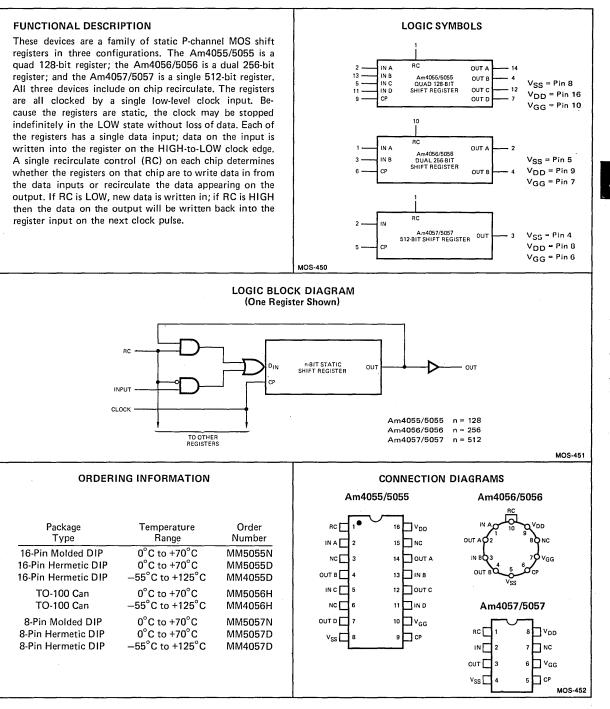
Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

Distinctive Characteristics

- Internal recirculate
- Single TTL compatible clock



 100% reliability assurance testing in compliance with MIL-STD-883



Am40/5055 • Am40/5056 • Am40/5057

MAXIMUM RATINGS (Above which the useful life may be impaired)

| Storage Temperature | -65°C to +160°C |
|----------------------------------|---|
| Temperature (Ambient) Under Bias | -55°C to +125°C |
| V _{DD} Supply Voltage | V _{SS} -10V to V _{SS} +0.3V |
| V _{GG} Supply Voltage | V _{SS} -20V to V _{SS} +0.3V |
| DC Input Voltage | V _{SS} –20V to V _{SS} +0.3V |

OPERATING RANGE

| Part Number Ambient Temperature | | V _{SS} | VDD | V _{GG} | |
|---------------------------------|-----------------|-----------------|-----|-----------------|--|
| Am4055 Am4056 Am4057 | –55°C to +125°C | 5.0V ±5% | ٥٧ | –12∨±5% | |
| Am5055 Am5056 Am5057 | 0°C to +70°C | 5.0V ±5% | ٥٧ | -12V ±5% | |

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

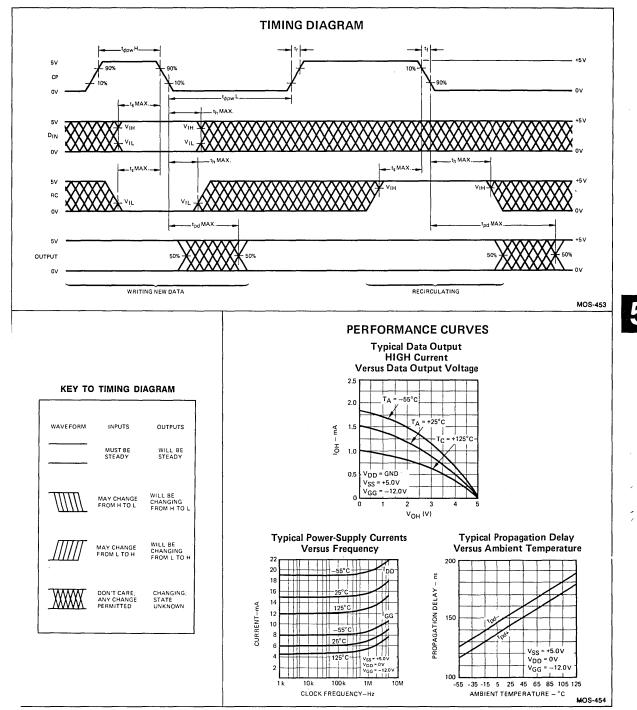
| Parameters | Description | Test | Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|-----------------|--------------------------------------|---|------------|----------------------|-----------------------|----------------------|----------------------|-------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.5mA | | | 2.4 | | | Volts |
| VOL | Output LOW Voltage | I _{OL} = 1.6mA | | | | | 0.4 | Volts |
| Nex | Input HIGH Level | Guaranteed input logical HIGH voltage 4055/6/7 for all inputs 5055/6/7 | | V _{SS} -1.0 | | V _{SS} +0.3 | Volts | |
| VIH | | | | V _{SS} -1.5 | | V _{SS} +0.3 | VOITS | |
| VIL | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | V _{SS} -18.5 | | V _{SS} -4.2 | Volts |
| Ι _{ΙL} | Input Leakage Current | $V_{IN} = -10.0V$, all other pins GND, $T_A = 25^{\circ}C$ | | | | 0.01 | 0.5 | μA |
| | Mar Bring Suraha Ourra | T _A = 25°C, | f ≤ 2.2MHz | | | 15.0 | 20.0 | |
| DD | V _{DD} Power Supply Current | t _{opw} H = 160 ns | f ≤ 10KHz | | | 13.0 | 18.0 | |
| IGG | N. D | Data = 1010 | f ≤ 1.6MHz | | | 10.5 | 15.5 | mA |
| | VGG Power Supply Current | output open | f ≤ 2.2MHz | | | 13.0 | 19.0 | |
| | f ≤ 10KHz | | | 6.5 | 9.0 | | | |

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = -12V, 25°C ambient.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | | Am4055/6/7 | | | Am5055/6/7 | | | |
|---------------------------------|---|--|------------|------|------|------------|------|------|-------|
| | | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| f | Clock Frequency | | 0 | | 1.0 | 0 | _ | 1.5 | MHz |
| t _{¢pw} H | Clock HIGH Time | | 0.4 | | 1.0 | 0.23 | | 100 | μs |
| t _{opw} L | Clock LOW Time | | 0.4 | | 00 | 0.3 | | | μs |
| t _r , t _f | Clock Rise and Fall Times | | | | 200 | | | 200 | ns |
| ts | Set-up Time, D or RC Inputs (see definitions) | t _r = t _f ≤ 10ns | 260 | | | 110 | | | ns |
| th | Hold Time, D or RC Inputs (see definitions) | t _r = t _f ≤ 10ns | 120 | | | 40 | | | ns |
| tpd | Delay, Clock to Output LOW or HIGH | $R_L = 4k, C_L = 10pF$ | | 350 | 700 | | 250 | 345 | ns |
| Cin | Capacitance, Data and RC Inputs (Note 2) | f = 1MHz, VIN = VSS | | 4 | 7 | | 4 | 7 | pF |
| c_{ϕ} | Capacitance, Clock Input (Note 2) | f = 1MHz, VIN = VSS | | | 14 | | | 14 | pF |

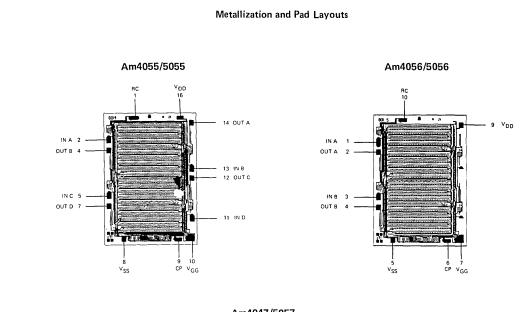
Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design. 3. At any temperature, t_{pd} min. is always much greater than $t_h(D)$ max.



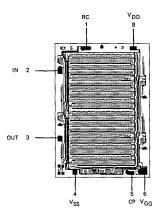
EFINITION OF TERMS

ATIC SHIFT REGISTER A shift register that is capable of intaining stored data without being continuously clocked. Is static shift registers are constructed with dynamic master d static slave flip-flops. The data is stored dynamically while clock is HIGH and is transferred to the static slaves while the ck is LOW. The clock may be stopped indefinitely in the LOW te, but there are limitations on the time it may reside in HIGH state. SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

1



Am4047/5057



DIE SIZES 0.101" X 0.140"