Am8085A/Am8085A-2/Am9085ADM

Single Chip 8-Bit N-Channel Microprocessor

DISTINCTIVE CHARACTERISTICS

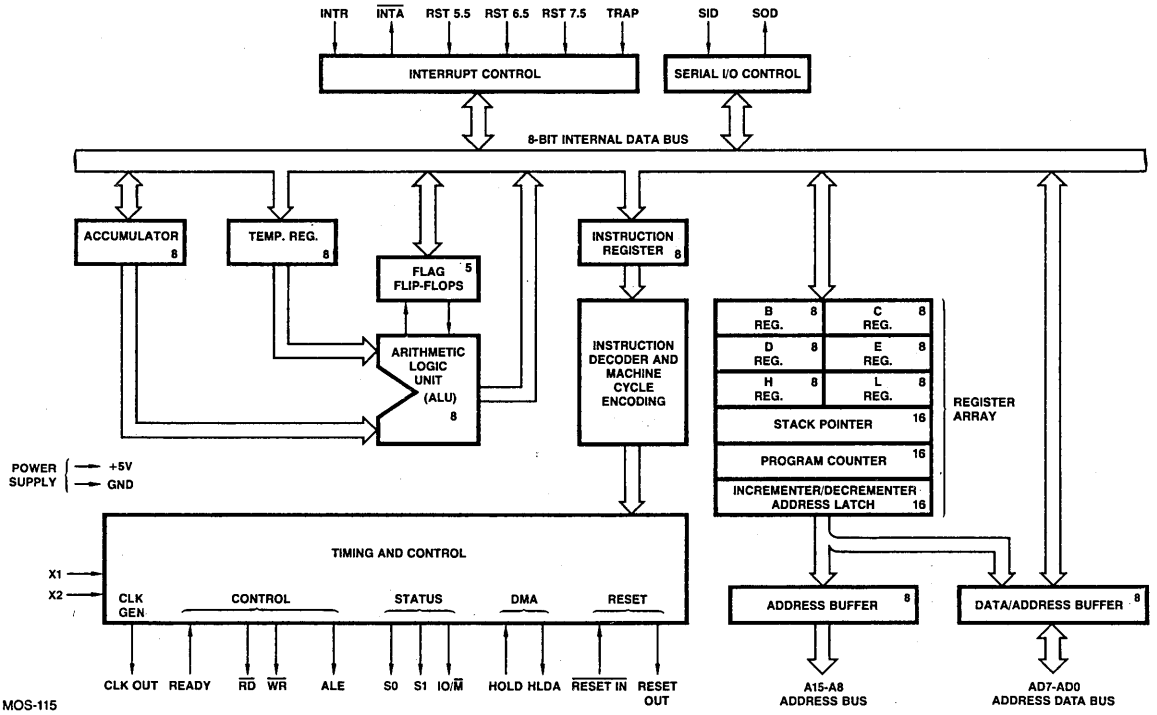
- Complete 8-bit parallel CPU
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- On-chip clock generator (with external crystal, LC or R/C network)
- Serial in/serial out port
- Decimal, binary and double precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 1.3μs instruction cycle (Am8085A)
- 0.8μs instruction cycle (Am8085A-2)
- 100% software compatible with Am9080A
- Single +5V power supply
- 100% MIL-STD-883, Level C processing

GENERAL DESCRIPTION

The Am8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the Am9080A microprocessor. Specifically, the Am8085A incorporates all of the features that the Am8224 (clock generator) and Am8228 (system controller) provided for the Am9080A. The Am8085A-2 is a faster version of the Am8085A.

The Am8085A uses a multiplexed Data Bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of Am8155/Am8355 memory products allows a direct interface with Am8085A. The Am8085A components, including various timing compatible support chips, allow system speed optimization.

BLOCK DIAGRAM

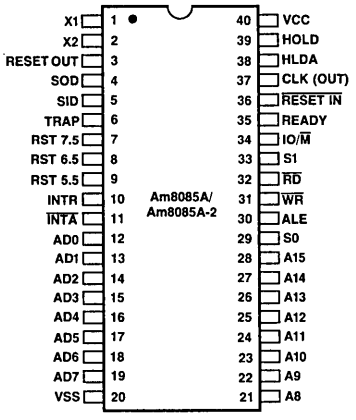


ORDERING INFORMATION

Package Type	Temperature Range	Maximum Clock Frequency	
		3MHz	5MHz
Molded DIP	0°C ≤ T_A ≤ 70°C	AM8085APC/P8085A AM8085ADC/D8085A AM8085ACC/C8085A	AM8085A-2PC/P8085A-2 AM8085A-2DC/D8085A-2 AM8085A-2CC/C8085A-2
Hermetic DIP*			
Hermetic DIP	−55°C ≤ T_A ≤ +125°C	AM9085ADM	

*Hermetic = Ceramic = DC = CC = D-40-1.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Figure 1. MOS-116

Am8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

A8-A15 (Output 3-State)

Address Bus – the most significant eight bits of the memory address or the eight bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD0-AD7 (Input/Output 3-State)

Multiplexed Address/Data Bus – lower eight bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine cycle. It then becomes the data bus during the second and third clock cycles.

Three-stated during Hold and Halt modes.

ALE (Output)

Address Latch Enable – it occurs during the first clock cycle of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge ALE can also be used to strobe the status information. ALE in never 3-stated.

S0, S1 (Output)

Data Bus Status. Encoded status of the bus cycle.

S1	S0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S1 can be used as an advanced R/$\overline{W}$ status.

$\overline{RD}$ (Output 3-State)

READ – A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Three-stated during Hold and Halt and during RESET.

$\overline{WR}$ (Output 3-State)

WRITE – A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Three-stated during Hold and Halt modes.

READY (Input)

If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.

HOLD (Input)

HOLD – indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are three-stated.

HLDA (Output)

HOLD ACKNOWLEDGE – indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes LOW.

INTR (Input)

INTERRUPT REQUEST – is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE – is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the Am9519 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5
RST 7.5
} (Inputs)

RESTART INTERRUPTS – these three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 ——► Highest Priority
RST 6.5
RST 5.5 ——► Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR. However they may be individually masked out using the SIM instructions.

TRAP (Input)

Trap interrupt is a non-maskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

$\overline{\text{RESET IN}}$ (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as RESET is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X1, X2 (Input)

Crystal, LC or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

IO/$\overline{\text{M}}$ (Output)

IO/$\overline{\text{M}}$ indicates whether the Read/Write is to memory or I/O. 3-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

VCC

+5 volt supply.

VSS

Ground reference.

FUNCTIONAL DESCRIPTION

The Am8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3MHz (5MHz: Am8085A-2) thus improving on the present Am9080's performance with higher system speed. Also it is designed to fit into a minimum system of three ICs: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The Am8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower eight bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready and all Interrupts are synchronized. The Am8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the Am8085A has three maskable, restart interrupts and one non-maskable trap interrupt.

Am8085A vs. Am8080A

The Am8085A includes the following features on-chip in addition to all of the Am9080A functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. RESET OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and non-maskable Interrupt
j. Serial Input/Output lines

The internal clock generator requires an external crystal or R/C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, non-overlapping clock is generated from this oscillator internally and one phase of the clock (ϕ2) is available as an external clock. The Am8085A directly provides the external RDY synchronization previously provided by the Am8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the Am8228 in Am9080A systems is also included in Am8085A.

STATUS INFORMATION

Status information is directly available from the Am8085A. ALE serves as a status strobe. The status is partially encoded and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S0, S1 carries the following status information:

MACHINE CYCLE STATUS

IO/$\overline{\text{M}}$	S1	S0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
•	0	0	Halt
•	X	X	Hold
•	X	X	Reset

• = 3-state (high impedance)
X = unspecified

S1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the Am8085A the eight LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

INTERRUPT AND SERIAL I/O

The Am8085A/Am8085A-2 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP. INTR is identical in function to the Am8080A INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

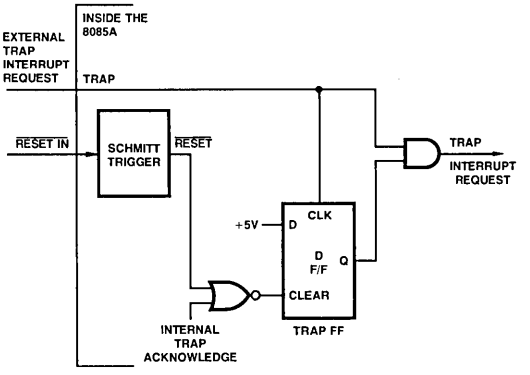
Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the Am8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive. For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the Am8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following diagram illustrates the TRAP interrupt request circuitry within the Am8085A.



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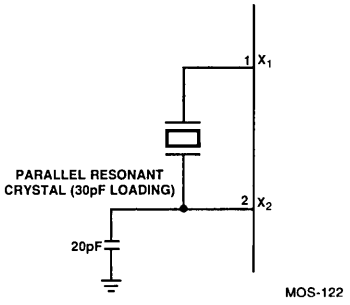
Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status.

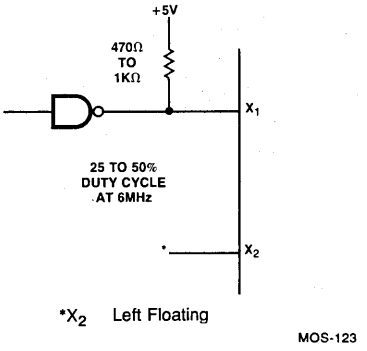
The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X1 an X2 INPUTS

The user may drive the X1 and X2 inputs of the Am8085A or Am8085A-2 with a crystal, an external clock source or an R/C network as shown below. The driving frequency must be twice the desired internal operating frequency (the Am8085A would require a 6MHz crystal for 3MHz internal operation).

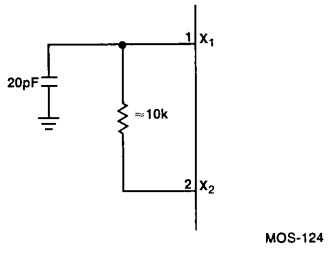


1-6 MHz Input Frequency

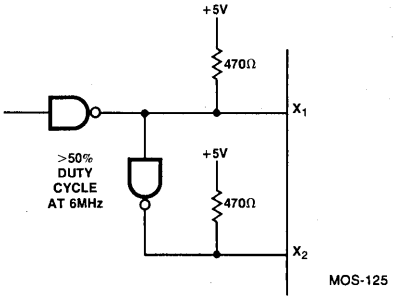


1-6 MHz Input Frequency

The 20pF capacitor is required to guarantee oscillation at the proper frequency during system startup.



≈3 MHz Input Frequency



≈6 MHz Input Frequency

RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application which can tolerate a wide frequency variation.

Note: Duty cycle refers to the percentage of the clock input cycle when X_1 is high.

Figure 2. Driving the Clock Inputs (X1 and X2) of Am8085A.

GENERATING Am8085A WAIT STATE

The following circuit may be used to insert one WAIT state in each Am8085A machine cycle.

The D flip-flops should be chosen such that

- CLK is rising edge triggered
- CLEAR is low-level active.

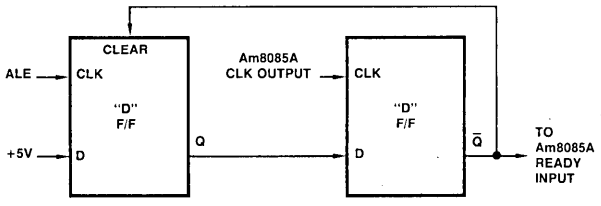


Figure 3. Generation of a Wait State for Am8085A CPU.

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BASIC SYSTEM TIMING

The Am8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the Am9080A, the READY line is used to extend the read and write pulse lengths so that the Am8085A can be used with slow memory. Hold causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

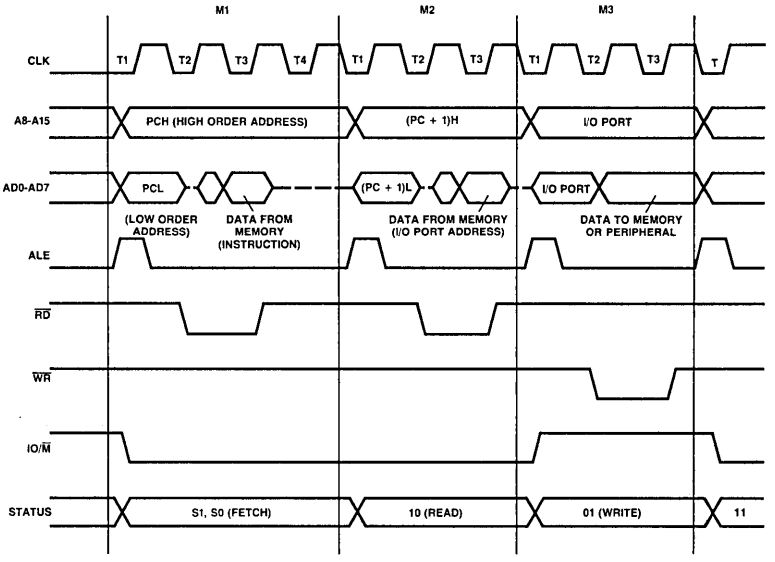


Figure 4. Am8085A Basic System Timing. MOS-118

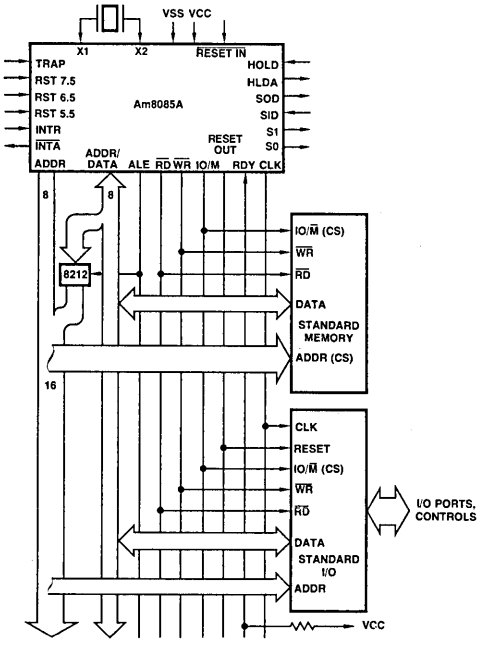


Figure 5. System Using Standard Memories. MOS-121

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	VCC	VSS
Am8085A/Am8085A-2	0 to 70°C	+5.0V ±5%	0V
Am9085ADM	−55 to +125°C	+5.0V ±10%	0V

DC CHARACTERISTICS

			Am8085A/Am8085A-2		Am9085ADM		
Parameter	**Description**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
VIL	Input Low Voltage		−0.5	+0.8	−0.5	+0.8	Volts
VIH	Input High Voltage		2.0	VCC+0.5	2.2	VCC+0.5	Volts
VOL	Output Low Voltage	IOL = 2.0mA		0.45		0.45*	Volts
VOH	Output High Voltage	IOH = −400μA	2.4		2.4		Volts
ICC	Power Supply Current			170		200	mA
IIL†	Input Leakage	VIN = VCC		±10		±10	μA
ILO	Output Leakage	0.45V ≤ VOUT ≤ VCC		±10		±10	μA
VILR	Input Low Level, RESET		−0.5	+0.8	−0.5	+0.8	Volts
VIHR	Input High Level, RESET		2.4	VCC+0.5	2.4	VCC+0.5	Volts
VHY	Hysteresis, RESET		0.25		0.25		Volts

*IOL = 1.6mA

†Except Pin 1 and Pin 2.

AC CHARACTERISTICS

Parameters	Description		Am8085A Min	Am8085A Max	Am8085A-2 Min	Am8085A-2 Max	Am9085ADM Min	Am9085ADM Max	Units
tCYC	CLK Cycle Period		320	2000	200	2000	320	2000	ns
tr, tf	CLK Rise and Fall Time			30		30		30	ns
tAL	A8-A15 Valid before Trailing Edge of ALE (Note 1)		115		50		115		ns
tACL	A0-A7 Valid to Leading Edge of Control		240		115		240		ns
tXKR	X1 Rising to CLK Rising		30	120	30	100	30	120	ns
tXKF	X1 Rising to CLK Falling		30	150	30	110	30	150	ns
t1	CLK Low Time	Standard 150pF Loading	80		40		80		ns
		Lightly Loaded (Note 8)	100				100		
t2	CLK High Time	Standard 150pF Loading	120		70		120		ns
		Lightly Loaded (Note 8)	150				150		
tALL	A0-A7 Valid to Leading Edge of Control		90		50		90		ns
tLRY	ALE to READY Stable			110		30		110	ns
tLA	Address Hold Time after ALE		100		50		100		ns
tLL	ALE Width		140		80		140		ns
tLCK	ALE Low During CLK High		100		50		100		ns
tLC	Trailing Edge of ALE to Leading Edge of Control		130		60		130		ns
tAFR	Address Float after Leading Edge of $\overline{READ}$ ($\overline{INTA}$)			0		0		0	ns
tAD	Valid Address to Valid Data In			575		350		575	ns
tRD	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data			300		150		300	ns
tRDH	Data Hold Time after $\overline{READ}$ ($\overline{INTA}$) (Note 7)		0		0		0		ns
tRAE	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address		150		90		150		ns
tCA	Address (A8-A15) Valid after Control		120		60		120		ns
tDW	Data Valid to Trailing Edge of $\overline{WRITE}$		420		230		420		ns
tWD	Data Valid after Trailing Edge of $\overline{WRITE}$		100		60		100		ns
tCC	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)		400		230		400		ns
tCL	Trailing Edge of Control to Leading Edge of ALE		50		25		50		ns
tARY	READY Valid from Address Valid			220		100		220	ns
tRYS	READY Setup Time to Leading Edge of CLK		110		100		110		ns
tRYH	READY Hold Time		0		0		0		ns
tHACK	HLDA Valid to Trailing Edge of CLK		110		40		110		ns
tHABF	Bus Float after HLDA			210		150		210	ns
tHABE	HLDA to Bus Enable			210		150		210	ns
tLDR	ALE to Valid Data In			460		270		460	ns
tRV	Control Trailing Edge to Leading Edge of Next Control		400		220		400		ns
tAC	A8-A15 Valid to Leading Edge of Control (Note 1)		270		115		270		ns
tHDS	HOLD Setup Time to Trailing Edge of CLK		170		120		170		ns
tHDH	HOLD Hold Time		0		0		0		ns
tINS	INTR Setup Time to Falling Edge of CLK, also RST and TRAP		160		150		160		ns
tINH	INTR Hold Time		0		0		0		ns

Notes:
1. A8-A15 Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A8-A15 are undefined during T4-T6 of OF cycle whereas IO/$\overline{M}$, S0 and S1 are stable.
2. Test Conditions: tCYC = 320ns (Am8085A)/200ns (Am8085A-2); CL = 150pF.
3. For all output timing where CL = 150pF use the following correction factors.
   25pF ≤ CL < 150pF: −.10ns/pF
   150pF < CL ≤ 300pF: +.30ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage VL = 0.8V, VH = 2.0V and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of tCYC use the table on Page 7-21.
7. Data Hold Time is guaranteed under all loading conditions.
8. Loading equivalent to 50pF +1 TTL input.

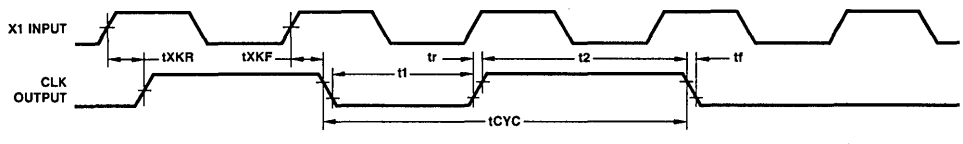
BUS TIMING SPECIFICATION AS A TCYC DEPENDENT

Parameters	Description	Am8085A/Am9085ADM Min	Am8085A/Am9085ADM Max	Am8085A-2 Min	Am8085A-2 Max	Units
tAL	Address Valid before Trailing Edge of ALE	(1/2)T−45		(1/2)T−50		ns
tLA	Address Hold Time after ALE	(1/2)T−60		(1/2)T−50		ns
tLL	ALE Width	(1/2)T−20		(1/2)T−20		ns
tLCK	ALE Low During CLK High	(1/2)T−60		(1/2)T−50		ns
tLC	Trailing Edge of ALE to Leading Edge of Control	(1/2)T−30		(1/2)T−40		ns
tAD	Valid Address to Valid Data In		(5/2+N)T−225		(5/2+N)T−150	ns
tRD	READ (or INTA) to Valid Data		(3/2+N)T−180		(3/2+N)T−150	ns
tRAE	Trailing Edge of READ to Re-Enabling of Address	(1/2)T−10		(1/2)T−10		ns
tCA	Address (A8-A15) Valid after Control	(1/2)T−40		(1/2)T−40		ns
tDW	Data Valid to Trailing Edge of WRITE	(3/2+N)T−60		(3/2+N)T−70		ns
tWD	Data Valid after Trailing Edge of WRITE	(1/2)T−60		(1/2)T−40		ns
tWDL	Leading Edge of WRITE to Data Valid		40		40	ns
tCC	Width of Control LOW (RD, WR, INTA)	(3/2+N)T−80		(3/2+N)T−70		ns
tCL	Trailing Edge of Control to Leading Edge of ALE	(1/2)T−110		(1/2)T−75		ns
tARY	READY Valid from Address Valid		(3/2)T−260		(3/2)T−200	ns
tHACK	HLDA Valid to Trailing Edge of CLK	(1/2)T−50		(1/2)T−60		ns
tHABF	Bus Float after HLDA		(1/2)T+50		(1/2)T+50	ns
tHABE	HLDA to Bus Enable		(1/2)T+50		(1/2)T+50	ns
tAC	Address Valid to Leading Edge of Control	(2/2)T−50		(2/2)T−85		ns
t1	CLK Low Time	(1/2)T−80		(1/2)T−60		ns
t2	CLK High Time	(1/2)T−40		(1/2)T−30		ns
tRV	Control Trailing Edge to Leading Edge of Next Control	(3/2)T−80		(3/2)T−80		ns
tLDR			(4/2)T−180		(4/2)T−130	ns
tLDW	Trailing Edge of ALE to Valid Data During WRITE		200		200	ns

Note: N is equal to the total WAIT states.
T = tCYC.

7

CLOCK TIMING WAVEFORM



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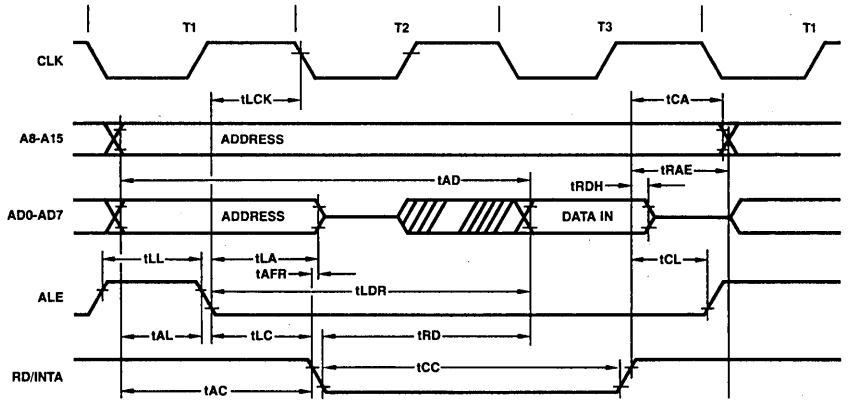
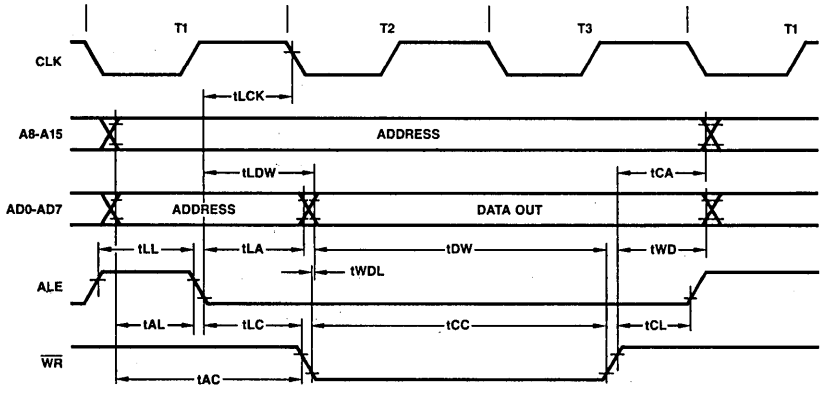
READ OPERATION



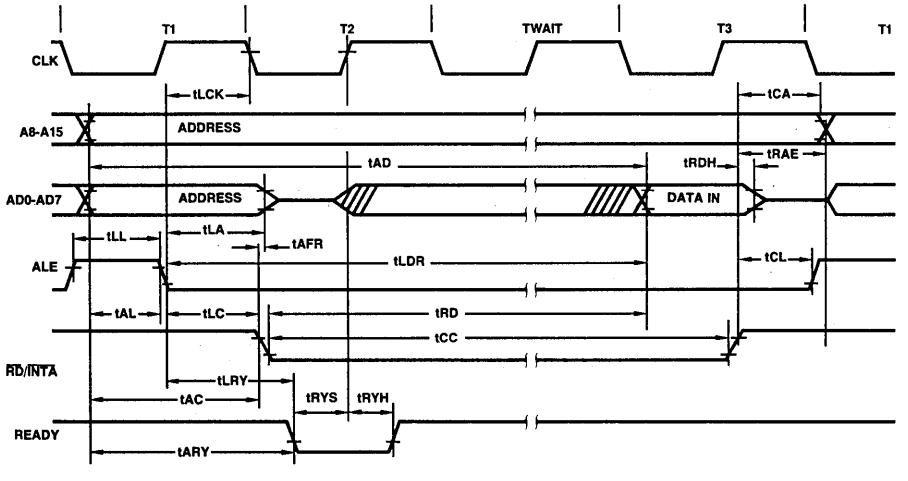
MOS-270

WRITE OPERATION



MOS-271

TYPICAL READ OPERATION WITH WAIT CYCLE



Same READY timing applies to WRITE operation.

Figure 6. Am8085A/Am8085A-2 Bus Timing

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HOLD OPERATION

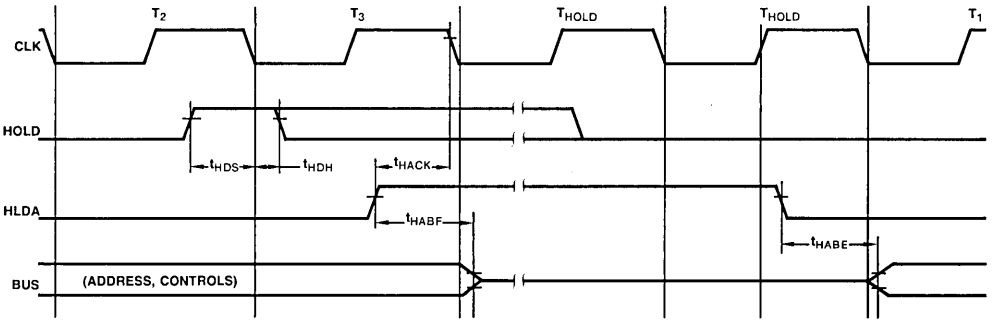

Figure 7. Am8085A Hold Timing.

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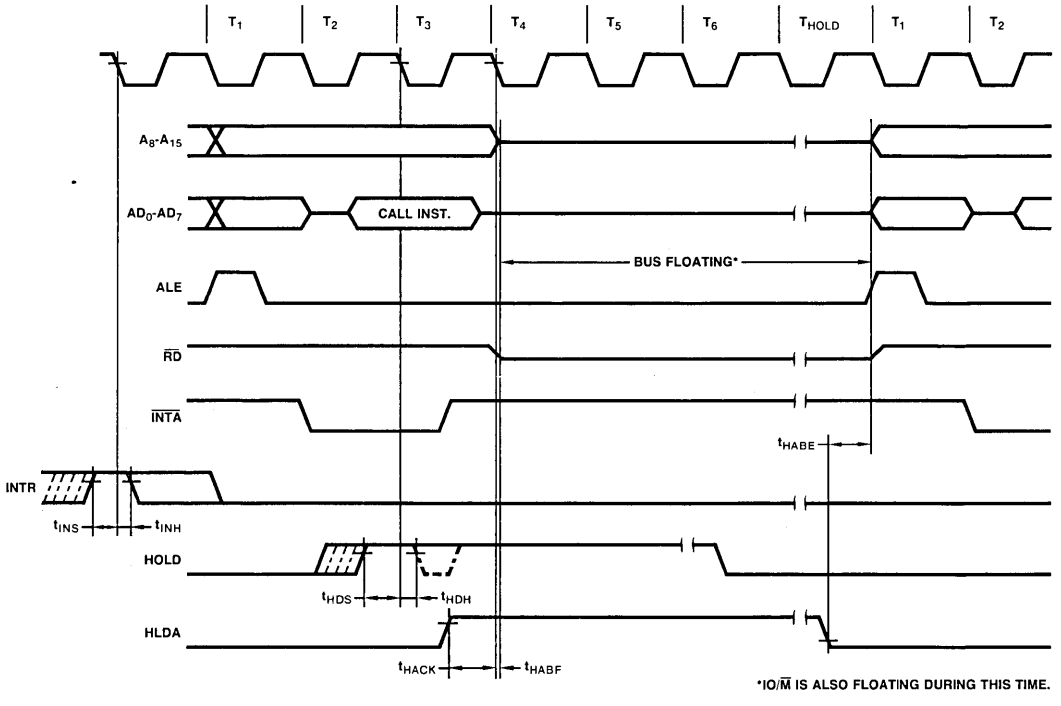

MOS-131

Figure 8. Am8085A Interrupt and Hold Timing.

INSTRUCTION SET SUMMARY

Mnemonic*	Description	Instruction Code (Note 1) D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles (Note 2)
MOVE, LOAD AND STORE										
MOVr1r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV Mr	Move register to memory	0	1	1	1	0	S	S	S	7
MOV rM	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10

INSTRUCTION SET SUMMARY (Cont.)

Mnemonic*	Description	Instruction Code (Note 1) D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles (Note 2)
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupts	1	1	1	1	0	0	1	1	4
NOP	No operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW Am8085A INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

Notes: 1. DOD or SSS: 8=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.