Am8224

Clock Generator and Driver for 8080A Compatible Microprocessors

Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Am8224-4 version available for use with 1µsec instruction cycle of Am9080A-4

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and ϕ_2 outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications. A high speed version, the Am8224-4, is available for use with the high speed Am9080A-4.



- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

PIN DEFINITION

XTAL 1			
XTAL 2	CONNECTIONS FOR CRYSTAL		
TANK	USED WITH OVERTONE XTAL		
OSC	OSCILLATOR OUTPUT		
$\phi_2(TTL)$	ϕ_2 CLK (TTL LEVEL)		
V _{CC}	+5.0V		
VDD	+12V		
GND	0V		
RESIN	RESET INPUT		
RESET	RESET OUTPUT		
RDYIN	READY INPUT		
READY	READY OUTPUT		
SYNC	SYNC INPUT		
STSTB	STATUS STB (ACTIVE LOW)		
¢1			
<i>ф</i> 2	Am9080A/8080A CLOCKS		



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	na n
V _{CC}	7.5V
V _{DD}	. 15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC, Am8224XC	Am8224-4XC (COM'L) T _A = (MIL) T _A =	0° C to +70° C V _{CC} = 5.0V ± 5% -55° C to +125° C V _{CC} = 5.0V ± 10%	V _{DD} = 12V V _{DD} = 12V	± 5% ± 10%	Tvp.			
Parameters Description		Test Conditions	Test Conditions			Max.	Units	
١ _F	Input Current Loading	V _F = 0.45 V	V _F = 0.45 V			-0.25	mA	
IR	Input Leakage Current	V _R = 5.25 V				10	μA	
	Input Forward Clamp Valtage					-1.0	Volta	
vс	mput Forward Clamp Voltage	$T_{C} = -5.0$ mA	MIL			-1.2	voits	
VIL	Input LOW Voltage	V _{CC} = 5.0 V	V _{CC} = 5.0 V				Volts	
		Posst is suit	COM'L	2.6	2.2			
VIH	Input HIGH Voltage	Reset input	MIL	2.8	2.2		Volts	
-		All other inputs	All other inputs					
$v_{IH} - v_{IL}$	RESIN Input Hysteresis	V _{CC} = 5.0 V	0.25	0.5		Volts		
v _{ol}		(ϕ_1, ϕ_2) , Ready, Reset, STSTB IOL = 2.5 mA			0.45			
	Output LOW Voltage	All other inputs I _{OL} = 15mA				0.45	Volts	
			COM'L	9.4	11			
	Output HIGH Voltage	$\phi_1, \phi_2; \text{IOH} = -100 \mu \text{A}$	MIL	V _{DD} 1.6V	/V _{DD} -1.0V		1	
v _{он}		READY RESET I	COM'L	3.6	4.0		Volts	
		TEADT, RESET, TOH = -100#A	MIL	3.35	4.0		1	
		All other outputs; IOH = -1.0mA	All other outputs; IOH = -1.0mA					
I _{SC}	Output Short Circuit Current (All Low Voltage Outputs On	V _O = 0V V _{CC} = 5.0V	V _O = 0V V _{CC} = 5.0V			60	mA	
Icc	Power Supply Current	V _{CC} = MAX. (Note 3)			70	115	mA	
חח	Power Supply Current	VDD = MAX.			5.0	12	mA	

Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.

2. Typical limits are at V_{CC} = 5.0 V, V_{DD} = 12 V, 25°C ambient and maximum loading.

3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.



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Am8224 AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

			Ai	m8224)	KM	Am8224XC			Am8224-4XC (Note 2)			
Parameters	Description	Test Conditions	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
tø1	ϕ_1 Pulse Width		$\frac{2t_{CY}}{9}$ -23ns			$\frac{2t_{CY}}{9}$ -20ns			45			
tφ2	ϕ_{2} Pulse Width		5tCY 9-35ns			$\frac{5t_{CY}}{9}$ -35ns			110			
tD1	φ ₁ to φ ₂ Delay	Ci =20nE	0			0			0			
tD2	ϕ_2 to ϕ_1 Delay	to 50pF	$\frac{2t_{CY}}{9}$ - 17ns			$\frac{2t_{CY}}{9}$ -14ns			35			ns
tD3	φ ₁ to φ ₂ Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +22ns	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20ns	55		76	-
tr	ϕ_1 and ϕ_2 Rise Time				20			20			20	
tf	ϕ_1 and ϕ_2 Fall Time				20			20			20	
^t D¢2	ϕ_2 to ϕ_2 (TTL) Delay	φ ₂ (TTL), C _L = 30pF R ₁ = 300Ω R ₂ = 600Ω	-5.0		15	-5.0		15	-5.0	i	15	ns
tDSS	ϕ_2 to STSTB Delay		$\frac{6t_{CY}}{9}$ -33ns		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}$ -30ns		6tCY 9	137		167	
tPW	STSTB Pulse Width	<u>STSTB,</u> С _L = 15pF,	$\frac{t_{CY}}{9}$ -18ns			$\frac{t_{CY}}{9}$ -15ns			18			
[†] DRS	RDYIN Set-up Time to Status Strobe	R ₁ = 2.0kΩ R ₂ = 4.0kΩ	$50 \text{ns} - \frac{4 \text{t}_{CY}}{9}$			$50ns - \frac{4t_{CY}}{9}$			-61			115
^t DRH	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			4tCY 9			111			
^t DR	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset C _L = 10pF R ₁ = 2.0kΩ R ₂ = 4.0kΩ	4tCY 9-25ns			$\frac{4t_{CY}}{9}$ -25ns			86			ns
^t CLK	CLK Period			tCY 9			tCY 9			28		
f _{Max} .	Maximum Oscillating Frequency		27			28.12			36			MHz
C _{in}	Input Capacitance	V _{CC} = 5.0V V _{DD} = 12V V _{BIAS} = 2.5V f = 1.0MHz			8.0			8.0			8.0	pF

AC CHARACTERISTICS (For t_{CY} = 488.28ns)

 $T_A = 0^{\circ}C \text{ to } +70^{\circ}C \qquad V_{CC} = +5.0 \text{ V} \pm 5\% \quad V_{DD} = +12 \text{ V} \pm 5\%$

Parameters	Description	Test Conditions	Min.	Тур.	Max.	Units
tø1	ϕ_1 Pulse Width		89			ns
t _{φ2}	ϕ_2 Pulse Width	Test Conditions ϕ_1 and ϕ_2 Loaded C_L = 20 to 50pF Ready and Reset Loaded C_L = 20 to 50pF R_1 = 2.0 k Ω , R_2 = 4.0 k Ω	236			ns
tD1	Delay ϕ_1 to ϕ_2		0			ns
t _{D2}	Delay ϕ_2 to ϕ_1	ϕ_1 and ϕ_2 Loaded C ₁ = 20 to 50 nF	95			ns
t _{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ńs
tr	Output Rise Time				20	ns
tf	Output Fall Time				20	ns
tDSS	ϕ_2 to STSTB Delay		296		326	ns
tDφ2	ϕ_2 to ϕ_2 (TTL) Delay		-5.0		15	ns
tpw	Status Strobe Pulse Width		40			ns
tDRS	RDYIN Set-up Time to STSTB	Ready and Reset Loaded C _L = 20 to 50pF	-167			ns
t DRH	RDYIN Hold Time After STSTB		217			ns
^t DR	Ready or Reset to ϕ_2 Delay	$R_1 = 2.0 k\Omega$, $R_2 = 4.0 k\Omega$	192			ns
FREQ	Oscillator Frequency				18.432	MHz

Notes: 1. All measurements referenced to 1.5V unless specified otherwise.
2. Am8224-4 parameter limits are given for t_{CY} = 250ns or an oscillating frequency of 36MHz. Between 28.12MHz and 36MHz min. and max. limits should be ratioed between the calculated Am8224XC limits at 28.12MHz and the given 36MHz parameter limits.



Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to determine the crystal frequency is:

$$f(XTAL) = \frac{1}{tCY}$$
 times 9

When using crystals above 10MHz a small amount of frequency "trimming" is necessary to produce the desired frequency. The addition of a selected capacitance (20pF - 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has a much lower output at its rated frequency and has a tendency to oscillate at its fundamental. To avoid the unwanted oscillation and increase the desired frequency output it is necessary to provide a parallel tuned resonant circuit of low impedance. The external LC network is connected to the TANK input and is AC coupled. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi \sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; ϕ_1 and ϕ_2 , can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

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The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe (STSTB) is achieved.



Figure 1. Clock Generator Waveforms.

STSTB (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ_{1A}), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The STSTB signal connects directly to the Am8228 System Controller.

The power-on Reset also generates STSTB, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the RESIN input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ_{2D} (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flipflop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ_{2D} , a synchronized READY signal at the correct input level, can be connected directly to the CPU.



Figure 2. Typical Application with Am8224 and Am9080A.

APPLICATION PRECAUTIONS WHEN USING Am8224 UP TO 36MHz

Usage with Third Harmonic Crystal or Am9080A-4

The use of the Am8224 with a third harmonic crystal requires a minor modification to the external circuitry associated with the Am8224. The changes are as follows:

- Series capacitor in conjunction with the xtal
- Adding a tuned circuit in the "tank" lead
- Tuning of circuit to proper frequency

It is necessary to maintain the crystal activity to a proper level if an xtal controlled circuit is to operate properly. A 20-30pfd capacitor placed in series will help achieve this level in third overtone crystal, while helping to suppress the fundamental mode. The Am8224 has an auxiliary port provided to allow for a tuned circuit. This tuned circuit eliminates the tendency of the circuit to oscillate at the crystal's fundamental. The tank or tuned circuit must have the following properties:

- 1. It must be parallel resonant at the crystal frequency (third order).
- 2. The off resonance impedance must be low enough to spoil the AC gain of the Am8224.
- 3. The circuit must be DC decoupled (or returned to V_{CC}) at a low impedance (substantially below 100Ω).

All frequency determining components must be in close proximity to the Am8224. Insert crystal and tune tank for best waveform at Pin 12 (OSC). If counter is available, adjust for match of crystal marking. The circuit in Figure 3 will accomplish the above result for the 36MHz range.



- $C_1 = E.F.$ Johnson 275-0430-005 5-30pF Trimmer or Equiv.
- L1 = J.W. Miller Inductor 9230-08

RESET

RESIN

RDYIN 3

READY

SYNC 5

φ2 (TTL)

STSTB

GND [

V_{CC} Ground

Due to the nature of our device (fast switching, higher voltage) it is necessary to provide a bypass capacitor from VCC to ground in the immediate proximity of the Am8224. This insures proper operation of the device while reducing noise spiking on adjacent circuits.

Resin Bypass

The use of a high impedance capacitor for timing R-C, and/or timing components remotely located from the Am8224 device may cause a disturbance to occur during the linear transition region. The capacitor for this function should be of the ceramic type and a value of 1000pF or greater.

This can be cured by placing a >1000pfd ceramic capacitor from Resin (Pin 2) to Ground (Pin 8) in the immediate proximity of the device. This will allow the timing R-C to be placed at will.

APPLICATIONS

The Am8224 can be driven from an external source of frequency by connecting as shown and driven with approximately 500mV over a wide frequency range.



O EXTERNAL

2kΩ

10,000 pF



٦ Vcc

7 XTAL 1

٦ XTAL 2

¢1

l osc

13 TANK

12

10 ___ ¢2

q

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The Am8224 can oscillate without a xtal by placing a small value capacitor $(10 \rightarrow 200 \text{pF})$ in place of a crystal.

