Am8228 • Am8238

System Controller and Bus Driver for 8080A Compatible Microprocessors

Distinctive Characteristics

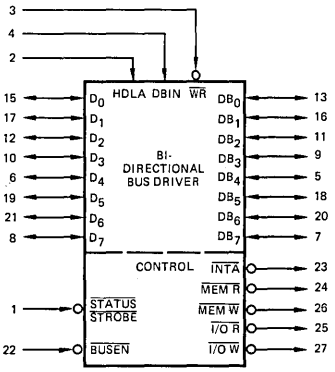
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Am8238-4 high speed version available for use with 1μsec instruction cycle of Am9080A-4
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}/\overline{MEMW}$ pulse width

FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A multiple byte interrupt vector operation.

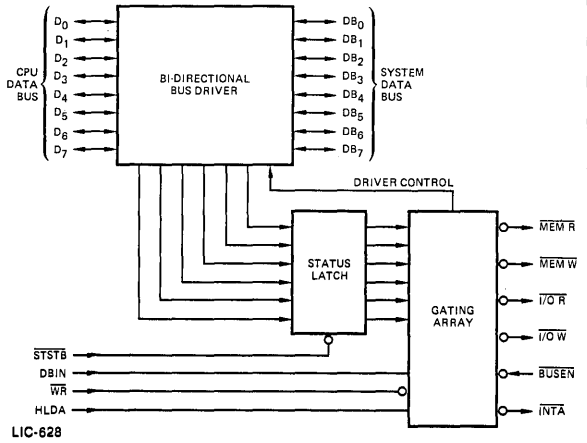
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

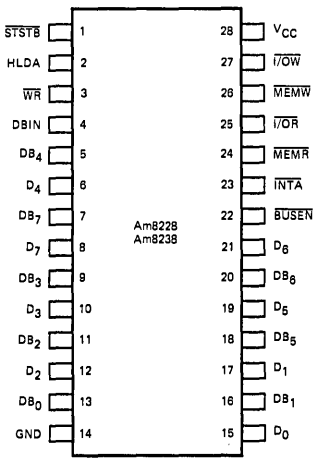
LIC-629

LOGIC DIAGRAM



LIC-628

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-630

ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC
Hermetic DIP	0°C to +70°C		AM8238-4DC*
Molded DIP	0°C to +70°C		AM8238-4PC*

*For use with Am9080A-4 with minimum clock period of 250ns.

8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−1.5V to +7.0V
DC Output Current, Into Outputs	50mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228XM, Am8238XM: T_A = −55°C to +125°C, V_{CC}MIN. = 4.50V, V_{CC}MAX. = 5.50V
Am8228XC, Am8238XC, Am8238-4XC: T_A = 0°C to +70°C, V_{CC}MIN. = 4.75V, V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −10μA	D_0–D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			I_{OH} = −1.0mA	All other outputs		2.4			
V_{OL}	Output Low Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0–D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., I_C = −5.0mA					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				−500	μA
				D_2 and D_6				−750	
				All other inputs				−250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0–DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Offstate Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Outputs)	V_{CC} = 5.0V				−15		−90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

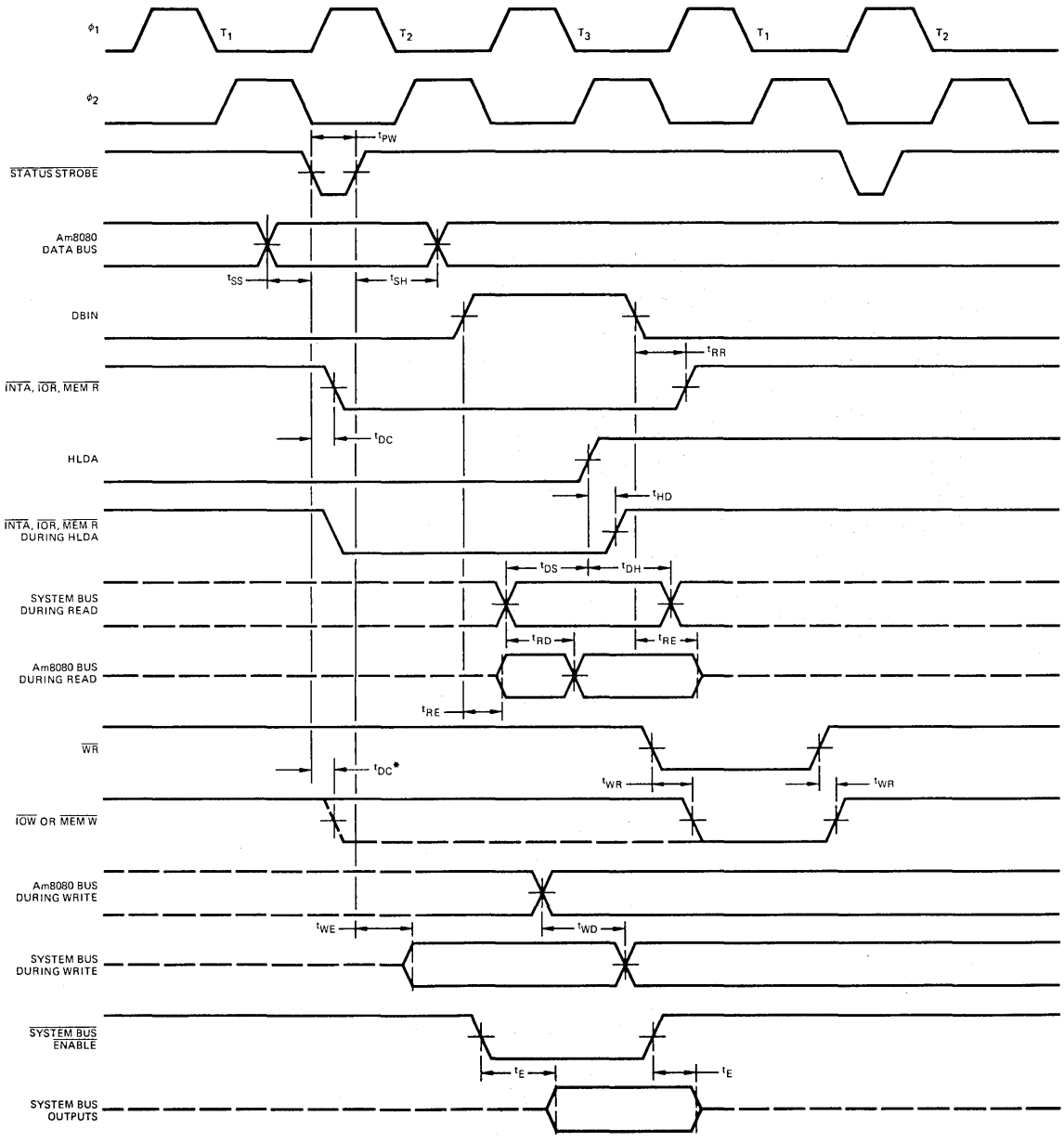
Parameters	Description		Test Conditions	Am8228XM/ Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/ Am8238XC Min.	Typ. (Note 1)	Max.	Am8238-4XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe			22			22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7			12			8.0			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7			5.0			5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to $\overline{MEMR}$		C_L = 100pF	20	30	60	20	30	60	20	30	40	ns
	Delay from $\overline{STSTB}$ to $\overline{INTA}$, $\overline{IOR}$			20	30	60	20	30	60	20	30	45	
	Delay from $\overline{STSTB}$ to all other Control Signals			20	30	60	20	30	60	20	30	60	
t_{RR}	Delay from DBIN to Control Outputs				15	35		15	30		15	30	ns
t_{RE}	Delay from DBIN to 8080A Bus	Enable	C_L = 25pF		25	45		25	45		12	20	ns
		Disable			25	45		25	45		25	35	
t_{RD}	Delay from System Bus to 8080A Bus During Read				15	30		15	30		15	20	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs		C_L = 100pF	5.0	20	45	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$				25	36		25	30		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write			5.0	20	40	5.0	20	40	5.0	20	40	ns
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7				25	35		25	30		20	30	ns
t_{HD}	HLDA to Read Status Outputs				15	28		15	25		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA			10			10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA			20			20			20			ns

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5 V, V_{CC} = 5.0 V T_A = 25°C, f = 1.0 MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

SWITCHING WAVEFORMS



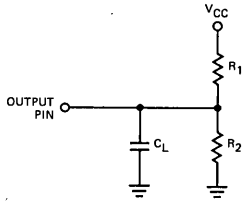
Voltage measurements points: D_0-D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

LIC-631

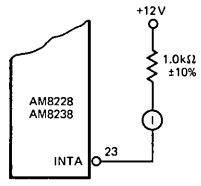
8

TEST CIRCUITS



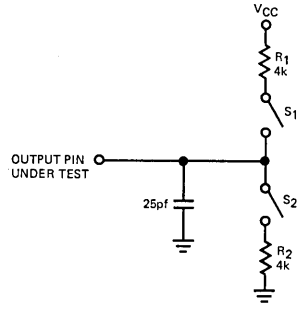
LIC-632

Note 1. For D_0-D_7: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.



LIC-633

INTA (for RST 7)



LIC-634

Test Circuit for DBIN to 8080A BUS

t_{RE}	S_1	S_2
Enable 8080 bus, HIGH-Z to logic "0"	Closed	Open
Enable 8080 bus, HIGH-Z to logic "1"	Open	Closed
Disable 8080 bus, logic "0" to HIGH-Z	Closed	Open
Disable 8080 bus, logic "1" to HIGH-Z	Open	Closed

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

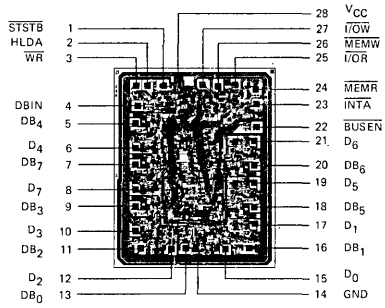
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{I/OR}$	Input/output read strobe output active LOW
$\overline{I/OW}$	Input/output write strobe output active LOW
$\overline{MEM\ R}$	Memory read strobe, output, active LOW
$\overline{MEM\ W}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{INTA}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{WR}$	Write input strobe, active HIGH
$\overline{BUSEN}$	BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{STSTB}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

Metallization and Pad Layout



DIE SIZE 0.110" X 0.136"

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{STSTB}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{WR}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{MEM\ R}$	24	–	10mA	−1mA
$\overline{MEM\ W}$	26	–	10mA	−1mA
$\overline{I/OR}$	25	–	10mA	−1mA
$\overline{IOW}$	27	–	10mA	−1mA
$\overline{BUSEN}$	22	250μA	–	–
$\overline{INTA}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

STATUS WORD CHART

Data Bus Bit	Status Information	TYPE OF MACHINE CYCLE: Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	$\overline{INTA}$	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEM R	1	1	0	1	0	0	0	0	1	0

Ⓝ STATUS WORD

CONTROL SIGNALS:
- $\overline{INTA}$
- (NONE)
- $\overline{INTA}$
- $\overline{I/O\ W}$
- $\overline{I/O\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ R}$

8