Am8253/Am8253-5

Programmable Interval Timer

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

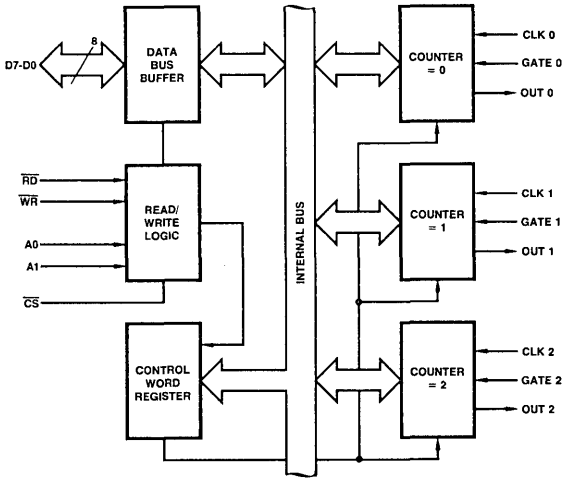
- Count binary or BCD
- Single +5V supply
- 24-pin dual-in-line package
- Three independent 16-bit counters
- DC to 2.5MHz
- Programmable counter modes
- Bus oriented I/O
- 100% reliability assurance testing to MIL-STD-883

GENERAL DESCRIPTION

The Am8253/Am8253-5 are programmable counter/timer chips designed for use as Am8080A/Am8085A Family peripherals. They use NMOS technology with a single +5V supply and are direct replacements for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 2.5MHz. All modes of operation are software programmable. For improved performance, see **Am9513 System Timing Controller.**

BLOCK DIAGRAM



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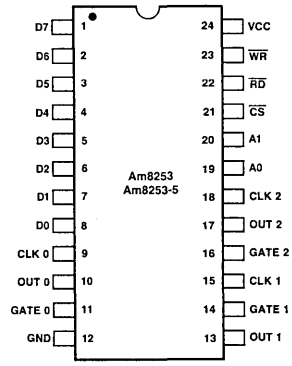
CONNECTION DIAGRAM
Top View

Note: Pin 1 is marked for orientation.



PIN NAMES

D7-D0	Data bus (8-bit)
CLK N	Counter clock inputs
GATE N	Counter gate inputs
OUT N	Counter outputs
$\overline{RD}$	Read counter
$\overline{WR}$	Write command or data
$\overline{CS}$	Chip select
A0-A1	Counter select
VCC	+5 Volts
GND	Ground

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ORDERING INFORMATION

Package Type	Ambient Temperature	Order Numbers	
Molded DIP	0°C ≤ T_A ≤ +70°C	AM8253PC/P8253	AM8253-5PC/P8253-5
Hermetic DIP*		AM8253DC/D8253 AM8253CC/C8253	AM8253-5DC/D8253-5 AM8253-5CC/C8253-5

*Hermetic = Ceramic = DC = CC = D-24-1.

FUNCTIONAL DESCRIPTION

General

The Am8253 is a programmable interval timer/counter specifically designed for use with the Am9080A Microcomputer systems. Its function is that of a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The Am8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the Am8253 to match his requirements, initializes one of the counters of the Am8253 with the desired quantity, then upon command the Am8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature, but also common to most microcomputers can be implemented with the Am8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real-Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the Am8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the Am8253
2. Loading the count registers
3. Reading the count values

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the Am8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the Am8253 that the CPU is outputting data in the form of MODE information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for MODE selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the Am8253. No reading or writing will occur unless the devices is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counter.

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate MODE configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications, and special commands and logic are included in the Am8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write MODE Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

OPERATIONAL DESCRIPTION

General

The complete functional definition of the Am8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the Am8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the Am8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the Am8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the Am8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11).

Control Word Format

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL – Read/Load:

RL1	RL0	
0	0	Counter Latching operation.
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M – MODE:

M2	M1	M0	
0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE DEFINITION

MODE 0: Interrupt on Terminal Count

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

1. Write 1st byte stops the current counting.
2. Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot

The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by one. Subsequent clock pulses decrement the clock by two. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by three. Subsequent clock pulses decrement the count by two until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

MODE 4: Software-Triggered Strobe

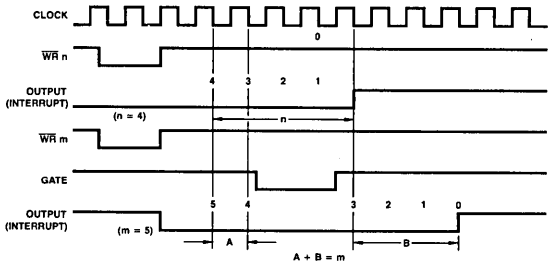
After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

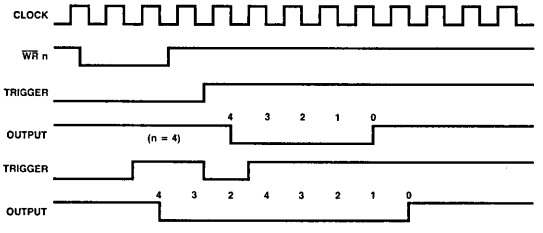
MODE 5: Hardware-Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

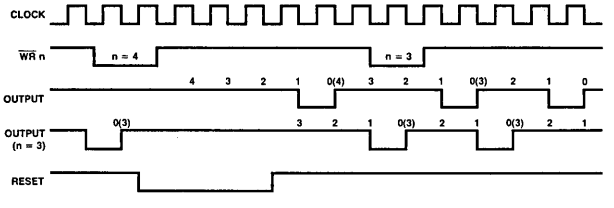
MODE 0. Interrupt on Terminal Count.



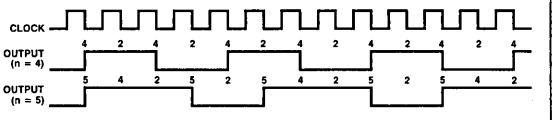
MODE 1. Programmable One-Shot.



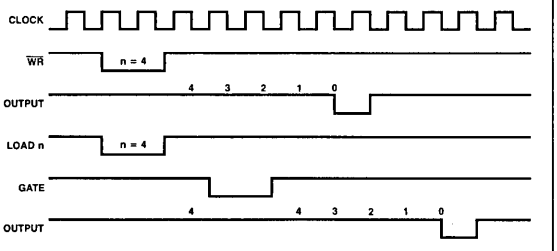
MODE 2. Rate Generator.



MODE 3. Square Wave Generator.



MODE 4. Software-Triggered Strobe.



MODE 5. Hardware-Triggered Strobe.

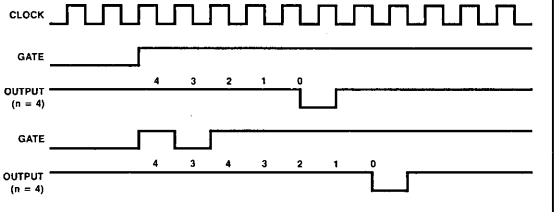


Figure 1. Am8253 Timing Diagrams.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	0 to 70°C
Voltage On Any Pin with Respect to Ground	−0.5V to +7.0V
Power Dissipation	1W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC CHARACTERISTICS (T_A = 0 to 70°C; VCC = 5.0V ±5% unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
VIL	Input Low Voltage		−0.5		0.8	Volts
VIH	Input High Voltage		2.2		VCC+.5V	Volts
VOL	Output Low Voltage	Note 1			0.45	Volts
VOH	Output High Voltage	Note 2	2.4			Volts
IIL	Input Load Current	VIN = VCC to 0V			±10	μA
IOFL	Output Float Leakage	VOUT = VCC to 0V			±10	μA
ICC	VCC Supply Current				140	mA

Notes: 1. Am8253, IOL = 1.6mA; Am8253-5, IOL = 2.2mA.
2. Am8253, IOH = −150μA; Am8253-5, IOH = −400μA.

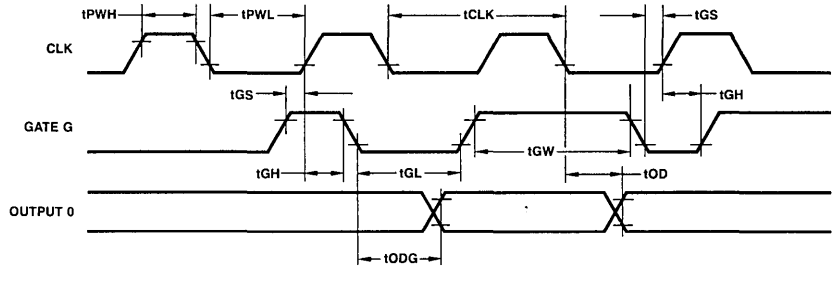
CAPACITANCE T_A = 25°C; VCC = GND = 0V

Parameter	Description	Test Conditions	Min	Typ	Max	Units
CIN	Input Capacitance	fc = 1MHz			10	pF
CI/O	I/O Capacitance	Unmeasured pins returned to VSS			20	pF

CLOCK AND GATE TIMING

		Am8253		Am8253-5		
Parameter	Description	Min	Max	Min	Max	Units
tCLK	Clock Period	380	dc	380	dc	ns
tPWH	High Pulse Width	230		230		ns
tPWL	Low Pulse Width	150		150		ns
tGW	Gate Width High	150		150		ns
tGL	Gate Width Low	100		100		ns
tGS	Gate Set Up Time to CLK↑	100		100		ns
tGH	Gate Hold Time After CLK↑	50		50		ns
tOD	Output Delay From CLK↓ (Note 1)		400		400	ns
tODG	Output Delay From Gate↓ (Note 1)		300		300	ns

Note: 1. Test Conditions: Am8253: CL = 100pF; Am8253-5: CL = 150pF.



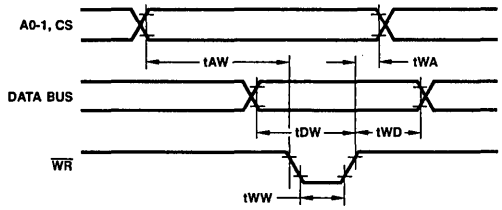
AC CHARACTERISTICS (T_A = 0 to 70°C; VCC = 5.0V ±5%; GND = 0V)

Bus Parameters (Note 1)

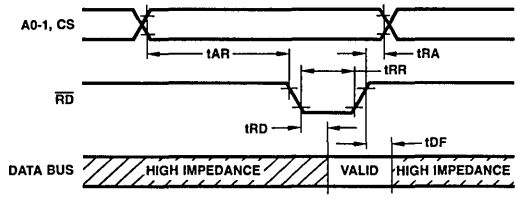
Parameter	Description	Am8253 Min	Am8253 Max	Am8253-5 Min	Am8253-5 Max	Units
Read Cycle:						
tAR	Address Stable Before $\overline{READ}$	50		30		ns
tRA	Address Hold Time for $\overline{READ}$	5		5		ns
tRR	$\overline{READ}$ Pulse Width	400		300		ns
tRD	Data Delay From $\overline{READ}$ (Note 2)		300		200	ns
tDF	$\overline{READ}$ to Data Floating	25	125	25	100	ns
tRV	Recovery Time Between READ and Any Other Control Signal	1		1		μs
Write Cycle:						
tAW	Address Stable Before $\overline{WRITE}$	50		30		ns
tWA	Address Hold Time for $\overline{WRITE}$	30		30		ns
tWW	$\overline{WRITE}$ Pulse Width	400		300		ns
tDW	Data Set Up Time for $\overline{WRITE}$	300		250		ns
tWD	Data Hold Time for $\overline{WRITE}$	40		30		ns
tRV	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

Notes: 1. AC timings measured at VOH = 2.2, VOL = 0.8.
2. Test Conditions: Am8253, CL = 100pF, Am8253-5: CL = 150pF.

Write Timing



Read Timing



Input Waveforms for AC Tests