Am9130 • Am91L30

1024 x 4 Static R/W Random Access Memories

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DISTINCTIVE CHARACTERISTICS

- 1k x 4 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- Low operating power
  - 578mW max., 9130
  - 368mW max., 91L30
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst-case
- High output drive – two standard TTL loads
- DC power-down mode – reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain – no large surges
- Unique Memory Status signal
  - improves performance
  - self clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

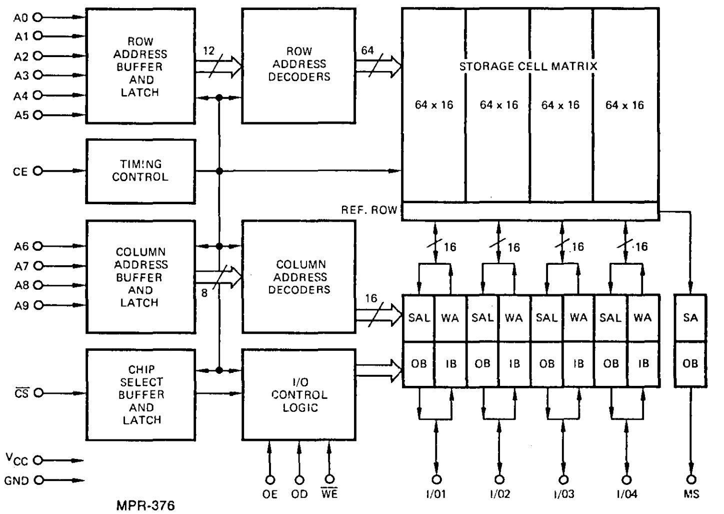
The Am9130 and Am91L30 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

BLOCK DIAGRAM



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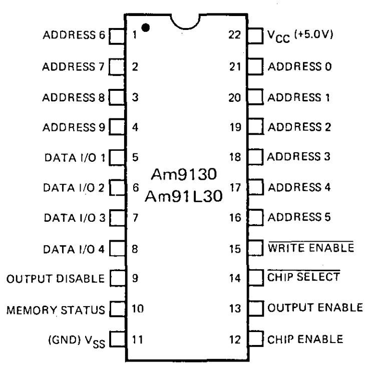
CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature	Power Type	Access Time 500ns	400ns	300ns	250ns	200ns
Molded	$0°C \leq T_A \leq +70°C$	STD	AM9130APC	AM9130BPC	AM9130CPC	AM9130DPC	AM9130EPC
		LOW	AM91L30APC	AM91L30BPC	AM91L30CPC	AM91L30DPC	
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	AM9130ADC	AM9130BDC	AM9130CDC	AM9130DDC	AM9130EDC
		LOW	AM91L30ADC	AM91L30BDC	AM91L30CDC	AM91L30DDC	
	$-55°C \leq T_A \leq +125°C$	STD	AM9130ADM	AM9130BDM	AM9130CDM		
		LOW	AM91L30ADM	AM91L30BDM	AM91L30CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE		POWER-DOWN RANGE			
V_{CC}	V_{SS}	V_{CC}	V_{SS}	Ambient Temperature	Part Number
$4.75V \leq V_{CC} \leq 5.25V$	0V	$1.5V \leq V_{CC} \leq 5.25V$	0V	$0°C \leq T_A \leq +70°C$	AM91X30XDC
$4.50V \leq V_{CC} \leq 5.50V$	0V	$1.5V \leq V_{CC} \leq 5.50V$	0V	$-55°C \leq T_A \leq +125°C$	AM91X30XDM

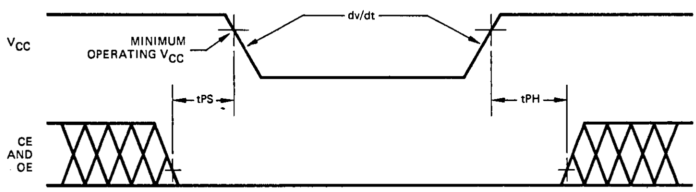
ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$	2.2			2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	μA
I_{CC}	V_{CC} Supply Current	Max. V_{CC} Output disabled	$T_A = 25°C$		50	100		40	65	mA
			$T_A = 0°C$			110			70	
			$T_A = -55°C$			125			80	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF
$C_{I/O}$	I/O Capacitance				6.0	9.0		6.0	9.0	pF

POWER DOWN CHARACTERISTICS

Parameter	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Unit
dv/dt	V_{CC} Rate of Change					3.0			3.0	V/μs
tPS	Power Down Set-Up Time			tEL			tEL			ns
tPH	Power Up Hold Time			tEL			tEL			ns
I_{PD}	I_{CC} in Standby (Note 2)	$V_{CC} = 2.0V$	$T_A = 25°C$		36	72		28	55	mA
			$T_A = 0°C$			78			60	mA
			$T_A = -55°$			89			68	mA
		$V_{CC} = 1.5V$	$T_A = 25°C$		20	52		16	45	mA
			$T_A = 0°C$			56			48	mA
			$T_A = -55°C$			64			55	mA

POWER DOWN WAVEFORM



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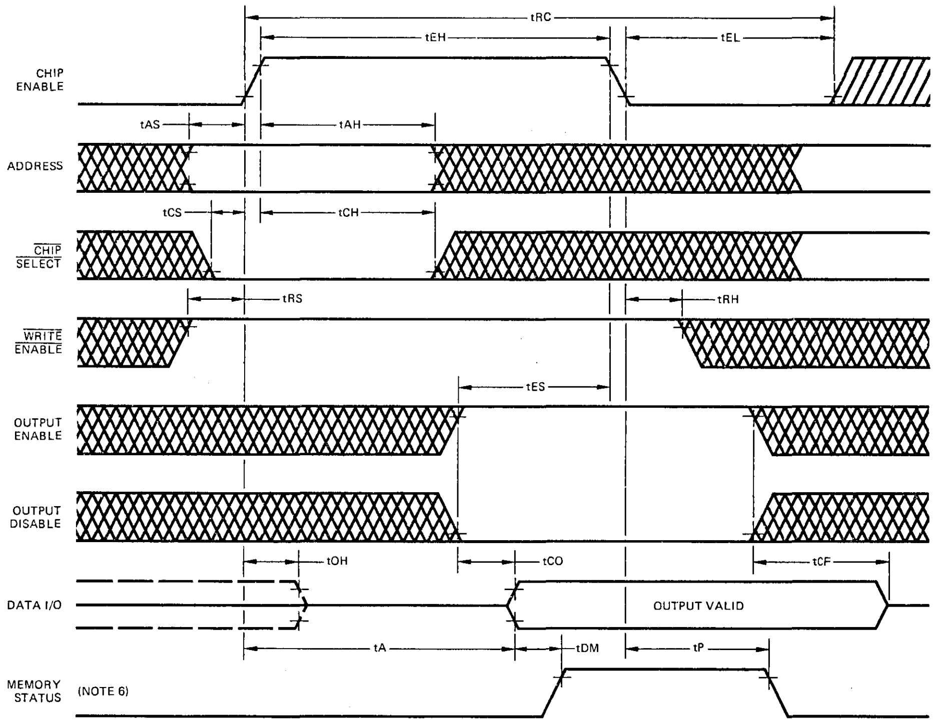
SWITCHING CHARACTERISTICS over operating range

READ CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Am9130A Am91L30A Max.	Am9130B Am91L30B Min.	Am9130B Am91L30B Max.	Am9130C Am91L30C Min.	Am9130C Am91L30C Max.	Am9130D Am91L30D Min.	Am9130D Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tRC	Read Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (Note 3) (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Note 14)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Note 14)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRH	Chip Enable to Read Hold Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay (Note 3)	0		0		0		0		0		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tES	Output Enable to CE LOW Set-Up Time (Note 12)	90		75		60		55		50		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval (Note 14)		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ CYCLE



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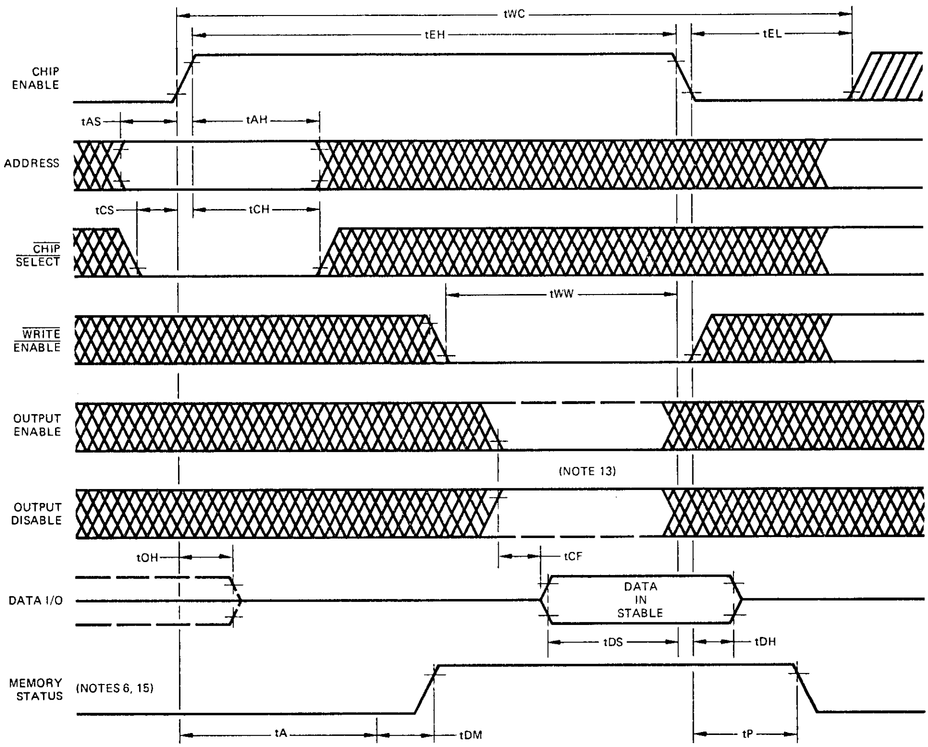
SWITCHING CHARACTERISTICS over operating range

WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Am9130A Am91L30A Max.	Am9130B Am91L30B Min.	Am9130B Am91L30B Max.	Am9130C Am91L30C Min.	Am9130C Am91L30C Max.	Am9130D Am91L30D Min.	Am9130D Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tWC	Write Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (CE to Output ON Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

WRITE CYCLE



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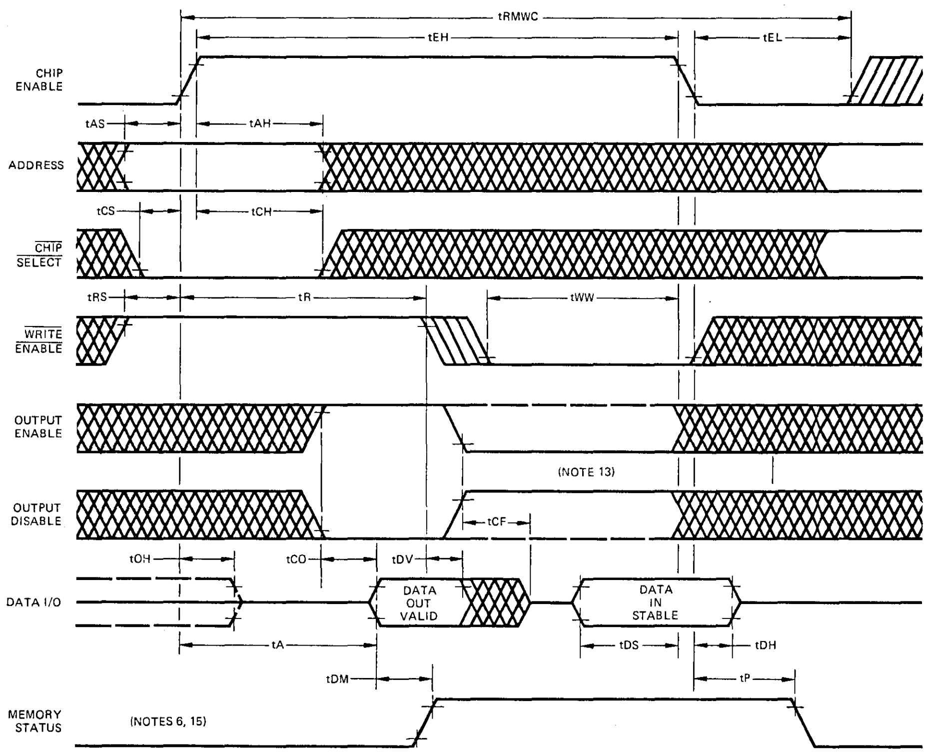
SWITCHING CHARACTERISTICS over operating range

READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Max.	Am9130B Am91L30B Min.	Max.	Am9130C Am91L30C Min.	Max.	Am9130D Am91L30D Min.	Max.	Am9130E Min.	Max.	Unit
tRMWC	R/M/W Cycle Time (Notes 5, 16)	1170		950		740		625		520		ns
tA	Access Time (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	900		730		570		480		400		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay	0		0		0		0		0		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tDV	Data Valid after Write Delay	10		10		10		10		10		ns
tR	Read Mode Hold Time	tA		tA		tA		tA		tA		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING CHARACTERISTICS

READ/MODIFY/WRITE CYCLE



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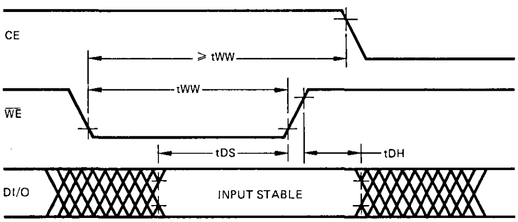
NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{\text{WE}}$ transition times are assumed to be ≤10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{\text{WE}}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{\text{WE}}$ high while CE is high, the following timing applies:



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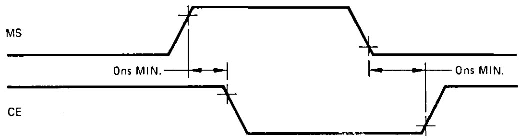
11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH ≥ tA and tEL ≥ tP:



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15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{\text{WE}}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{\text{WE}}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) +tCF (max.) + tDS (min.). This provides a conservative design with no I/O overlap and assumes that tCF begins at the end of the tR time. Other designs with somewhat shorter R/M/W cycles are possible.

FUNCTION DESCRIPTION

Block Diagram

The block diagram for the Am9130 shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing 4 bits. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) are decoded and used to select 4 of 64 columns for the sense amplifiers. Thus a single cell is connected to each output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

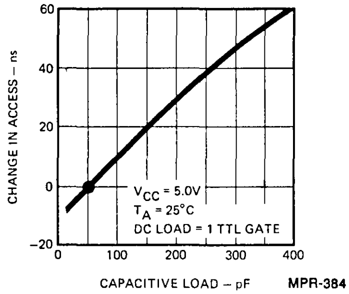
Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

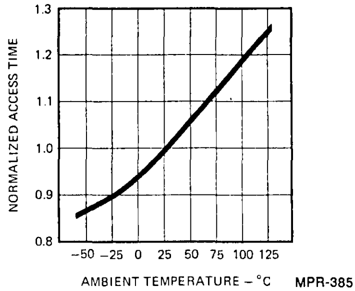
The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

CHARACTERISTICS

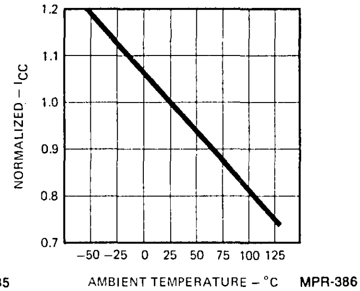
Access Change Versus Capacitive Load



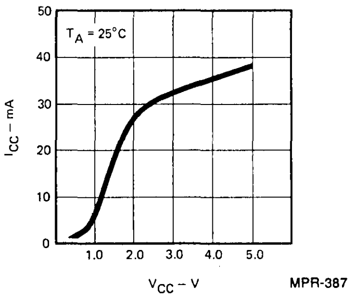
Access Time Versus Ambient Temperature



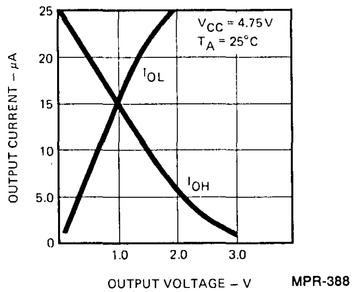
Supply Current Versus Ambient Temperature



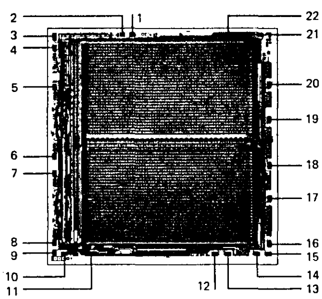
Typical I_{CC} Versus V_{CC}



Typical Output Currents Versus Output Voltage

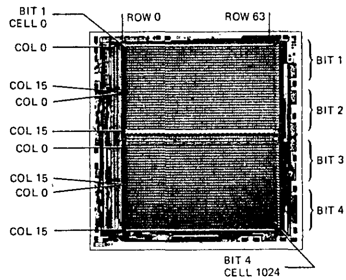


Metallization and Pad Layout



DIE SIZE 0.192" X 0.197"

Bit Map



For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A9