Am9112/Am91L12 FAMILY

256x4 Static R/W Random Access Memories

Part Number	Am2112	Am2112-2	Am9112A Am91L12A	Am9112B Am91L12B	Am9112C Am91L12C	Am9112D
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns

Distinctive Characteristics

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
  20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads guaranteed
- High noise immunity — full 400mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns.
- Single +5V power supply — tolerances ±5% commercial, ±10% military
- Bus oriented I/O data
- Zero address, set-up, and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

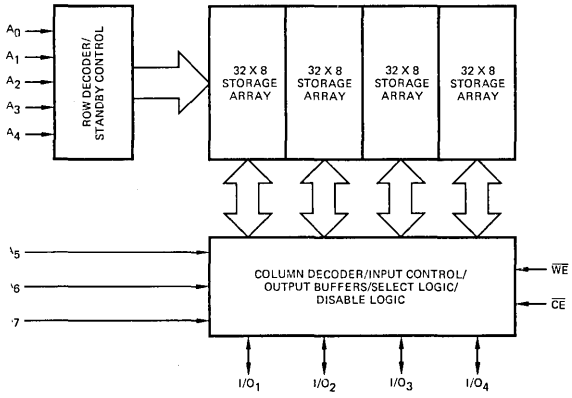
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

Am9112 BLOCK DIAGRAM



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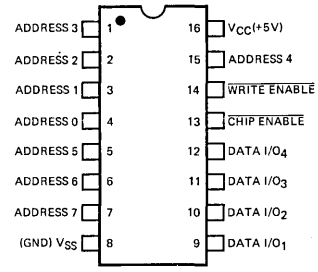
CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

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ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times					
			1000ns	650ns	500ns	400ns	300ns	250ns
0°C to +70°C	Molded DIP	Standard	P2112	P2112-2	AM9112APC	AM9112BPC	AM9112CPC	AM9112DPC
		Low			AM91L12APC	AM91L12BPC	AM91L12CPC	
	Hermetic DIP	Standard	C2112	C2112-2	AM9112ADC	AM9112BDC	AM9112CDC	AM9112DDC
		Low			AM91L12ADC	AM91L12BDC	AM91L12CDC	
−55°C to +125°C	Hermetic DIP	Standard			AM9112ADM	AM9112BDM	AM9112CDM	
		Low			AM91L12ADM	AM91L12BDM	AM91L12CDM	
	Hermetic Flat Pack	Standard			AM9112AFM	AM9112BFM		
		Low			AM91L12AFM	AM91L12BFM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9112PC, Am9112DC $T_A = 0°C$ to $+70°C$
Am91L12PC, Am91L12DC $V_{CC} = +5V \pm 5\%$

Parameters	Description	Test Conditions			Am9112/Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -200\mu A$			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.25V$				10	μA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			5.0	μA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C/D/E		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC2}			$T_A = 0°C$	Am9112A/B		55	
				Am9112C/D/E		60	
				Am91L12A/B		33	
				Am91L12C		36	

ELECTRICAL CHARACTERISTICS

Am9112DM, Am9112FM $T_A = -55°C$ to $+125°C$
Am91L12DM, Am91L12FM $V_{CC} = +5.0V \pm 10\%$

Parameters	Description	Test Conditions			Am9112/Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$		2.4		Volts
			$V_{CC} = 4.50V$		2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.5V$				10	μA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			10	μA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC3}			$T_A = -55°C$	Am9112A/B		60	
				Am9112C		65	
				Am91L12A/B		37	
				Am91L12C		40	

CAPACITANCE

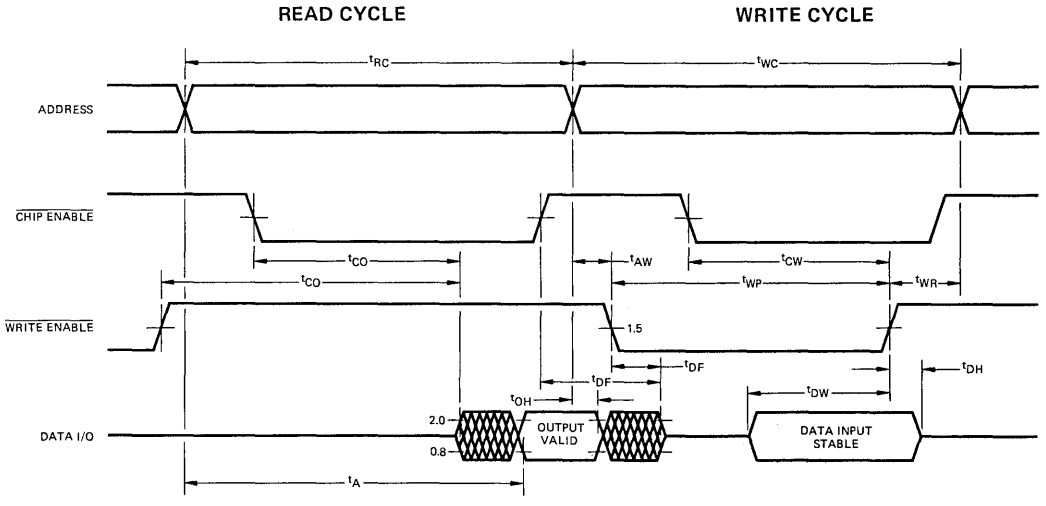
Parameters	Description	Test Conditions		Typ.	Max.	Uni
C_{IN}	Input Capacitance, $V_{IN} = 0V$	$T_A = 25°C$, f = 1 mHz	Am2112	4.0	8.0	pF
			Am9112/Am91L12	3.0	6.0	
C_{OUT}	Output Capacitance, $V_{OUT} = 0V$		Am2112	10	18	pF
			Am9112/Am91L12	8.0	11	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

		Am9112A Am91L12A		Am9112B Am91L12B		Am9112C Am91L12C		Am9112D		
Parameters	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{RC}	Read Cycle Time	500		400		300		250		ns
t_A	Access Time		500		400		300		250	ns
t_{CO}	Output Enabled to Output ON Delay (Note 1)	5.0	175	5.0	150	5.0	125	5.0	100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
t_{DF}	Output Disabled to Output OFF Delay (Note 2)	5.0	125	5.0	100	5.0	100	5.0	75	ns
t_{WC}	Write Cycle Time	500		400		300		250		ns
t_{AW}	Address Set-up Time	0		0		0		0		ns
t_{WR}	Address Hold Time	0		0		0		0		ns
t_{WP}	Write Pulse Width (Note 3)	175		150		125		100		ns
t_{CW}	Chip Enable Set-up Time	175		150		125		100		ns
t_{DW}	Input Data Set-up Time	150		125		100		85		ns
t_{DH}	Input Data Hold Time (Note 4)	0		0		0		0		ns

SWITCHING WAVEFORMS (Note 5)



Notes:
1. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and t_{DF} defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min.)} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
5. See "Application Information" section of this specification.

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DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Output Enable Time. The time during which $\overline{CE}$ must be LOW and $\overline{WE}$ must be HIGH prior to data on the output.

t_{OH} Minimum time which will elapse between change of address and any change on the data output.

t_{DF} Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

POWER DOWN STANDBY OPERATION

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or; in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

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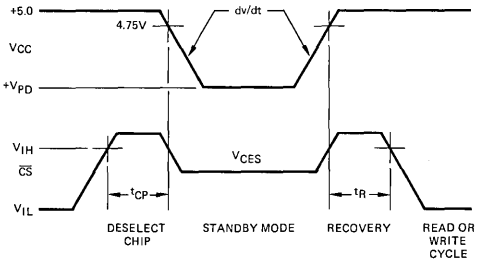
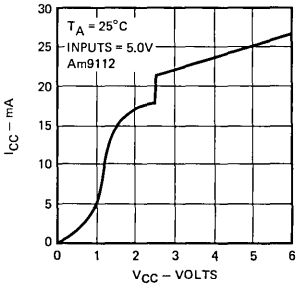
STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

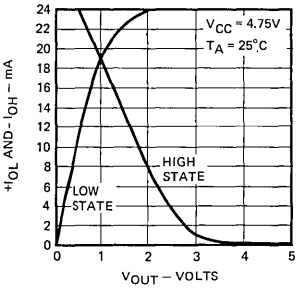
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	25	mA
				Am9112		13	31	
			$V_{PD} = 2.0V$	Am91L12		13	31	
				Am9112		17	41	
		$T_A = -55°C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	28	mA
				Am9112		13	34	
			$V_{PD} = 2.0V$	Am91L12		13	34	
				Am9112		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



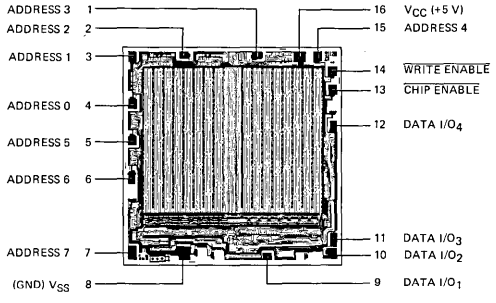
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

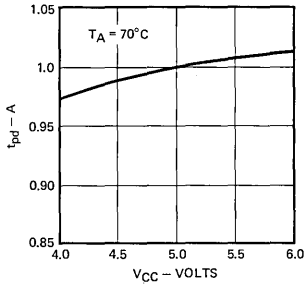


Metallization and Pad Layout

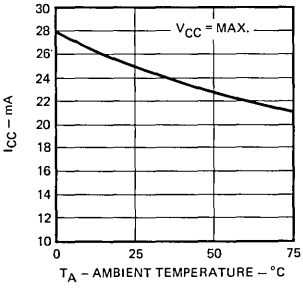


DIE SIZE 0.132" X 0.131"

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



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APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

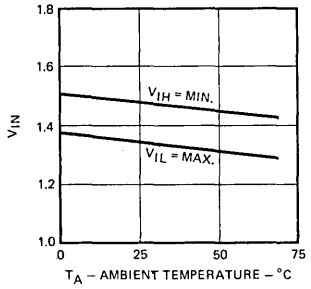
This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

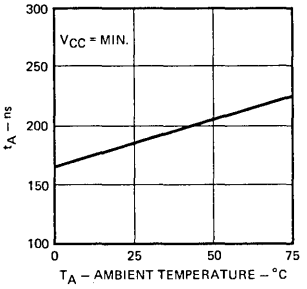
These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure t_{WP} is at least $t_{DW} + t_{DF}$ and delay the input data until t_{DF} following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is high for at least t_{DF} preceeding the falling edge of $\overline{WE}$, t_{WP} may assume the minimum specified value. When $\overline{CE}$ is high for t_{DF} before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25ns.

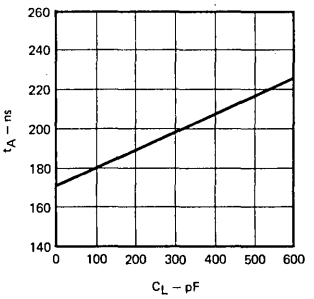
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L



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