Am9232 • Am9233

4096 X 8 Read Only Memory

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- 4096 X 8 organization
- No clocks or refresh required
- Access time selected to 300ns
- Fully capacitive inputs – simplified driving
- 2 mask programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three state output buffers – simplified expansion
- Drives two TTL loads
- Single +5 volt power supply
- Two different pinouts for universal application
- Low power dissipation
- 100% MIL-STD-883 reliability assurance testing
- Non-connect option on chip selects.

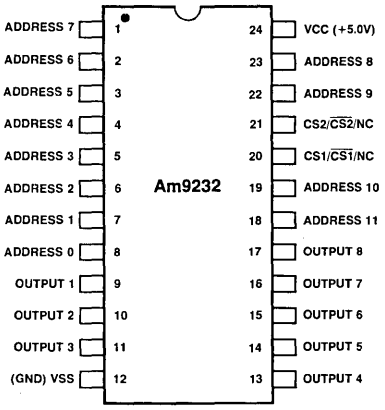
FUNCTIONAL DESCRIPTION

The Am9232/33 devices are high performance, 32,768-bit, static, mask programmed, read only memories. Each memory is implemented as 4096 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes of 4096 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9232/33 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

CONNECTION DIAGRAMS
Top Views



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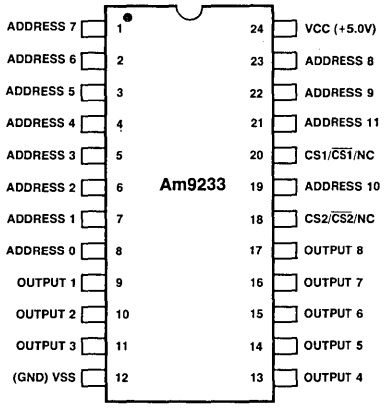

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Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450ns	300ns
Molded	$0°C \leq T_A \leq +70°C$	AM9232/33BPC	AM9232/33CPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9232/33BCC	AM9232/33CCC
Side-Brazed Ceramic	$-55°C \leq T_A \leq +125°C$	AM9232/33BDM	
	$0°C \leq T_A \leq +70°C$	AM9232/33BDC	AM9232/33CDC

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9232DC/PC/CC	0°C ≤ T_A ≤ +70°C	+5.0V ±5%	0V
Am9232/33DM	−55°C ≤ T_A ≤ +125°C	+5.0V ±10%	0V

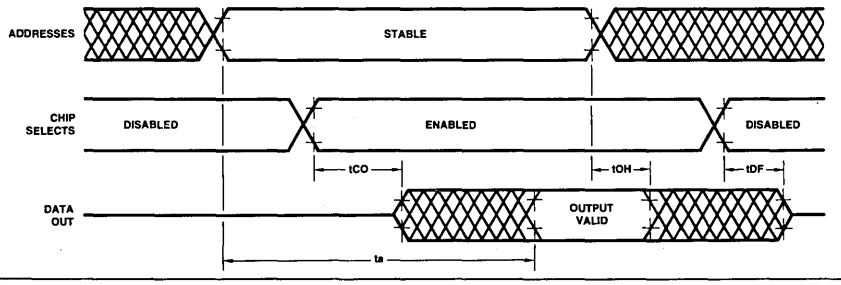
ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am9232/Am9233 Min.	Max.	Unit
VOH	Output HIGH Voltage	IOH = −200μA	VCC = 4.75	2.4		Volts
			VCC = 4.50	2.2		
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage			2.0	VCC+1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	Volts
ILI	Input Load Current	VSS ≤ VI ≤ VCC			10	μA
ILO	Output Leakage Current	VSS ≤ VO ≤ VCC Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
ICC	VCC Supply Current		0°C		80	mA
			−55°C (DM)		100	
CI	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V			7.0	pF
CO	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am9232/33B Min.	Am9232/33B Max.	Am9232/33C Min.	Am9232/33C Max.	Unit
ta	Address to Output Access Time	tr = tf = 20ns Output Load: one standard TTL gate plus 100pF (Note 1)		450		300	ns
tCO	Chip Select to Output ON Delay			150		120	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		ns
tDF	Chip Select to Output OFF Delay			150		120	ns

SWITCHING WAVEFORMS



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PROGRAMMING INTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9232 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	9232 or 9233
65 thru 72	Optional information

SECOND CARD

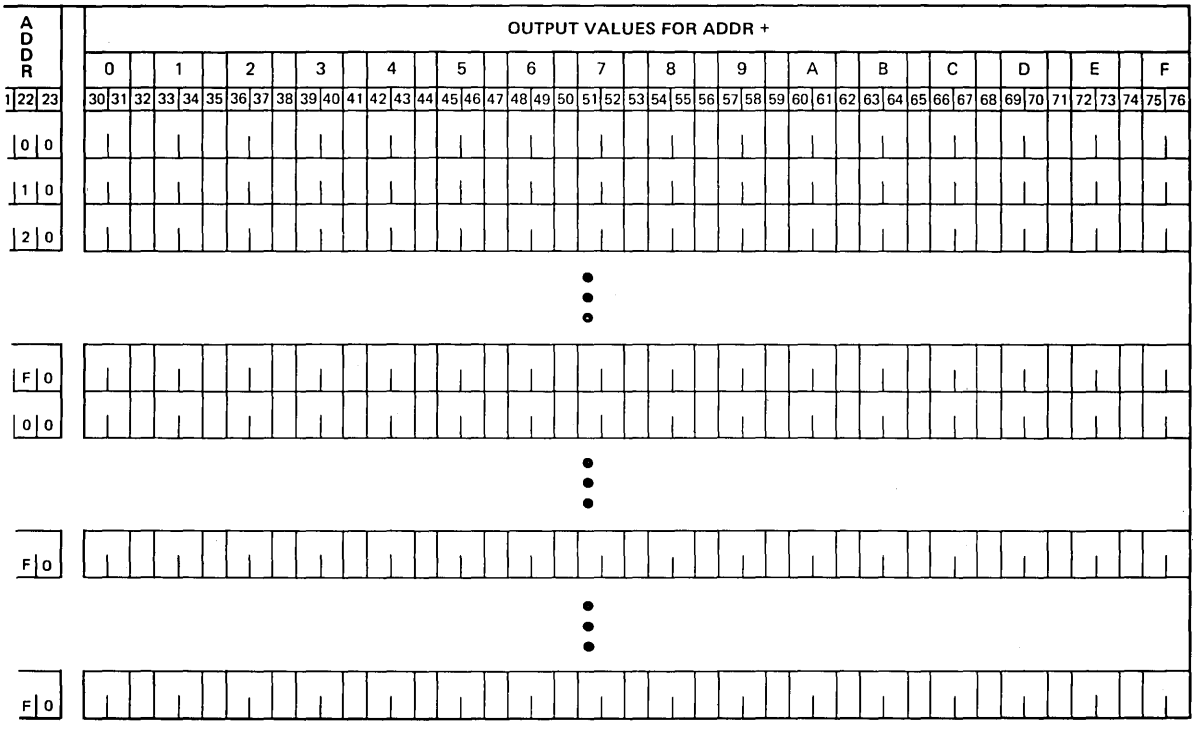
Column Number	Description
31	CS2 input required to select chip (0 or 1); If CS2 = NC, column 31 = 2.
33	CS1 input required to select chip (0 or 1); If CS1 = NC, column 33 = 2.

Two options are provided for entering the data pattern with the remaining cards.

OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 4096 data cards are required.

Column Number	
8, 10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A11) in column 8 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 256 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through FF:256 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



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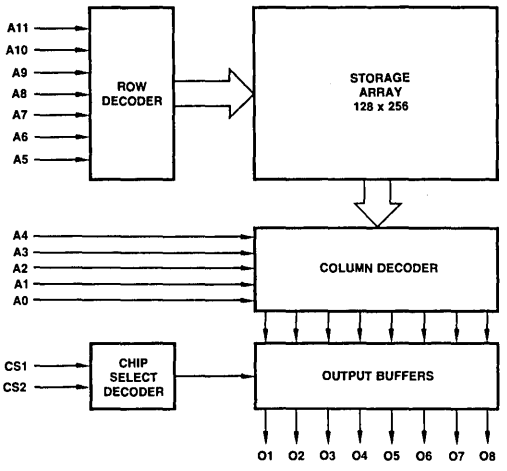
BLOCK DIAGRAM



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